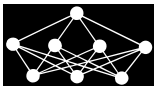

HIERARCHICAL APPROACH TO DIAGNOSIS OF MIXED-MODE CIRCUITS USING ARTIFICIAL NEURAL NETWORKS

*Miona Andrejević Stošović, Dragiša Milovanović, Vančo Litovski**

Abstract: Feed-forward artificial neural networks (ANNs) have been applied to the diagnosis of mixed-mode electronic circuit. In order to tackle the circuit complexity and to reduce the number of test points, hierarchical approach to the diagnosis generation was implemented with two levels of decision: the system level and the circuit level. For every level, using the simulation-before-test (SBT) approach, fault dictionary was created first, containing data relating to the fault code and the circuit response for a given input signal. ANNs were used to model the fault dictionaries. During the learning phase, the ANNs were considered as an approximation algorithm to capture the mapping enclosed within the fault dictionary. Later on, in the diagnostic phase, the ANNs were used as an algorithm for mapping the measured data into fault code, which is equivalent to searching the fault dictionary performed by some other diagnostic procedures. At the topmost level, the fault dictionary was split into parts simplifying the implementation of the concept. A voting system was created at the topmost level in order to distinguish which ANN's output is to be accepted as the final diagnostic statement. The approach was tested on an example of an analog-to-digital converter, and only one test point was used, i.e. the digital output. Full diversity of faults was considered in both digital (stuck-at and delay faults) and analog (parametric and catastrophic faults) parts of the diagnosed system. Special attention was paid to the faults related to the A/D and D/A interfaces within the circuit.

Key words: *Fault diagnosis, hierarchical systems, mixed analog-digital circuits, neural networks*

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1. Introduction

Whenever we think about why something does not behave as it should, we are starting the process of diagnosis. Diagnosis is, therefore, a common activity in our

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everyday lives [1]. Every system is liable to faults or failures. In most general terms, a fault is every change in a system that prevents it from operating in proper manner. We define diagnosis as the task of identifying the cause and location of a fault manifested by some observed behavior. This is often considered to be a two-stage process: first the fact that fault has occurred must be recognized – this is referred to as *fault detection*. Secondly, the *nature and location* should be determined such that appropriate remedial action may be initiated.

The general structure of a diagnostic system is shown in Fig. 1. Signals $u(t)$ and $y(t)$ are input and output to the system, here denoted as the "Process", respectively. Faults and disturbances (in our considerations measurement errors) also influence the system under test but there is no information about the values of these errors. The task of the diagnostic system is to generate a diagnostic statement $\boldsymbol{S}$, which contains information about fault modes that can explain the behavior of the Process. Note that the diagnostic system is assumed to be passive, i.e. it cannot affect the Process itself.

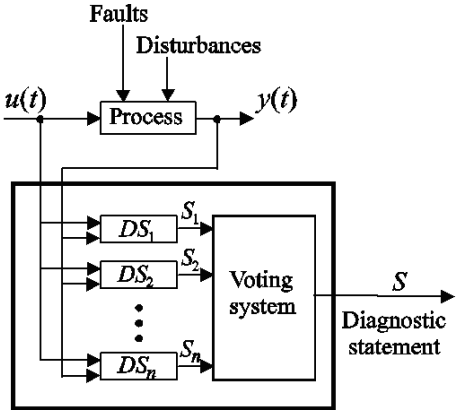

Fig. 1 *A general diagnostic system.*

The whole diagnostic system can be divided into smaller parts here referred to as tests. These tests are also diagnostic systems, DS_i $(i = 1, \ldots, n)$. It is assumed that each of them generates a diagnostic statement (or hypothesis) $S_i (i = 1, \ldots, n)$. The purpose of the decision logic (voting system) is then to combine this information in order to form the final diagnostic statement $\boldsymbol{S}$. Modern automatic test pattern generator may support such concepts [2].

The number of possible faults in an electronic system may be large and a fault can be located anywhere in the system. In order to diagnose in such conditions, we adopted a hierarchical approach where successive diagnostic statements are generated as the level of description of the system is lowered going down towards the fault itself [3], [4]. This allows for smaller sets of faults to be considered at a time at a given hierarchical level.

The very process of generating the final diagnostic statement may be based on different concepts. When combinational digital circuits are to be diagnosed, one usually creates fault tables and searches for them to locate the fault. Localization

of faults in sequential digital circuits is performed by edge-pin testing or by guided-probe testing [5]. Due to the diversity of the stimuli and to different domains to be considered, analog diagnosis was covered by many concepts, as described in detail in [6]. To our knowledge there were no unified concepts proposed for diagnosis of mixed-signal circuits. Here we suggest implementation of ANNs for diagnosis of electronic systems no matter of the structure. No specific learning algorithms are advised. In addition, the very same concept and, accordingly, the same ANN structure is used at every hierarchical level of decision-making involving different signal domains. It is our opinion that no other concept may be implemented in such a straightforward manner as the ANNs. Here comes our motivation for this research.

After shortly reviewing the existing concepts of diagnosis, in the next section, we will consider the specifics of diagnosis of mixed-signal electronic circuits. In fact, hierarchical concept to mixed-mode electronic circuits diagnosis will be described here for the first time. That may be considered as the main contribution of this paper since, to our knowledge, no similar results have been published until now. The new concepts implemented will be described. An example will be given illustrating both the nature of the subject and the underlying ideas.

2. Concepts of Diagnosis

Besides a human expert performing the diagnosis, one needs tools that will help, and ideally, perform the diagnosis automatically. Such tools are a great challenge to design engineers because, usually, the diagnostic problem is underspecified. In addition, it is a deductive process with one set of data creating, in general, an unlimited number of hypotheses among which we try to find a solution. This is why the research community continues to be attracted by this problem [7].

Thanks to the advances in computational intelligence in the last decades new diagnostic paradigms have been applied based on: model-based concepts [1]; production-rule based artificial intelligence [8], [9]; ANNs [10]; genetic algorithms [11]; and fuzzy-reasoning [12]; all trying to create an approach that exhibits properties that we might consider to be "intelligent behavior". A comprehensive overview of the complete subject of diagnosis of analog electronic circuit may be found in [6]. Based on that, we claim that what we are reporting now is a unique and successful attempt to hierarchically diagnose mixed-mode circuit.

In order to get an idea of why and how ANNs are applied to mixed-mode electronic circuit diagnosis, the application of the diagnostic concept (Fig. 1) will be first elaborated in some detail. It involves collaboration of design, test, and field engineers and mutual distribution of responsibilities throughout the life cycle of an electronic product. We assume that field engineers are expected to react after a functional failure of the system. In order to diagnose such a system, they need to be supplied with: testing equipment, a list of specific measurements to be done (including a set of signals and test points), and diagnostic software to process the measurement data. A similar set of data and tools would be given to a test engineer in a production-plant environment in order to evaluate the production yield and create feedback to process engineers when prototyping the circuit.

We believe, however, that design engineers are best acquainted with the product and are most qualified and capable to synthesize test and diagnostic signals, and procedures. The importance of that comes especially to the fore when mass produced systems are to be diagnosed before shipping to customers. This means that the simulation-before-test (SBT) approach has to be applied to create fault dictionaries containing exhaustive lists of faults and corresponding responses. The fault dictionary is, in fact, a table representing the mapping from the fault list into a list of faulty (or possibly, fault-free) responses. In that way, the diagnostic process becomes a search through the fault dictionary. Alternatively, modern diagnostic techniques using traditional artificial intelligence and reasoning methods typically fall into the simulation-after-test (SAT) category. This will increase the time spent on diagnosing the system at production time [13]. SBT systems typically require more initial computational costs, but provide faster diagnosis at production time, this being an additional reason why this concept was accepted here.

We claim here that ANNs, being universal approximators [14], are the best way both to capture the mapping, and to reproduce the fault code based on measured data, thereby to perform diagnosis. If a large number of faults and a reduced number of outputs are to be conceived at the same time, thanks to the resemblance of the fault effects, the search process within the fault dictionary requires a highly sophisticated classification algorithm. We will show in the next section how ANNs can perform successfully in the most difficult conditions.

3. Diagnosis of Mixed-Mode Circuit

The explosion of integrated circuit technology has brought with it some difficult testing problems. The recent growth of mixed analogue and digital circuits complicates the testing problem even further. It becomes more complicated to determine a set of input test signals and output measurements that will provide a high degree of fault coverage. There is also a timing problem when testing such circuits even on the fastest automated equipment.

Analogue electronic circuits are known to be difficult to test and diagnose. Apart from the huge number of possible faults, this difficulty is a consequence of the inherent nonlinearity of this circuit category. Even linear circuits (having linear input-output signal interdependence) exhibit non-linear relations between circuit-parameter values and the output response. There are no linear active networks. Active networks are non-linear with non-linear reactive elements. They may be linearized and thought of as such in situations where signal and parameter changes are small in comparison to nominal values. When large parameter changes or even catastrophic faults occur (affecting the DC quiescent state), however, one must distinguish between linear and analogue circuits. This, unfortunately, is not the case in most research reports which bring confusion into the subject [15], [16].

A specific aspect of diagnosis is the number and location of the test points. Simply, we can say that internal test points should be avoided, and measurements on the primary inputs and outputs are preferred. This is not only related to their automatic accessibility but also to the nature of the diagnostic reasoning. Namely, one looks for functionality in order to start diagnosing, the function being seen at the primary terminals. Of course, in order to compensate for the reduced number

of test points, additional measurements with different types of applied signals may be needed to extract complete information about the system behavior. For complex analogue systems, however, hierarchical approaches based on decomposition [3], [4], [7], [17], [18] are inevitable, provided that no propagation of the fault effect arises between partitions. That is not easy to achieve. Of course, there are circuits that may be partitioned based on functionality known *a priori* from the design process, as mentioned in the introduction.

In this paper, we describe the results of applying feed-forward ANNs to the diagnosis of non-linear dynamic electronic circuits that are mixed with digital ones with no restriction to the number and type of faults. This method is based on fault dictionary creation and using an ANN for data compression by memorizing the table representing the fault dictionary. The ANN created in this way is, consequently, used for diagnosis by applying to its inputs the signals obtained by measurement of faulty network. This process may be considered as looking-up of a fault in the fault dictionary. The ANN finds the most probable *fault code* that corresponds to the measured signals. The procedure was earlier applied to analog circuits and illustrated in [6].

A specific experiment is described in [6] related to the robustness of the ANN used as a fault code classifier for analogue circuit diagnosis. Namely, the measured data were corrupted by disturbances, as shown in Fig. 1. That was random addition of noise (up to $\pm 5\%$). Not in a single case was false response obtained. Here, however, since our targets were implementation of hierarchical concept and diagnosis of mixed-signal circuits, that experiment was not performed and remains to be done later as a task for future work.

Putting the SBT approach in the general context of diagnosis, we first note that the fault dictionary contains all the knowledge we need. In other words, all hypotheses are memorized (within the ANN) and no further hypothesis needs to be created after the dictionary is known. This is equivalent to the structural concept of testing. The fault not conceived in advance cannot be tested or diagnosed. Now, after measurement, we look among the hypotheses (by searching the dictionary, i.e. by running the ANN) to find the one most similar to the actual (faulty) circuit response. The difficulties here are the complexity of the search and the decision algorithm that finds the "most similar" entry in the dictionary. As will be shown by an example, this can be an extremely difficult task that has been successfully solved using ANNs.

For a mixed signal system, such the one depicted in Fig. 2, we are faced with additional difficulties related to the different nature of the responses sought at different nodes. In order to tackle that problem the fault dictionary created at the system level was partitioned in two parts enabling implementation of the concept described in Fig. 1.

The ANNs used for this diagnostic example are the well-known feed-forward neural networks structured in three layers. The network topology will be graphically depicted later on, while presenting the example. They have only one hidden layer, which has been proved sufficient for this kind of applications, i.e. approximation [19]. The neurons in the hidden layer are activated by a sigmoid (logistic) function, while the neurons in the output layer use linear activation function. Linear activation function at the output is of crucial importance for the implementa-

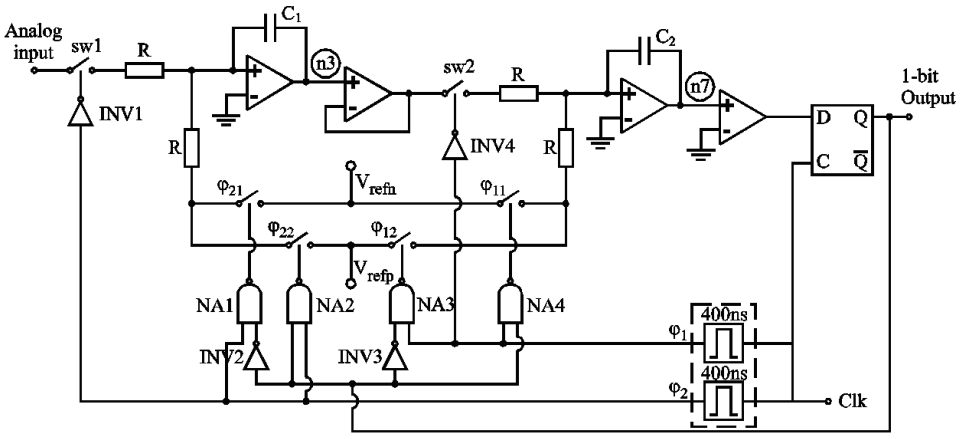

Fig. 2 *Sigma-delta modulator structure.*

tion of the method since the response value of the output neuron is limited by the number of faults conceived to be diagnosed only. The learning algorithm used for training this network is a version of the steepest-descent minimization algorithm [20]. We consider this proceeding mostly as a contribution to the implementation of ANNs and less as a contribution to the ANN theory. Accordingly, less attention will be paid to the latter, and links to the literature will be given.

4. Fault Dictionary Creation and Application Example

In order to describe the way in which the fault dictionary was created, the sigma-delta modulator circuit depicted in Fig. 2 was used. It is a mixed-signal system with representative functional complexity having analogue, digital, and switching elements. The switches in the circuit are modeled as truly ideal, exhibiting zero and infinite resistance for closed and open state, respectively.

The integrator charging time is invariable with respect to clock rate in order to keep the gain constant. This means that the analogue switch must be turned on for fixed time duration regardless of clock rate. This is achieved by using monostable multivibrator as a fixed-width pulse generator in the circuit. The monostable multivibrator between the clock-input and switch-control block operates as a pulse generator to produce control signals of fixed time duration.

In this paper, we consider defects in the whole circuit, meaning in analogue, digital, and the switching part. We do not intend to diagnose multiple faults.

There are two types of defects in the digital part of the system observed: catastrophic (stuck-at) and delay faults (delays of rising and falling edge of digital signals).

In the system of Fig. 2, the analogue switches are controlled by digital signals, so there are pairs with the same fault effects, i.e. the effect is the same when the switch

is stuck at ON (OFF) and when the logic circuit's output is "stuck-at-1" ("stuck-at-0"). So, we will consider hard faults (that are associated with the analogue part of the circuit) as stucked switches [21].

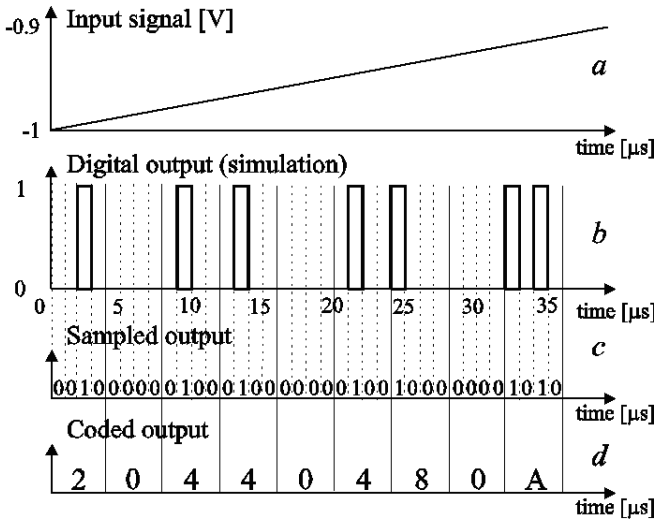

Fig. 3 *Fault dictionary creation – response of the fault-free system.*

Having in mind that the clock period in the system is 1.2 μs (half period is 600 ns), we examined effects of delays not greater than 400 ns. In fact, effects of rising edge delay are simulated for delay values of: 100 ns, 250 ns, 400 ns, while for the falling edge, we inserted smaller values: 50 ns, 100 ns, 150 ns. The goal was to determine the mapping of the delay faults onto the output digital signal. All digital gates were examined (4 inverters and 4 nand circuits). Simulations were performed using Alecsis simulator [22]. The first conclusion was that delays in the circuit of inverter 2 (INV2, Fig. 2) do not influence output signal, meaning that the output was not changed.

The fault dictionaries for both analogue and digital part of the system were created using the response of the circuit to an input ramp signal (Fig. 3*a*). The system output value was registered after every clock period (Fig. 3*b*), so these output digital values form the output signature (Fig. 3*c*). These are then represented in more compact hexadecimal form (Fig. 3*d*). As an illustration, part of the fault dictionary for the digital part of the system is created, as shown in Tab. I.

The defect type coding in the Tab. I refers to the notation given in Fig. 2. For example, *na1*(*tf*=100ns) stands for the falling-edge delay of NAND1 being 100 ns, *na3*(*tr*=250ns) stands for the rising-edge delay of NAND4 being 250 ns, *φ12OFF* is coding the switch φ12 stuck-at OFF, while *sw2OFF* is coding the switch sw2 stuck-at OFF. FF stands for the fault free circuit.

The degree of accuracy to which faults can be located is called diagnostic resolution. There exist groups of delay values causing the same fault-effect. Such groups are referred to as ambiguity groups or the groups of functionally equivalent faults (FEF). No external testing can distinguish among FEF. The partition of all

Defect code	*Defect type*	*Signature*
0	FF	20440480A
2	inv1(tr=150ns)	000010010
5	na1(tf=100ns)	008000010
8	na3(tf=50ns)	104108210
15	inv3(tr=100ns)	202404410
22	φ_{11}OFF	001C00038
24	sw2ON	018018030
27	na3(tr=250ns)	021041084
30	na3(tf=100ns)	082202208
33	sw2OFF	996696699
36	inv1(tr=50ns)	040810108
42	φ12OFF	300038003
45	na4(tf=150ns)	802408811

Tab. I *Part of the fault dictionary for the digital part of the circuit.*

faults into distinct subsets of FEF defines the maximal fault resolution. A test that achieves the maximal fault resolution is said to be a complete fault-location test.

As for the subset of faults belonging to the digital part of the system FEF, these are listed in Tab. II. The first four FEFs show cases where delay increments in different circuits cause the same effect at the system output, i.e., the same delay.

In the second column of the Tab. II, groups of defects giving rise to the same effects are listed, and accordingly, the third column presents that common fault-effect (signature). The fifth ambiguity group is in a way different. The members of that group are both catastrophic and delay faults. Note that only one representative of each ambiguity group is introduced in the fault dictionary, Tab. I.

In the analogue part of the system, we have considered both parametric and catastrophic defects [23], [24]. As parametric faults we considered variations of resistance and capacitance values. The capacitances of both capacitors are changed. The first stage of the system is more sensitive to parameter variations, while the changes in the second stage have reduced effect on the performance, due to noise shaping. That is best seen when the fault effect of the capacitance in the first stage is observed. However, changes of capacitance in the second stage cause exactly the same effect as the fault free circuit.

Catastrophic (hard) faults in an analogue system change the circuit topology. In order to illustrate this, we have observed the situation when the feed-back capacitor of the operational amplifier is disconnected, and also the situation when there is an open circuit at the operational amplifier's output (in the example given here, the output of the third operational amplifier-OA3 is disconnected, node $n7$ in Fig. 2). Part of the fault dictionary for the analogue part of the system is created, as shown in Tab. III, where defect code 0 denotes the fault-free system as it does in Tab. I.

The fault coding (column 1 in Tabs. I and III) is an important issue. In fact, some defects exhibit very similar effects at the circuit output. So, input data (signatures) to the diagnostic system can have very close numerical values. Consequently,

Ambiguity group	*Defect type*	*Signature*
1	na3(tf=50ns)	104108210
	na4(tr=250ns)	
2	na3(tr=400ns)	102104208
	na4(tr=400ns)	
3	na4(tf=100ns)	404210240
	inv3(tf=100ns)	
4	FF	20440480A
	inv2(tr=50ns)	
	inv2(tr=100ns)	
	inv2(tr=150ns)	
	inv2(tf=50ns)	
	inv2(tf=100ns)	
	inv2(tf=150ns)	
5	φ21OFF	000000000
	na1(tf=150ns)	
	sw1ON	

Tab. II *Functionally equivalent faults.*

Defect code	*Defect type*	*Signature*
0	FF	20440480A
1	C1 disconnected	E38E38E38
3	0.8*C1	102204210
6	1.2*R1	822211110
10	0.8*R4	804809011
12	OA3 output disconnected	805005012

Tab. III *Part of the fault dictionary for the analog part of the circuit.*

if the output values (defect codes) were also similar, difficulties may arise during the network training. Faults are coded randomly, so that faults with similar effects are unlikely to have similar codes. This approach is proven to be good, because the way of coding influences the training time and error.

The second column of Tabs. I and III describes the type of the defect. The third column contains the signature seen at the output. Note that, for obtaining the nine-digit hexadecimal number coding the binary output, one had to get 36 samples of the output waveform.

5. Synthesis of a Hierarchical Diagnostic System

A two level hierarchical system is depicted in Fig. 4. The idea is to look at: the system and the subsystem (or circuit or component) level. Accordingly, one diagnostic system is to be created at the topmost level the task of which is to

locate the faulty subsystem (component) and to deliver enough information (fault code and, possibly, type of hypothesis) to the lower diagnostic level to locate the fault within the subsystem (component). For that, of course, one needs as many diagnostic subsystems at the subsystem level as many circuits are conceived within the system. Generally, such subsystems in the analogue part may be operational amplifiers, circuits built of passive components and operational amplifiers (filters, for example) etc. while in the digital part one meets basic logic gates, flip/flops or even registers and memory blocks. It is assumed that fault dictionaries and corresponding ANNs for diagnostic purposes are at the disposal and incorporated into the diagnostic software at the time of diagnosis of the whole system.

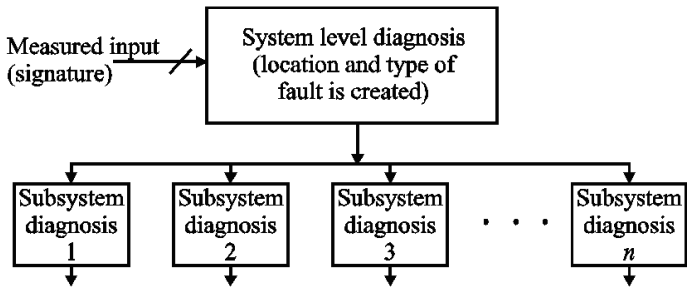

Fig. 4 *A two level hierarchical system.*

At the system level, the modular approach was implemented first, making the search for the diagnostic statement easier. The digital and analogue part of the system were considered as modules, and two artificial neural networks were trained for capturing the look-up tables, one for diagnosis in the digital part, and another for diagnosis in the analogue part of the system. Note, the partition is natural from the point of view of creation of fault dictionaries being obtained by simulation successively: firstly, for the digital and later for the analogue part. Both networks are feed-forward with one hidden layer. The signatures are inputs to the ANNs, and the fault code is ANN's output to be learned. It means that both neural networks have 9 inputs (one input per hexadecimal digit) and one output terminal. After learning was completed, the number of hidden neurons in the resulting ANN was 10 (Fig. 5), for the network implementing the fault dictionary related to the digital part, and 3, for another, what was found by trial and error after several iterations starting with an estimation based on [25].

The effectiveness of the training process of the obtained ANNs was verified by exciting the ANNs with faulty inputs. Responses of the ANNs show that there were no errors in identifying the faults, which is partly presented in Tab. IV, where results for the defects listed in Tab. I are shown. Only negligible discrepancies may be observed.

To mention again, two groups of faults were considered in order to reduce the number of faults per ANN, thus enabling easier learning and reduced complexity of the ANNs. Now, the task is to have a complete diagnosis at system level responding to every signature. The practical implementation of the concept of Fig. 1 is depicted

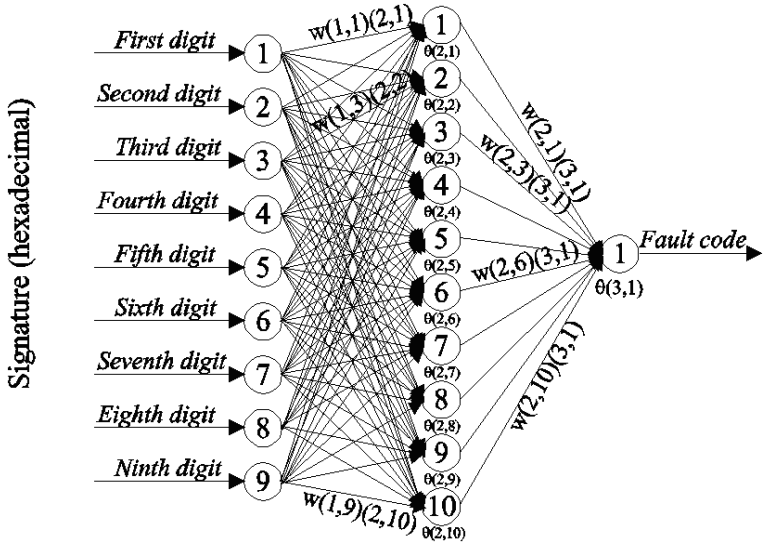

Fig. 5 *The structure of one of the diagnostic ANNs.*

Defect type	***Defect code***	***ANN output***
FF	0	-0.000215
inv1(tr=150ns)	2	1.99969
na1(tf=100ns)	5	4.99988
na3(tf=50ns)	8	7.99998
inv3(tr=100ns)	15	15
φ_{11}OFF	22	22
sw2ON	24	23.9997
na3(tr=250ns)	27	27
na3(tf=100ns)	30	30
sw2OFF	33	33.0021
inv1(tr=50ns)	36	36
φ12OFF	42	41.9996
na4(tf=150ns)	45	44.9996

Tab. IV *ANN output results.*

in Fig. 6. *ANN1* diagnoses defects in the digital part of the system and fault codes are in the range from 0 to 45. *ANN2* diagnoses defects in the analogue part of the system and fault codes are in the range from 0 to 12. We can notice that we use numbers starting from 0 in both cases in order to denote fault codes. With that notation, when both diagnostic ANNs work in parallel, one cannot distinguish whether the fault code refers to analogue or digital defect. So, we provided *ANN3* in order to help distinguishing if certain defect is digital or analogue.

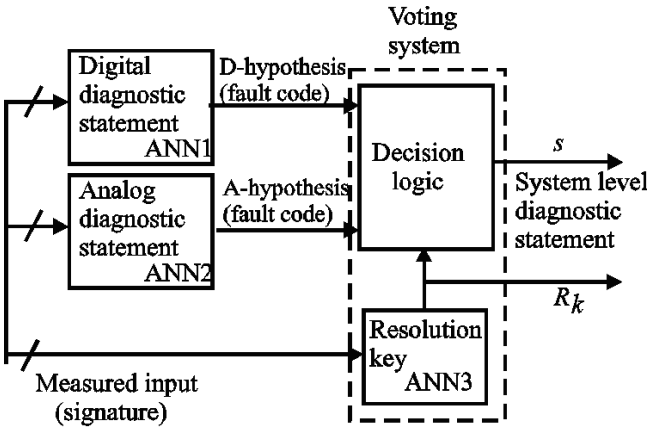

Fig. 6 *The ANN based hierarchical diagnostic system.*

ANN3 also has 9 inputs and it gets the measured signature as an input as *ANN1* and *ANN2* do. It gets trained so that its output code takes values from the set $\{-1, 0, 1\}$. We refer to these values as resolution key. Namely, if the defect comes from the digital part, the output code is set to 1, while if it comes from the analogue, the output code is set to -1. In the special cases when ambiguity arises, that is when one has the same signature coming from faults belonging to the digital and analogue part, we assign 0 to the output of *ANN3.* We will give a few examples now, in order to illustrate the previous explanation.

Suppose that we excite our ANNs with the input signature: {0 8 2 2 0 2 2 0 8}. The responses of the three networks are as follows:
ANN1 response: 30
ANN2 response: -0.0800663
ANN3 response: 0.99934. The resolution key is 1.
The decision logic (Fig. 6) decides that we have digital defect (because the *ANN3* output value is approximately 1), and its code is 30 (because the *ANN1* output value is 30). *ANN2* response is ignored.
Next, we suppose that we excite our diagnostic system with the input signature: { 8 0 4 4 1 0 4 2 1 }. The responses of the three networks are as follows:
ANN1 response: 29.0138
ANN2 response: 4.00001
ANN3 response: -1.00066. The resolution key is -1.
The conclusion is that we have analogue defect (because the *ANN3* output value is approximately -1) and its fault code is 4 (because the *ANN2* output value is 4). *ANN1* response is ignored.
Finally, we suppose that we excite our 3 ANNs with the input signature: { 1 0 4 1 0 8 2 1 0 }. The responses of the three networks are as follows:
ANN1 response: 7.99998
ANN2 response: 11
ANN3 response: -0.00172622. The resolution key is 0.

We consider now both *ANN1* and *ANN2* responses because the response of *ANN3* is approximately 0, indicating ambiguity. The conclusion is that we have analogue defect with fault code 11, or digital defect coded with 8. We cannot decide which one of them really happened in the system because they have exactly the same response, and this is a problem that may be resolved by increasing the number of sampling intervals or by introducing additional signals for fault dictionary creation. That will not be discussed here anymore.

6. Hierarchy Application

The diagnostic statement obtained so far at the system level, may be handed down to, say, a component level where the final diagnostic act may be performed. To do that one needs to perform diagnosis for the subsystems. In the A/D converter depicted in Fig. 2 the role of the subsystems may be played by the digital gates and operational amplifiers.

Identical process of fault dictionary creation and ANN synthesis is expected to be done for every single subsystem in order to perform diagnosis at the lower level. An example of such a solution for an operational amplifier is given in [6] and will be used here for illustration of the rest of the diagnostic process.

Earlier in this paper, we took into consideration a defect within the operational amplifier OA3, in the analogue part of the system of Fig. 2, diagnosed by *ANN2*. It is the defect coded by 12: "*OA3 output disconnected*". Let that be the result of diagnosis at the system level: the location and the fault-code related to that location. The structure of this operational amplifier is shown in Fig. 7.

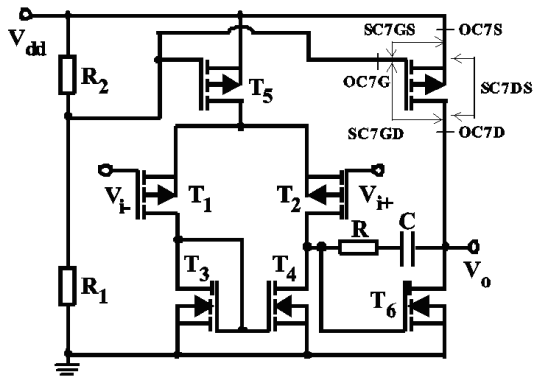

Fig. 7 *Operational amplifier structure.*

At the lower level, after searching the fault dictionary of OA3, being created separately for this subsystem as described in [6] (we here skip all redundant explanations and data already published), we come to a final conclusion: the fault affecting the output of the whole system is that the drain of transistor T6 is disconnected.

Similar activities may be performed for every other fault that is diagnosed at the topmost level to belong to a fault located within one of the subsystems.

To summarize, in Tab. V, we present the complete algorithm representing the activity-flow for a diagnostic system to be developed and implemented. It is well known that complex approximation activities are implemented whenever new ANN is created. That involves initial solution and convergence problem solving, not to mention handling of local minima. All that, however, was already discussed by many authors and will not be elaborated here.

A. *Fault dictionary creation phase* ***at the subsystem level.*** This activity is to be performed once for a given technology and the results are kept as intellectual property (i.e. library).

For every subsystem{

Choose a signal(s) expected to activate all the faults from the fault list (of length m);

For j=1,m (i.e. all the faults from the fault list) {

Create a signature by simulation of the faulty subsystem;

Create a random number k_j with uniform distribution such that $1 \leq k_j \leq m$, and $k_j \neq k_l$, $l = 1, 2, ..., j-1$. This will be considered fault-code.

Add the fault-code and signature to the fault dictionary.

}

Perform ANN training to memorize the local fault dictionary. This includes not only determination of the numerical values of the weights and thresholds but the complexity of the ANN, too.}

B. *Fault dictionary creation phase* ***at the system level***

Choose a signal(s) expected to activate all the faults from the fault list (of length r);

For j=1,r (i.e. all the faults from the fault list) {

Create a signature by simulation of the faulty system;

Create a random number k_j with uniform distribution such that $1 \leq k_j \leq r$, and $k_j \neq k_l$, $l = 1, 2, ..., j-1$. This will be considered fault-code.

Add the fault code and signature to the fault dictionary.

}

Perform ANN training to memorize the system's fault dictionary.

C. ***Diagnosis***

Create signature by processing the measured response of the faulty system.

Run the appropriate ANN to get the diagnostic statement at the system level.

Run the appropriate ANN to get the diagnostic statement at subsystem level

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Tab. V *Activity-flow of a diagnostic system.*

7. Conclusion

Feed-forward artificial neural networks, being universal approximators, have been successfully applied to the diagnosis of mixed-mode electronic circuit containing analogue, digital and a part with internally controlled switches. In order to tackle the complexity of a circuit, hierarchical approach to the diagnostic statement generation was applied.

The simulation before test approach was implemented in order to prepare data for diagnosis. The simulation results were captured within a fault dictionary. Here, a list of all conceivable faults is supposed to be given. To avoid difficulties in decision-making at the topmost level, when measurement results are to be compared with the ones previously stored, the dictionary was separated in two groups. One was related to the faults in the analog part of the circuit while the other was related to the rest of the faults. In general, there should not be restrictions on the number of partitions that may be used for diagnosis at any level. In addition, one can introduce as many levels of diagnosis as necessary.

The number of test points, which is very important from the measurement point of view, was reduced to the input and output terminals only. That allows for simplified testing procedures when automatic testing or diagnostic equipments are applied. No limitation on the fault types was imposed. That means stuck-at and delay faults were considered within the digital part, while parametric and catastrophic faults were allowed to happen in the analogue. The switches were also allowed to get stuck-at states. Special attention was paid to the faults related to the A/D and D/A interfaces within the circuit.

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