DESIGN AUTOMATION CONFERENCE

# CALL FOR CONTRIBUTIONS

DAC continues to be the premier conference devoted to Electronic Design Automation (EDA) and the application of EDA tools in designing advanced electronic systems. DAC 2011 is seeking submissions that deal with tools, algorithms, and design technologies for all aspects of electronic circuit, system, and embedded design. All submissions must be made electronically through the DAC website.

**New in 2011:** In addition to submissions in core and emerging EDA topics, DAC invites submissions in embedded systems and software topics outlined in a separate Call for Papers. DAC also invites work-in-progress (WIP) submissions that will be presented at DAC through interactive poster sessions. Finally, DAC solicits submissions in focus cross-cutting topics that include low-power, 3-D, and reliability.

DAC invites **submissions** in the following categories:

- Research Papers
- Embedded Systems and Software Papers (new)
- "Work-in-Progress" (WIP) Abstracts (new)
- User Track Extended Abstracts
- "Wild and Crazy Ideas" (WACI) short papers
- Special Session Proposals
- Panel Proposals
- Workshop Proposals
- Proposal for Colocated Events
- Student Design Contest

## June 5-10, 2011
## San Diego, California

Sponsored by:

SIGDA · EDA CONSORTIUM · CEDA IEEE Council on Electronic Design Automation

In technical cooperation with:

SSCS

**WWW.DAC.COM**

# RESEARCH PAPERS

**DUE BEFORE 5:00pm MT, November 18, 2010**

All research paper submissions MUST adhere to the following rules:

1. be in PDF format only
2. contain an abstract of approximately 60 words clearly stating the significant contribution, impact, and results of the submission
3. must not exceed six pages (including the abstract, figures, tables, and references), double-columned, 9-pt or 10-pt font
4. MUST NOT identify the author(s) by their name(s) or affiliation(s) anywhere on the manuscript or abstract, with all references to the author(s)'s own previous work or affiliations in the bibliographic citations being in the third person.
5. list all authors and their affiliations in the web-based submission form (i.e., not in the paper); the addition of new authors to an accepted paper will not be permitted.

DAC papers go through a double-blind review process; i.e., the identity of authors and reviewers is only known to the TPC co-chairs. DAC ensures that there are no conflicts of interest between authors and reviewers. DAC will compare each submission against a vast database and any paper with significant similarity to previously published works or with papers that are simultaneously under review with other venues with archival publications (e.g., conferences, symposia, journals, and workshops with archival proceedings), will be rejected. Submissions not adhering to these rules will be rejected.

Format templates are available on the DAC website. All research papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage. Acceptance notices will be available by logging in to the DAC website after Feb. 4, 2011. Complete instructions for final paper submission and required release forms will be available on the DAC website by March 7, 2011. Authors of accepted papers must sign and submit a copyright release form for their paper. All conference presenters will be required to register at the time of final paper submission, present their paper and participate in a research poster session.

ACM and IEEE reserve the right to exclude a paper from archival distribution after the conference if the paper is not presented by one of the co-authors at the conference, or in other exceptional cases. DAC will support the IEEE Prohibited Authors List.

Select authors of submitted DAC papers that are not accepted for publication in 2011 will be invited in mid-February 2011 to participate in "Work-In-Progress" (WIP) poster sessions. They will be asked to submit a 100 word abstract to publish on the website (and not in the proceedings). Authors will also be given the option to post their poster presentation on dac.com.

## SUBMISSION CATEGORIES FOR RESEARCH PAPERS

Authors of research papers are required to specify a category from the list below. Authors of submissions that cover cross-cutting topics (e.g. low-power, reliability, 3-D, etc.) should select a category that is closest to the essential contribution of the submission. Authors may choose a second submission category to accommodate cross-cutting contributions. Please note the separate call for submissions for embedded systems and software.

**R1. System-on-Chip (SOC) Platforms and Applications**

R1.1 Application-specific platforms
R1.2 Virtual and hardware prototyping
R1.3 Flows and methods for specific applications and design domains
R1.4 Solutions for managing SOC constraints: reliability, power, security, etc.
R1.5 Custom memory and storage
R1.6 SOC design case studies

**R2. System-Level Design and Codesign**

R2.1 System specification, modeling, simulation, verification, and performance analysis
R2.2 Scheduling, HW/SW partitioning, HW/SW interface synthesis
R2.3 IP and platform-based design
R2.4 Security and IP protection
R2.5 Design of Multiprocessor System-On-Chip (MPSOC)
R2.6 Application-specific processor design tools

**R3. System-Level Communication and Networks-On-Chip**

R3.1 Modeling and performance analysis
R3.2 Communications-based design, communication and network synthesis
R3.3 Optimization for energy, fault tolerance, reliability
R3.4 Interfacing and software issues, beyond-the-die communication
R3.5 NOC design methodologies, case studies and prototyping

**R4. Power Analysis and Low-Power Design**

R4.1 System-level power design and thermal management
R4.2 System/Architectural low-power techniques: partitioning, scheduling, and resource management
R4.3 High-level power estimation and optimization
R4.4 Gate-level power analysis and optimization
R4.5 Device and circuit techniques for low-power design
R4.6 Power-aware and energy-efficient wireless protocols, algorithms and design techniques

**R5. Verification**
R5.1 Functional, transaction-level, RTL, and gate-level modeling and verification of hardware design
R5.2 Dynamic simulation, equivalence checking, formal (and semiformal) verification model and property checking
R5.3 Emulation and hardware simulators or accelerator engines
R5.4 Modeling languages and related formalisms, verification plan development and implementation
R5.5 Assertion-based verification, coverage analysis, constrained random testbench generation
R5.6 Verification techniques for software correctness

**R6. High-Level Synthesis, Logic Synthesis and Circuit Optimization**
R6.1 Combinational, sequential and asynchronous logic synthesis
R6.2 Library mapping, cell-based design and optimization
R6.3 Transistor and gate sizing, resynthesis
R6.4 Interactions between logic design and layout or physical synthesis
R6.5 High-level, behavioral, algorithmic, and architectural synthesis, “C” to gates tools and methods
R6.6 Resource scheduling, allocation, and synthesis

**R7. Circuit, Interconnect and Manufacturing Simulation and Analysis**
R7.1 Electrical, thermal, and electro-thermal simulation
R7.2 Model order reduction methods
R7.3 Interconnect and substrate modeling and extraction
R7.4 High-frequency and electromagnetic simulation of circuits
R7.5 Process technology characterization, and modeling
R7.6 Technology CAD and fab automation

**R8. Timing Analysis, Integrity and Design Reliability**
R8.1 Deterministic and statistical timing analysis
R8.2 Signal integrity and substrate noise
R8.3 Power delivery analysis and optimization
R8.4 Electrical and thermal reliability
R8.5 Soft errors
R8.6 Novel clocking methodologies

**R9. Physical Design and Manufacturability**
R9.1 Floorplanning, partitioning, placement
R9.2 Buffer insertion, routing, interconnect planning
R9.3 Physical verification and design rule checking
R9.4 Automated synthesis of clock networks
R9.5 Reticle enhancement, lithography-related design optimizations
R9.6 Design for manufacturability, yield, defect tolerance, cost issues, and DFM impact
R9.7 Physical design of 3-D integrated circuits
R9.8 System-in-package design, package-board codesign
R9.9 Design for resilience under manufacturing variations

**R10. Analog, Mixed-Signal, and RF**
R10.1 Analog, mixed-signal, and RF design methodologies
R10.2 Automated synthesis
R10.3 Analog, mixed-signal, and RF simulation
R10.4 High-frequency design and advanced antenna design for wireless design

**R11. FPGA Design Tools and Applications**
R11.1 Rapid prototyping
R11.2 Logic synthesis and physical design techniques for FPGAs
R11.3 Configurable and reconfigurable computing

**R12. Testing**
R12.1 Test quality/reliability, current based test, delay test, low-power test
R12.2 Digital fault modeling, automatic test generation, fault simulation
R12.3 Digital design for test, test data compression, built-in self test
R12.4 Memory test and repair, FPGA testing
R12.5 Fault-tolerance and online testing
R12.6 Analog/mixed-signal/RF testing, system-in-package (SIP) testing
R12.7 Board- and system-level test, system-on-chip (SOC) testing
R12.8 Silicon debug and diagnosis, post-silicon design validation

**R13. Design Automation for Synthetic Biology**
R13.1 Design methodologies for synthetic biology
R13.2 Tools for engineering parts and devices
R13.3 Tools for protein and pathway engineering
R13.4 Tools for bridging experimental and computational frameworks

**R14. New and Emerging Design Technologies (including but not restricted to)**
R14.1 New transistor structures, devices, and novel process technologies
R14.2 Nanotechnologies, nanowires, nanotubes
R14.3 Optical devices and communication
R14.4 Quantum computing
R14.5 Biologically-based or biologically-inspired computing systems
R14.6 MEMS, sensors, actuators, imaging devices
R14.7 Cyber-physical systems

**ALL SUBMISSIONS MUST BE MADE ELECTRONICALLY AT** : http://www.dac.com
ACM and IEEE reserve the right to exclude a paper from archival distribution after the conference if the paper is not presented by one of the co-authors at the conference, or in other exceptional cases. DAC will support the IEEE Prohibited Authors List.

# Embedded Systems and Software (ESS)

**Submission site opens October 22, 2010**

**DUE BEFORE 5:00pm MT, November 18, 2010**

New for this year is the focus topic on Embedded Systems and Software (ESS). Authors of Research Papers on all aspects of Embedded Systems and Software are encouraged to submit to this focus call. A submission to this topic must specify a category from the list below. Authors may choose a second submission category (both from the regular research topics as well as from the focus embedded topics) to accommodate cross-cutting contributions. All Embedded Systems and Software paper submissions must adhere to the same rules outlined for the Research Papers. (http://www2.dac.com/48th+call+for+contributions.aspx)

Select authors of submitted DAC Embedded Systems and Software papers that are not accepted for publication in 2011 will be invited in mid-February 2011 to participate in "Work-In-Progress" (WIP) poster sessions. They will be asked to submit a 100-word summary to publish on the website (and not in the proceedings). Authors will also be given the option to post their poster presentation on dac.com.

**E1. Embedded System Specification and Software Engineering**

E1.1 Domain-specific programming languages
E1.2 Software architectures and software engineering
E1.3 Model- and component-based embedded software design
E1.4 Software frameworks
E1.5 Hardware/software co-specification

**E2. Embedded Software and Tools**

E2.1 Real-time operating systems and middleware
E2.2 Virtual machines
E2.3 Hardware/software co-design
E2.4 Software for multicore, GPU, and novel embedded architectures
E2.5 Retargetable compilation for embedded architectures
E2.6 Worst-case execution time analysis
E2.7 Hardware-dependent software
E2.8 Customized interfaces and protocols
E2.9 Tools for managing embedded I/O: device drivers, timers, etc.

**E3. Architectures for Embedded Systems**

E3.1 Many- and multi-core embedded architectures
E3.2 Application-specific embedded processor (ASIP) design and tools
E3.3 Run-time and design time reconfigurable processors
E3.4 On-chip memory architectures and management: scratchpads, compiler controlled memories, etc.
E3.5 Custom storage organizations: flash, etc.
E3.6 Custom communication design

**E4. Embedded System Validation, Verification, Security**

E4.1 Formal verification
E4.2 System validation
E4.3 Testing and regression analysis
E4.4 Hardware/software co-validation
E4.5 Hardware and software security

**E5. Embedded Systems Platforms, Design Methodologies and Case Studies**

E5.1 Platforms for domain-specific applications (e.g., avionics, automotive, medical, mobile, multimedia, etc.)
E5.2 IP-based design
E5.3 Rapid prototyping
E5.4 Packaging issues
E5.5 Design methodologies and design flows
E5.6 Case studies

**E6. Design Space Exploration and Optimization**

E6.1 Modeling embedded constraints: reliability, power, security, etc.
E6.2 Early estimation and co-simulation
E6.3 Multiple-constraint-driven embedded system synthesis and optimization
E6.4 Distributed embedded systems, end-to-end QoS management, performance analysis

## "WORK-IN-PROGRESS" (WIP) ABSTRACTS

**Authors are invited to submit a one-page abstract.**
**DUE BEFORE 5:00pm MT, March 1, 2011**

In contrast to other tracks at DAC, this track aims to provide authors an opportunity for early feedback on work-in-progress or to share early results. A WIP submission must be one page in length, in PDF format, and clearly specify a technical problem, outline a solution, and provide some early results. WIP submissions will be accepted for presentation at a poster session. A WIP submission will not be included in the DAC proceedings. The 100-word summary abstract will be published on the website. A WIP presentation at DAC is not considered a DAC publication. WIP submissions will be reviewed by the Technical Program Committee and expert external reviewers, but no specific feedback will be provided. Acceptance notices will be available by logging in to the DAC website after April 8, 2011. The 100-word summary abstract will be placed on the dac.com website once the submission is accepted. WIP authors are at liberty to submit an extended version of their work to other conferences and to journals without violating common codes of ethics.

Some authors of submitted DAC research and embedded systems and software papers that are not accepted for publication in 2011 will be given "WIP pre-selected" status. These authors will be invited in mid-February 2011 to participate in the WIP poster sessions. The authors will be asked to submit a 100-word summary abstract to be published on the website (and not in the proceedings). WIP submissions received by the WIP deadline are expected to be competitive with the WIP pre-selected submissions. The number of planned poster sessions will be commensurate with the quality of WIP submissions.

## WILD AND CRAZY IDEAS (WACI) PAPERS

**DUE BEFORE 5:00pm MT, November 18, 2010**

DAC invites submissions with genuinely forward-looking, radical, and innovative ideas in the area of electronic design or electronic design automation. The WACI sessions feature novel (and even preliminary or unproven) technical ideas. The aim of WACI is to promote revolutionary and way-out ideas that do not fit the conventional mold, that inspire discussion among conference attendees, that create a buzz, and that get people talking. Research that incrementally improves on prior work is not suited for this category.

Submissions to the "Wild and Crazy Ideas" track must not exceed two pages, but must otherwise follow the above rules and deadlines for the research papers. Unlike a DAC research paper that explores a specific technology problem and proposes a complete solution to it, with extensive experimental results, a WACI paper could present less developed but highly innovative ideas related to areas relevant to DAC. All WACI accepted papers will be required to post a two-minute video describing the work as part of the acceptance process. DAC 2010 WACI videos may be seen at http://www2.dac.com/waci+videos.aspx.

## USER TRACK PAPERS EXTENDED ABSTRACTS

**DUE BEFORE 5:00pm MT, January 18, 2011**

DAC's User Track addresses the real-life issues facing IC designers, application engineers, and design flow developers. It provides valuable insights and experiences with in-house or commercial EDA tool flows. User Track papers may describe the application of EDA tools to the design of a novel electronic system, or the integration of EDA tools within a design flow or methodology to produce such systems. A User Track paper may be problem-specific in scope (e.g., analyzing substrate coupling during floorplanning) or may address a specific application domain (e.g., designing wireless handsets). Initial submissions are in the form of a two-page extended abstract. Final submissions will be in the form of a PowerPoint presentation. User Track authors will not be required to sign a copyright release form as final submissions will not be published. For more details, please see the separate User Track Call for Papers on the DAC website.

## SPECIAL SESSION PROPOSALS

**DUE BEFORE 5:00pm MT, October 19, 2010**

Special session proposals must include descriptions of the proposed papers and speakers, and the importance of the special session to the DAC audience. A special session is devoted to a topic of strong contemporary or future interest. The topic must represent an emerging area that does not yet receive sufficient focus from research papers. A submission must list at least three inspiring speakers who address the topic from different angles. DAC reserves the right to restructure all special session proposals. Particular topics of interest this year include, but are not limited to, spintronics, topological insulators for interconnect, bio-design automation, and embedded systems and software. For early feedback on a proposal topic, please contact the program co-chairs.

## PANEL and TUTORIAL PROPOSALS

**PANEL PROPOSALS DUE BEFORE 5:00pm MT, October 19, 2010**
**TUTORIAL PROPOSALS DUE BEFORE 5:00pm MT. November 1, 2010**

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure all panel and tutorial suggestions.

## COLOCATED EVENT PROPOSALS

**DUE BEFORE 5:00pm MT, January 20, 2011**

DAC invites you to colocate your conference, meeting or other special event with DAC. We will provide you with meeting rooms at the conference center at no cost. Your event will be financed and otherwise organized by you.

## WORKSHOP PROPOSALS

**DUE BEFORE 5:00pm MT, January 20, 2011**

DAC invites you to organize a workshop on topics related to design, design methodologies, and design automation. DAC provides the financial and organizational support, including attendee registration, rooms at the conference center and audio visual equipment.

## STUDENT DESIGN CONTEST SUBMISSIONS

**DUE BEFORE 5:00pm MT, November 24, 2010**

ISSCC and DAC will jointly sponsor the 2011 ISSCC/DAC Student Design Contest. The contest promotes excellence in the design of electronic systems within an academic environment and provides a forum in which undergraduate/graduate students' ingenuity can be shared with an audience of academic/industrial technical experts. The winners will present their designs through a poster at ISSCC 2011 and DAC 2011. Designs can be for analog, digital, MEMS, optics, biological, or programmable circuits and embedded systems/platforms in any of the three categories: operational, system-level, or conceptual.