53 DESIGN AUTOMATION CONFERENCE

CONFERENCE PROGRAM & EXHIBITS GUIDE

JUNE 5-9, 2016 | AUSTIN, TX

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GENERAL CHAIR'S WELCOME

Dear Colleagues,

I am delighted to welcome you to Austin, Texas, home of the 53rd Design Automation Conference. Austin also happens to be my home for the past 20 years. In that time, I have watched the city, known to many as Silicon Hills, grow into a technology powerhouse. Austin is famous for being weird, but with the arrival of the 53rd Design Automation Conference, it is now nerdy as well. Over the past year we have introduced the "Keep Austin Nerdy" theme for the 53rd DAC and hope to continue this trend for years to come.

Monday evening brings a new addition to the conference: the first DAC Silicon/Technology Art Show. The Art Show will highlight the beauty of electronic design and algorithms and showcase the works of companies and individuals that contribute to our industry. I encourage you to attend the Art Show/evening reception on Monday night starting at 6:00pm.

With the help of hundreds of volunteers, the DAC executive committee has assembled a fantastic technical program, featuring sessions on hardware and software security, automotive, IoT, design, EDA algorithms, IP, and embedded software and systems.

I am especially proud of the direction the Design/IP Track has taken this year with over 27 sessions consisting of over 127 presentations taking place over three days. This is more than double the content that this track had three years ago, the last time DAC was in Austin. This Design/IP Track is THE place for the design community to connect with each other and share their best practices. On Monday-Wednesday, the Design/IP Track concludes at 5:00 each day with a happy hour/poster session on the show floor.

Highlighting the diversity of our program are the outstanding Keynotes taking place each morning of the conference spanning from Automotive to Robotics. Lars Reger from NXP kicks things off on Monday and will tie our EDA industry to the burgeoning space of automotive electronics. On Tuesday, Sameer Halepete from NVIDIA explains the design and applications of complex graphics chips. Wednesday, Mark Papermaster CTO from AMD (and former silicon design chief for Apple and IBM) explains his secrets for making truly great products.

Finally, this all star lineup concludes on Thursday with UT-Austin researcher Peter Stone explaining how machine learning has helped him construct the world's top soccer robot team.

New at DAC this year will be Research Grove and the Grove Lounge, where I invite those of you attending the technical sessions to stop by the Grove to sit and relax after a day of sessions. The "Grove" enables those attending the research conference program a place to get some refreshments and network with their colleagues.

As we all know, much of the action and excitement happens on the exhibition floor. This year, DAC is pleased to host over 175 exhibitors who are an integral part of the conference ecosystem. In addition to the vendors the DAC exhibition floor offers the following for all attendees to enjoy:

- World of IoT Exhibit featuring the IP Pavilion, the Embedded Pavilion and the Maker's Market
- NXP IoT truck, showcasing devices that the industry enables
- NXP US Finals Racecar Challenge
- Food Trucks featuring local cuisine
- The DAC Pavilion which each day includes a SKY Talk, an Austin Angle Talk, an unscripted interview with an EDA CEO, an industry analyst review and a teardown.

While the show floor closes on Wednesday afternoon, stick around on Thursday for revamped training day. As in previous years, Duolos brings forth first class designer training. This year we are also offering training in advanced C++ and executive management, sponsored by the McCombs School of Business.

With so much going on at the show, how do you keep track of all the sessions and activities at DAC? I encourage you to download the mobile app! It is the best way I can recommend you manage your schedule and activities at the show plus by playing the DAC Attack app game you can win cool prizes.

Enjoy the show!

#53DAC

Charles J. Alpert
General Chair, 53rd DAC




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CONFERENCE SPONSORS

ACM/SIGDA

ACM is the world's largest computing society and brings together computing educators, researchers and professionals to inspire dialogue, share resources and address the field's challenge. The ACM Special Interest Group on Design Automation has a long history of supporting conferences and the EDA profession. In addition to sponsoring DAC, SIGDA sponsors ICCAD, DATE, and ASP-DAC, plus approximately 15 other symposia and workshops. SIGDA provides a broad array of additional resources to our members, to students and professors, and to the EDA profession in general. SIGDA organizes the University Research Demo and Ph.D. Forum at DAC, and the CADathlon at ICCAD, and also funds various scholarships and awards. Other benefits provided to SIGDA members include the SIGDA's E-Newsletter containing information on upcoming conferences and funding opportunities, SIGDA News highlighting most relevant events in EDA and semiconductor industry, and the "What is...?" column that brings to the attention of EDA professionals the most recent topics of interest in design automation.

For further information on SIGDA's programs and resources, see www.sigda.org.

IEEE/COUNCIL ON ELECTRONIC DESIGN AUTOMATION

The IEEE is the world's leading professional association for the advancement of technology, with 430,000 members across 160 countries. The IEEE Council on Electronic Design Automation (CEDA) provides a single focal point for all EDA activities across six major IEEE societies (Circuits & Systems, Computer, Electron Devices, Solid State Circuits, Antennas & Propagation, and Microwave Theory & Techniques). The Council sponsors or co-sponsors over a dozen key EDA conferences around the world; its publications include ***IEEE Embedded Systems Letters, IEEE Transactions on CAD,*** and ***IEEE Embedded Systems Letters,*** as well as the co-publication, ***Design&Test Magazine***. Additionally, CEDA recognizes and supports its community by way of awards, travel grants, initiatives, and local chapters.

For more information on CEDA, visit: www.ieee-ceda.org, like us on Facebook, join us on LinkedIn, follow us on Twitter.

ELECTRONIC SYSTEM DESIGN ALLIANCE

The Electronic System Design Alliance (ESD Alliance), an international association of companies providing goods and services throughout the semiconductor design ecosystem, is a forum to address technical, marketing, economic and legislative issues affecting the entire industry. It acts as the central voice to communicate and promote the value of the semiconductor design industry as a vital component of the global electronics industry. For more information on the ESD Alliance, please visit: www.esd-alliance.org.

CONFERENCE INFORMATION

EXHIBIT HOURS

LOCATION: EXHIBIT HALLS 1-4

Monday, June 6	10:00am - 6:00pm
Tuesday, June 7	10:00am - 6:00pm
Wednesday, June 8	10:00am - 6:00pm

REGISTRATION HOURS

LOCATION: AUSTIN CONVENTION CENTER ATRIUM

Friday, June 3 - Sunday, June 5	8:00am – 6:00pm
Monday, June 6 - Thursday, June 9	7:00am – 7:00pm

Thank You to Our Sponsor: ANSYS

ONLINE PROCEEDINGS

DAC Proceedings and tutorials will be delivered electronically online via a username and password.

To access: http://proceedings.dac.com
Username = Email address
Password = Registration ID (on your badge)

Please refer to your registration receipt to be reminded of what package and associated files you are eligible to view.

STAY CONNECTED

WIRELESS INTERNET

Austin Convention Center has complimentary wireless internet service throughout the facility.

"BIRDS-OF-A-FEATHER" MEETINGS

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal, non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather" (BOF). All BOF meetings are held at the Austin Convention Center, Tuesday, June 7 from 7:00 - 8:30pm.

To arrange a BOF meeting, please contact Corinne@dac.com. An LCD projector and screen will be provided.

FIRST AID ROOM

First Aid Room is located between Exhibit Halls 3 & 4 on the Trinity Street side of the building.

First Aid Room Hours:
Saturday, June 4 - Sunday, June 5: **8:00am to 6:00pm**
Monday, June 6 - Thursday, June 9: **7:00am to 7:00pm**

Non-emergency: 311

In-house security: 512-404-4111

DAC MOBLE APP

Download the DAC App!

Review the conference program, find exhibitors, and create a personalized schedule all from your phone or mobile device.

The DAC App is **FREE** for registered attendees! Check your email for your personalized invite or visit DAC.com for more information

Google play | Available on the App Store

DAC NETWORKING OPPORTUNITIES

WELCOME RECEPTION

Sunday, June 5
5:30 - 7:00pm | 4th Floor Foyer

Join fellow attendees for the first event to network and kick-off DAC 2016!

Thank You to Our Sponsor:

AUSTIN CONVENTION CENTER

RECEPTION

Monday, June 6
6:00 - 7:00pm | Trinity St. Foyer

Join attendees for refreshments and lively discussion recapping the day's events.

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DAC SILICON/TECHNOLOGY ART SHOW

Monday, June 6
6:00 - 7:00pm | Trinity St. Foyer

The DAC Silicon/Technology Art Show will feature stunning images submitted by DAC attendees that demonstrate the beauty of everyday work in this industry. Submitted pieces will be judged in various categories and the winners for each category will be announced Wednesday, June 8 at 9:00am in Ballroom A.

RECEPTION

Tuesday, June 7
6:00 - 7:00pm | Trinity St. Foyer

Join us in the Foyer to see Work-in-Progress posters and enjoy light hors' d'oeuvres and beverages.

Thank You to Our Sponsors:

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RECEPTION

Wednesday, June 8
6:00 - 7:00pm | Trinity St. Foyer

Join us in the Foyer to see Work-in-Progress posters and enjoy light hors' d'oeuvres and beverages.

Thank You to Our Sponsor:

Don't miss the book signing:

RECEPTION

Thursday, June 9
5:30 - 6:30pm | 4th Floor Foyer

Join attendees for refreshments and lively discussion recapping the day's events.

KEYNOTE PRESENTATIONS

KEYNOTE: REVOLUTION AHEAD – WHAT IT TAKES TO ENABLE SECURELY CONNECTED, SELF-DRIVING CARS

Lars Reger - *Chief Technology Officer of Automotive Business Unit, NXP Semiconductors, Hamburg, Germany*

▶ ***Monday, June 6 || 9:15 - 10:00am || Ballroom A***

Few industries are as primed for radical change in the years ahead as the worldwide automotive market. Advanced driver assistance system (ADAS) features are increasingly common in entry-level/affordable new car models, and today's high-end vehicles commonly receive over-the-air software updates and feature semi-autonomous driving functionality. Meanwhile, Silicon Valley start-ups and established auto OEMs alike are rushing to deliver the first true "self-driving" cars.

See page 22 for more details.

VISIONARY TALK: LEARNING FROM LIFE: BIOLOGICALLY INSPIRED ELECTRONIC DESIGN

Lou Scheffer - *Principal Scientist, Janelia Research Campus, Howard Hughes Medical Institute, Chevy Chase, MD*

▶ ***Tuesday, June 7 || 9:00 - 9:20am || Ballroom A***

Modern electronics does amazing things, but biology routinely performs feats no current electronics can match. Every animal can learn on short timescales, defend against unforeseen threats, self-assemble and repair, all with great resilience. The shortest path to incorporating these features in our gadgets is to understand how biology works, then adapt these techniques to the semiconductor world.

See page 36 for more details.

KEYNOTE: DRIVING THE NEXT DECADE OF INNOVATIONS IN VISUAL AND ACCELERATED COMPUTING

Sameer Halepete - *Vice President of VLSI Engineering, NVIDIA Corp, Santa Clara, CA*

▶ ***Tuesday, June 7 || 9:20 - 10:00am || Ballroom A***

The ever-increasing performance demands of performance visual and accelerated computing has resulted in GPUs becoming some of the most complex ASICs being built today. These multi-billion transistor processors push design technologies to their limits and require incredibly robust implementation methodologies. At the same time, there are new performance demands from both the traditional source of gaming thanks to higher resolution displays and virtual reality applications as well as new GPU uses like deep learning and autonomous driving.

See page 36 for more details.

KEYNOTE: THE CHALLENGE TO DEVELOP TRULY GREAT PRODUCTS

Mark Papermaster - *Chief Technology Officer and Senior Vice President, Advanced Micro Devices, Inc., Sunnyvale, CA*

▶ ***Wednesday, June 8 || 9:00 - 10:00am || Ballroom A***

Mark Papermaster, CTO and SVP of Technology and Engineering at AMD, will take closer look at various challenges companies face when they set out to build winning products. Drawing up on more than 30 years of engineering experience, Mark explores innovation and what defines a great product, as well as his thoughts on the role of leadership to create an environment to enable both disruptive thinking combined with strong execution.

See page 53 for more details.

KEYNOTE: LEARNING AND MULTIAGENT REASONING FOR AUTONOMOUS ROBOTS

Peter Stone - *David Bruton, Jr. Centennial Professor of Computer Science, Univ. of Texas at Austin, TX*

▶ ***Thursday, June 9 || 9:10 - 10:00am || Ballroom A***

Over the past half-century, we have transitioned from a world with just a handful of mainframe computers owned by large corporations, to a world in which private individuals have multiple computers in their homes, in their cars, in their pockets, and even on their bodies. This transition was enabled by computer science research in multiple areas such as systems, networking, programming languages, human computer interaction, and artificial intelligence.

See page 71 for more details.

SKY TALKS

SKY TALK: WIRELESS IMPLANTABLE MICROSYSTEMS: MINIMALLY INVASIVE INTERFACES TO THE BRAIN

Rikky Muller - *Univ. of California, Berkeley & Cortera Neurotechnologies, Berkeley, CA*

▶ ***Monday, June 6 || 1:00 - 1:30pm || DAC Pavilion - Booth 1839***

Smart and connected medical implants are the next frontier in the Internet of Things (IoT) and are set to revolutionize healthcare. Advancing our ability to interface technology with biological environments will enable patients to be monitored and receive treatment at home, and in the long term, have chronically implanted electronic devices seamlessly integrate with their everyday lives. As an example, clinically viable and minimally invasive neural interfaces stand to transform disease care for patients of neurological conditions.

See page 24 for more details.

SKY TALK: RISC-V: INSTRUCTION SETS WANT TO BE FREE

Krste Asanovic - *Univ. of California, Berkeley & SiFive, Inc., Berkeley, CA*

▶ ***Tuesday, June 7 || 1:00 - 1:30pm || DAC Pavilion - Booth 1839***

The most important interface in a computer system is the instruction set architecture (ISA) as it connects software to hardware. So, given the prevalence of open standards for almost all other important interfaces, why is the ISA still proprietary? We argue that a free ISA is a necessary precursor to future hardware innovation, and there's no good technical reason not to have free, open ISAs just as we have free, open networking standards and free, open operating systems.

See page 41 for more details.

SKY TALK: SECURITY AT DIFFERENT LAYERS OF ABSTRACTIONS: APPLICATION, OPERATING SYSTEMS, AND HARDWARE

Bryan Payne - *Netflix, Los Gatos, CA*

▶ ***Wednesday, June 8 || 1:00 - 1:30pm || DAC Pavilion - Booth 1839***

When it comes to computer security, attackers often seek out weaknesses at the abstraction boundaries in a system. Therefore, boundaries between layers such as the hardware, operating system, and application have a significant security impact. This talk will address how security is influenced by different dimensions of computing including hardware and software abstractions and scale, along with how threat models can help to manage this complexity.

See page 58 for more details.

SKY TALK: BIOLOGICAL ELECTRONICS: MERGING LIFE'S TRANSISTORS WITH THE SOLID-STATE

Kenneth Shepard - *Columbia Univ., New York, NY*

▶ ***Thursday, June 9 || 1:00 - 1:30pm || Room 17AB***

Silicon integrated circuits based on CMOS technology form the basis for complex electronic systems with more than 10 billion transistors in a single chip. As the scaling of solid-state devices through Moore's Law reaches an end and there is a search to expand the capabilities of CMOS technology to new applications through the addition of new materials ("more than Moore"), biological components represent a largely untapped opportunity. Living systems have lipid bilayer membranes, which act as capacitors, storing charge as ionic gradients across these membranes.

See page 75 for more details.

ERNEST S. KUH | 1928 - 2015

Since June 2015, the design automation community has mourned a pioneering scholar, educator, visionary and mentor.

Professor Ernest Shiu-Jen Kuh was born in Beijing in 1928. He left China in 1947 to study electrical engineering at the University of Michigan, where he received the B.S. degree in 1949. He received the M.S. degree from MIT in 1950, and the Ph.D. degree from Stanford in 1952. From 1952 to 1956, he was a member of the Technical Staff at Bell Telephone Laboratories in Murray Hill, where his work on transmission repeater designs and submarine cable design was incorporated into the first trans-Atlantic telephone cable. He joined the UC Berkeley faculty in 1956.

After completing (with Charles Desoer) the classic 1967 textbook, Basic Circuit Theory, Professor Kuh served as chair of the newly integrated EE&CS department at Berkeley from 1968-1972. He then served as Dean of the College of Engineering from 1973-1980. His leadership and vision presciently opened up such new frontiers as bioelectronics; established the Industrial Liaison Program model of research interaction and the Berkeley Engineering Fund; and raised funds for what would become the Bechtel Engineering Center. A 1977-1978 sabbatical in Japan led to his interest in VLSI CAD, which became the focus of his research for the remainder of his career.

Professor Kuh shaped the field of placement and floorplanning with the Berkeley Building Block Layout (BBL) system; the RAMP resistive-network placement approach that exploited sparse-matrix techniques; the PROUD analytic placer; quadratic Boolean programming for multi-way partitioning; and many other seminal works. He shaped the field of routing with works on planar routing and single-row routing; graph models such the channel intersection graph for building-block layout; power/ground network sizing; and the matching-based approach to clock tree synthesis. It is no surprise that Volume 1, Issue Number 1 of IEEE Transactions on CAD (January 1982) contains the seminal paper of Yoshimura and Kuh, “Efficient Algorithms for Channel Routing”, which has been cited nearly 300 times.

As noted by his Ph.D. graduate, Dr. Chi-Ping Hsu, “Since the mid-1970s, Professor Kuh has been one of the key founding fathers of the EDA industry …. Many of the early EDA companies were formed by his students and fellow researchers. His vision and guidance helped expedite the formation and maturity of the EDA industry.” Even after decades of refinement and reinvention, the credit due to Professor Kuh’s many paradigmatic works (e.g., analytic placement, performance-driven layout, physical synthesis) remains clear. Today, many of Professor Kuh’s 40 Ph.D. graduates and numerous industrial visitors occupy senior leadership positions in academia and industry. Truly, EDA would not be what it is today without the many contributions of Professor Kuh and the “kuhsgroup” alumni.

Over his lifetime, Professor Kuh received numerous honors and awards for his pioneering contributions in active and passive circuit theory, electronic design automation of integrated circuits, and engineering education. These include the IEEE Centennial Medal, the IEEE Education Medal, the IEEE Circuits and Systems Society Award, the IEEE Millennium Medal, and the EDA Consortium’s Phil Kaufman Award. He was also a member of the National Academy of Engineering and the Academia Sinica, and a foreign member of the Chinese Academy of Sciences. From the mid-1970s, he worked to recruit and retain more women and people of color to the engineering field. With his wife Bettine, he endowed the Ernest S. Kuh Distinguished Lecture Series to bring notable scientists and engineers to campus. And even in retirement, he would sit through entire DAC sessions, listening carefully to the talks and asking the most probing and thought-provoking questions.

Dr. Wayne Dai, another Ph.D. graduate, said, “Professor Kuh has been my lifelong mentor and role model. His great vision of the ‘big picture,’ his brilliant mind driven by passion and persistence, and his deeply caring spirit that never faltered in its generosity will be remembered fondly by all of us.” Professor Kuh will be remembered by students and colleagues as a true scholar and gentleman, a sportsman who loved to play tennis, and a kind and generous mentor.

Memorial gifts may be directed to the Berkeley Engineering Fund, College of Engineering, 201 McLaughlin Hall #1722, Berkeley, CA 94720-1722, designated to the Ernest S. Kuh Distinguished Lecture Series. Donations may also be made to the California Alumni Association’s Professor Ernest Kuh Alumni Scholarship, sent to 1 Alumni House, Berkeley, CA 94720-7520.

In Prof. Kuh’s honor, CEDA has renamed its IEEE CEDA Early Career Award to IEEE CEDA Ernest S. Kuh Early Career Award.

STEVEN P. LEVITAN | 1950 - 2016

With a heavy heart, we say goodbye to Steven P. Levitan, a kind and inspiring colleague, a fabulous mentor, a distinctive educator and researcher, and a longtime DAC volunteer leader.

Steven P. Levitan was the John A. Jurenko Professor of Computer Engineering in the Department of Electrical and Computer Engineering at The University of Pittsburgh. He received his B.S. degree from Case Western Reserve University in 1972. From 1972 to 1977, he worked for Xylogic Systems designing hardware for computerized text processing systems. He received his M.S. (1979) and Ph.D. (1984), both in Computer Science, from the University of Massachusetts, Amherst. During that time he also worked for Digital Equipment Corporation, and Viewlogic Systems, as a consultant in HDL simulation and synthesis. Steve was an Assistant Professor from 1984 to 1986 in the Electrical and Computer Engineering Department at the University of Massachusetts. In 1987 he joined the Electrical Engineering faculty at the University of Pittsburgh where he held a joint appointment in the Department of Computer Science. Steve was co-founder and organizer of the Computer Engineering program at Pitt.

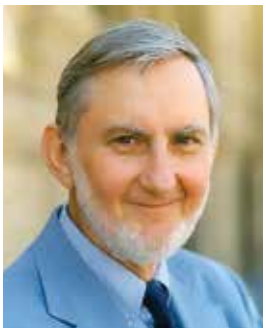
Steve's fundamental contributions to education and research in microsystems technology have spanned the three decades of his professional career. In the 1980s he partnered with engineers from Digital Equipment Corporation to develop one of the first VLSI design course sequences for undergraduate students at the University of Massachusetts, Amherst. This led to his creation of one of the first undergraduate VLSI capstone design sequences in the United States. Steve was an early strong advocate for VLSI capstone courses that tie together many of the fundamental ideas in a computer engineering degree as well as providing a necessary significant design experience for students before they entered the workforce.

Steve developed the first publically available compiler and simulator for the VHDL design language that he distributed to over 150 academic and industry users. In the mid-90s, Steve turned his attention to research and development of tools for mixed-technology microsystems. Funded by NSF and DARPA he developed the first multi-scale mixed technology simulator for electro-optical-mechanical systems. Steve was also instrumental in leading efforts to develop material for teaching functional verification at the undergraduate-level that has been adopted by more than 75 universities world-wide. He was working on new models of non-Boolean computing using the intrinsic dynamics of coupled oscillator systems funded by the NSF Expeditions in Computing Program at the time of his death.

Steve's service to the EDA community is immense. He was Chair of the ACM Special Interest Group on Design Automation (SIGDA). He was on the ACM/IEEE Design Automation Executive Committee from 1998 to 2008 and General Chair of the 44th DAC in 2007. Steve organized/co-organized numerous workshops for faculty development (including this year's DAC Young Faculty Workshop) and numerous workshops targeted at recruiting, retaining, and advancing undergraduate and graduate students in microsystems design. He was a great friend to many of his students, colleagues and collaborators.

Steve passed away unexpectedly during Spring Recess, on March 7, 2016, in his San Diego home. Steve's leadership, warmth, and humor will be missed but his legacy will remain.

EDWARD J. MCCLUSKEY | 1929-2016



Ed McCluskey, Professor Emeritus of Electrical Engineering and Computer Science at Stanford, was a giant who shaped the design and testing of digital systems for over half a century. He sustained a relentless pace of fundamental contributions for efficient and robust design, high-quality testing, and reliable operation of digital systems. Ed was also a pioneer in establishing and fostering computer engineering as a profession.

"Prof. McCluskey was the father of modern digital design. His seminal contributions to switching theory, logic design, testing and fault-tolerant computing laid the foundation for the computer processors that power so much of our world today," said Dr. Arvind Krishna, senior vice president and director of IBM Research.

Ed created the Quine-McCluskey logic minimization procedure as a doctoral student, which marked the beginning of Electronic Design Automation (EDA). Over the last 60 years, this method has been and continues to be used in numerous EDA tools. His work on hazards in logic circuits and fundamental-mode sequential circuits are classics.

When Ed entered the digital testing field in the late 1960s, it was considered "black art" without solid technical foundations. His deep insights transformed the way testing is practiced in industry and researched in academia: algebraic fault properties, Murphy and ELF experiments establishing test metrics (rather than fault models) as key to high-quality testing, and Very Low Voltage testing. Ed was on the forefront of exploring novel approaches, rooted in mathematical principles, for blending test into digital system design.

Ed and his students developed many key concepts in fault-tolerant computing. One example is diverse replication, logic circuitry implementing alternative structures to check the main structure, or watchdog processor checking the main program by executing a related, but simpler, version. Software diverse redundancy concepts in the ARGOS mission demonstrated feasibility of commercial off-the-shelf microprocessors in space applications. Ed's fault-tolerance and testing concepts are even more essential for safety in future applications such as self-driving cars.

Ed was one of the world's leading educators. His textbooks on logic design defined the discipline. Computer Engineering and the IEEE Computer Society owe their current status to Ed in a major way. He was first president of the IEEE Computer Society. At Princeton, Ed established the Computer Engineering curriculum, and founded the university computer center in the early 1960s. At Stanford, he founded the Digital Systems Lab (renamed Computer Systems Lab) that uniquely cultivated collaboration between EE and CS. "Ed McCluskey was a pioneer in the computer engineering community," said Stanford President John Hennessy. "He recruited me to Stanford to join the laboratory in 1977. In addition to shaping the development of digital systems, he was a great educator, producing an incredible group of [75] PhD graduates, many of whom have gone on to become industry leaders." He founded the Center for Reliable Computing (CRC) at Stanford. CRC played a major role in advancing the fields of computer reliability and testing from ad hoc pursuits to frontline academic and industrial research.

Ed received numerous awards and honors. Dr. Aart De Geus, Synopsys Chairman, summarized: "We see a great oak tree suddenly fall and immediately feel the void left behind. As a young student learning about Ed's work, all the way to today appreciating his contributions in making the 'digital revolution' not a slogan but a world-changing reality, we realize the impact of Ed's contribution on our field and our own destiny."

People wishing to share thoughts and memories of Ed are invited to send them to ejm.memorial@gmail.com.

IEEE Council on EDA (CEDA) sponsors a CEDA Luncheon at DAC in honor of Prof. Edward J. McCluskey on Tuesday, June 7th, at 12:00pm. It features tributes by leading researchers and a distinguished lecture. Please join us in Ballroom D to thank Ed!

MARIE R. PISTILLI | 1933 - 2015

Marie Pistilli took an unusual path to the EDA industry. She wasn't trained as an engineer but she played an important role in helping to guide the industry from its infancy. With the launch of the commercial EDA industry in 1982 there was a natural need to bring these young companies together (Daisy, Mentor, Valid, etc.) and DAC was the place to do it. Along with her husband Pat (DAC co-founder and an engineer at AT&T Bell Labs), Marie had the foresight to understand that for DAC to reach its potential it needed professional support and a steady hand so in 1984 MP Associates was born. Through Marie's steadfast leadership she was able to guide DAC through a period of tumultuous growth shepherding it from just 20 companies to over 250 by the end of the millennium, placing it as one of the top 100 shows in the US.

While her critical contribution was in helping the EDA industry through its early years of rapid and chaotic growth, perhaps her proudest contribution was in her efforts to gain recognition for the contributions of women in EDA. Along with a dedicated group of committee members, she worked to bring recognition to the many technical and industrial contributions of women in the evolution of design automation. While doing so she also worked to establish connections between women in all stages of their careers. In honor of her efforts the DAC executive Committee established the Marie R. Pistilli Women in EDA Achievement Award, which is awarded at DAC annually since 2001 to an individual who has a made a significant contribution to the advancement of women in the field of EDA. She remained active in these efforts until her death in November, 2015.

It is said that "If I have seen further it is by standing on the shoulders of giants." Through the foundation Marie built years ago, industry events such as DAC and ICCAD are still here and still going strong.

She is survived by Pat, her husband of 62 years, three daughters and 5 grandchildren.

GARY SMITH | 1941 - 2015

This year we lost a visionary in the field of design automation. Smith was the best-known industry analyst in EDA, a leading design technologist and foremost EDA strategist. He defined market segments, tracked market share, offered market growth projections, consulted with major EDA providers and their customers, published detailed research reports, and served as a tireless advocate for more efficient ways of designing chips that may have a billion transistors or more. A blog post called Smith the "single most important prognosticator in EDA."

Smith was the founder and chief analyst at Gary Smith EDA (GSEDA) since 2006. Prior to GSEDA, Smith was chief analyst at Dataquest (later known as Gartner Dataquest) beginning in 1994.

Born in Stockton, California, Smith grew up in the San Joaquin Valley. He earned a bachelor of science degree in engineering from the U.S. Naval Academy in Annapolis, Md. After 6 years of active duty in Vietnam, he embarked on a career in semiconductors starting in sales for a variety of companies, including National Electronics, International Rectifier, TRW, Signetics, Telmos, and Plessey. At Plessey, he went back into engineering as business unit manager for ASICs, which then represented some of the first attempts at customer-designed ICs.

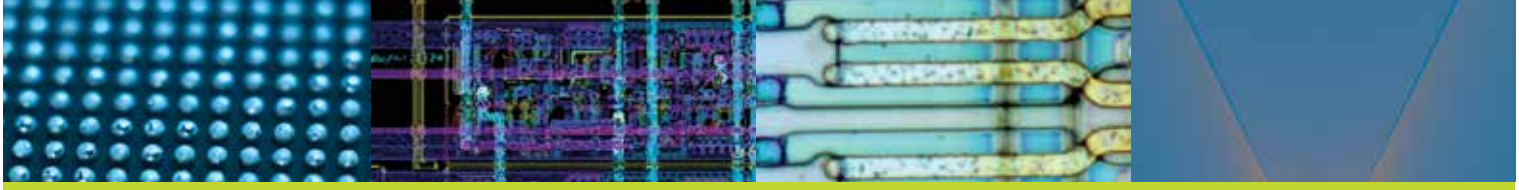
At LSI Logic, Smith became a CAD methodologist as well as an evangelist for the emerging register-transfer level (RTL) design methodology. This design methodology, which was widely adopted in the late 1980s and early 1990s, allowed engineers to work at a much higher level of abstraction than gate-level schematics. This breakthrough made possible the design of chips with hundreds of millions of transistors.

In 1994 Smith went to work as an EDA industry analyst for research firm Gartner Dataquest. For his lengthy tenure there, lasting until 2006, Smith was an authoritative, independent spokesperson who was widely quoted in the electronics trade press whenever EDA was mentioned. He was also a strong proponent of system-level design, often called Electronic System Level (ESL), which provides an even higher abstraction level than RTL and enables engineers to design both hardware and software.

Finally, Smith launched Gary Smith EDA in 2006 with several other former Gartner Dataquest analysts. Today the company is a provider of market intelligence and advisory services for the global EDA market. The company offers market share reports, research reports, an annual "What to see at DAC" (Design Automation Conference) list, Wallcharts that depict EDA vendor classifications, and strategic consulting services.

Outside of work, Smith was an accomplished musician, and he played bass guitar for the Los Gatos Blues Band. He was also a member of the Full Disclosure Blues Band, which had its debut at DAC 2001 and reprised its showcase performances at many subsequent DAC conferences. Smith's interests also included Eastern and Western philosophies and religions, travel, history, reading, visiting libraries and time with family.

A special Gary Smith Memorial Scholarship has been set up with San Jose State University. Guardian Scholars serves former foster and homeless youth attending San Jose State University. In addition DAC will enable the Gary Smith Memorial Scholarship students to attend DAC. To make a gift, please visit http://www.garysmitheda.com/memory.



DAC SILICON/TECHNOLOGY ART SHOW

Those of us who work in the Design Automation community can see the beauty in our work every day.
We create electronic devices with billions of transistors, complex algorithms, data visualizations, and clever data structures.
This year at DAC we want to showcase the beauty of our work for the rest of the world to see.
That's why we are hosting a silicon and technology art show.

Don't miss seeing these works of art at the Silicon/Technology Art Show, starting on Monday, June 6 at the Austin Convention Center. Judges will review each piece for several categories and winners will be announced Wednesday, June 8 at 9:00am in Ballroom A.

Thanks to everyone who submitted:

Bob Smith - *ESD Alliance:* **First MPW Wafer - circa 1981**

Christian Miller - *Concept Engineering GmbH:* **Welcome to 53rd DAC!**

Eric Tim - *IBM Corp.:* **Tri-Chip Pendant**

Guilherme Flach - *Univ. Federal do Rio Grande do Sul:* **Placement Scribbles; Placement Blast**

Kiran Gonsalves - *Intersil Corp.:* **FFT Processor on 3D IC**

Larry Toda - *Mentor Graphics Corp.:* **Mentor Graphics PCB Design Images; Thermal Images from Mentor Graphics**

Mateus Fogaca - *Univ. Federal do Rio Grande do Sul:* **Applying Poisson Equation with a Quadratic Approach to Standard Cell Placement; A bug in the circuit, literally!**

Michael Solka - *Coherent Logix, Inc.:* **Balls; Bumps**

Mike Gianfagna - *eSilicon Corp.:* **386 Plot; ASIC Plot; Bell Labs Microprocessor Plot; Cover - MOMA Chip Art Exhibit Book**

Nany Kollesar - *IBM Corp.:* **Tractor Beam; Inspiration Ball; Silicon Septopus; Forever Flower**

Nathaniel Pinckney - *Univ. of Michigan:* **Oversized bumps; BGA Test Socket**

Paula Sterling - *Synopsys, Inc.:* **Eye Diagram Abstract**

Ricardo Reis - *Univ. Federal do Rio Grande do Sul:* **MemoryHeart; Decoding Art; Z80 Register Cell; Acid Disaster or Poly Ballet; Color of Gates 2**

Richard Morse - *Morse Consulting:* **The Art of IC Design; Layout Abstraction; Old School**

Roland Weber - *Concept Engineering GmbH:* **Two blocks, 128 pins per side, inverted connection**

Sherie Taylor - *Intel Corp.:* **Merrifield Wafer; Skylake Die; Skylake Wafer**

Tania Ferla - *Univ. Federal do Rio Grande do Sul:* **Lithographic Simulation Kernels**

Vasso Kalaitzidou - *Fieldscale:* **Pillars of Innovation**

Yibo Lin - *Univ. of Texas at Austin:* **TPLPlace**

Jeff Gustafson - *Texas A&M Univ.:* **random3-h**

Misha Temkin - *Silvaco, Inc:* **Ion Implantation Channeling Effect**

Jan Henrik Weinstock - *RWTH Aachen Univ.:* **Euretile**

Karen Mangum - *Micro Magic, Inc.:* **Central Intelligence; MAX-3D**

Milos Popovic - *Univ. of Colorado:* **Enlightened Microprocessor**

Jose Paredes - *IBM Corp.:* **Scale Out Warmth; POWER8-E Wafer**

Olivier Sentieys - *IBM Corp.:* **Ochre: On-Chip Randomness Extraction**

Chrystian Guth - *Federal Univ.of Santa Catarina:* **Standard Cell Metropolis**

Rob Harrison - *ARM Ltd.:* **Juno**

Carl Das - *IMEC & Europractice:* **Artist impression of a EUROPRACTICE 0.13um MPW**

Hugo Romano - *TowerJazz:* **Development; Imagine; Spaceship; Flipchip**

Tsun-Ming Tseng - *Technische Univ. München:* **Automatic Layout Generation for Continuous-Flow Microfluidics**

Joe Civello - *Keysight Technologies:* **Electro-Thermal Dreaming**

Simone Casale Brunet - *École Polytechnique Fédérale de Lausanne:* **Execution Trace Graph of an HEVC video decoder**

Anupam Bakshi - *Agnisys, Inc.:* **Tag Chip**

Ahmed Nejim - *Silvaco, Inc.:* **Solar Cell**

Andreas Hoessinger - *Silvaco, Inc.:* **3D NAND Flash Memory**

Hongyi Yu - *Silvaco, Inc.:* **Flat Panel TFT**

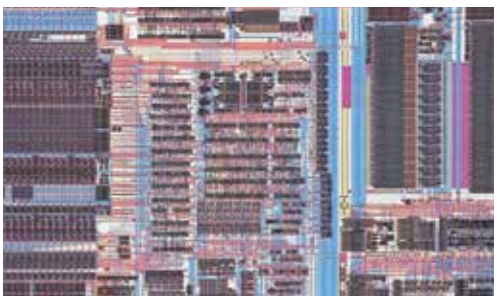
David Fried: *Coventor, Inc.:* **"14nm FinFET Technology" by Coventor® SEMulator3D®**

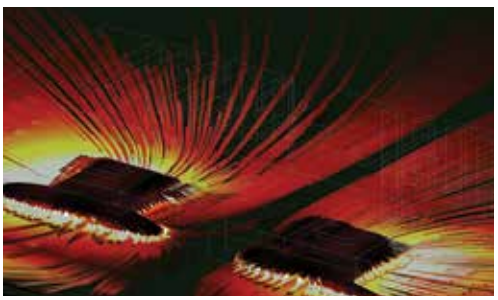
Yu-Hsuan Su & Yao-Wen Chang *-National Taiwan Univ.:* **Routability-driven multilevel routing**

Huang-Yu Chen, Szu-Jui Chou, Sheng-Lung Wang, & Yao-Wen Chang *- National Taiwan Univ.:* **A novel wire-density-driven full-chip routing system for CMP variation control**

Chau-Chin Huang & Yao-Wen Chang *- National Taiwan Univ.:* **Placement Considering Fence Regions**

Ina Prinz *- Arithmeum/Research Institute for Discrete Mathematics, Rheinische Friedrich-Wilhelms-Universität Bonn, Germany*





ART SHOW RECEPTION

Monday, June 6 | 6:00 - 7:00pm
Trinity St. Foyer

WORKSHOPS

W1 WORKSHOP 1: DAC WORKSHOP ON COMPUTING IN HETEROGENEOUS, AUTONOMOUS 'N' GOAL-ORIENTED ENVIRONMENTS (CHANGE)

Time: 9:00am - 5:00pm || Room: 19AB || Event Type: Workshop
Track: Embedded Systems, Design || Topic Area: Emerging Technologies, General Interest, Reconfigurable Systems

ORGANIZERS:

Marco Santambrogio - *Politecnico di Milano, Italy*
Hank Hoffmann - *Univ. of Chicago, IL*

As the push for parallelism continues to increase the number of cores on a chip, system design has become incredibly complex; optimizing for performance and power efficiency is now nearly impossible for the application programmer. To assist the programmer, a variety of techniques for optimizing performance and power at runtime have been developed, but many employ the use of speculative threads or performance counters. These approaches result in stolen cycles, or the use of an extra core, and such expensive penalties can greatly reduce the potential gains.

Within this context imagine a revolutionary computing system that can observe its own execution and optimize its behavior around a user's or application's needs. Imagine a programming capability by which users can specify their desired goals rather than how to perform a task, along with constraints in terms of an energy budget, a time constraint, or simply a preference for an approximate answer over an exact answer.

Imagine further a computing system that performs better according to a user's preferred goal the longer it runs an application. Such an architecture will enable, for example, a handheld radio or a cell phone that can run cooler the longer the connection time. Or, a system that can perform reliably and continuously in a range of environments by tolerating hard and transient failures through self healing.

Self-aware computer systems are the key technology to succeed in doing this. They will be able to configure, heal, optimize, improve interaction and protect themselves without the need for human intervention, exploiting abilities that allow them to automatically find the best way to accomplish a given goal with the resources at hand. Within this context, imagine a revolutionary computing system that can observe its own execution and optimize its behavior around the external environment, user's and application's needs.

The Self-Aware computing research leverages the new balance of resources to improve performance, utilization, reliability and programmability. Within this context, the proposed workshop is intended to present innovative works describing:

- Self-aware Operating Systems

- Autonomous self-aware computer architecture

- Adaptive algorithm and distributed self-training algorithms

- Biologically inspired systems

SPEAKERS:

Nikil Dutt - *Univ. of California, Irvine, CA*
Wayne Luk - *Imperial College London, United Kingdom*
Jonathan Eastep - *Intel Corp., Portland, OR*
Jian Li - *Huawei Technologies Co., Ltd., Austin, TX*
Gianluca Durelli - *Politecnico di Milano, Italy*
Diana Goehringer - *Univ. Bochum, Germany*
Matteo Ferroni - *Politecnico di Milano, Italy*

W2 WORKSHOP 2: INTERNATIONAL WORKSHOP ON DESIGN AUTOMATION FOR CYBER-PHYSICAL SYSTEMS

Time: 9:00am - 5:00pm || Room: 15 || Event Type: Workshop || Track: Design, IoT
Topic Area: Cyber-Physical Systems

ORGANIZERS:

Shiyan Hu - *Michigan Technological Univ., Houghton, MI*
Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*
Qi Zhu - *Univ. of California, Riverside, CA*
Yier Jin - *Univ. of Central Florida, Orlando, FL*
Bei Yu - *Chinese Univ. of Hong Kong, China*

Cyber-Physical Systems (CPS) are characterized by the strong interactions among cyber components and dynamic physical components. CPS system examples include automotive and transportation systems, smart home, building and community, smart battery and energy systems, surveillance systems, cyber-physical biochip, and wearable devices. Due to the deeply complex intertwining among different components, CPS designs pose fundamental challenges in multiple aspects such as performance, energy, security, reliability, fault tolerance and flexibility. Tackling these challenges necessitates high performance design automation techniques.

This workshop will present the state-of-the-art research results on the topic of design automation for CPS, and stimulate the CAD researchers to participate in the interdisciplinary CPS research area in the future.

SPEAKERS:

P.R. Kumar - *Texas A&M Univ., College Station, TX*
Subhasish Mitra - *Stanford Univ., Stanford, CA*
Rajesh Gupta - *Univ. of California at San Diego, La Jolla, CA*
Sachin Sapatenkar - *Univ. of Minnesota, Minneapolis, MN*
Sharon Hu - *Univ. of Notre Dame, IN*
David Z. Pan - *Univ. of Texas at Austin, TX*
Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*
Shiyan Hu - *Michigan Technological Univ., Houghton, MI*
Bei Yu - *Chinese Univ. of Hong Kong, China*
Chengbin Ma - *Shanghai Jiao Tong Univ., Shanghai, China*

W3 WORKSHOP 3: SYSTEM-TO-SILICON PERFORMANCE MODELING AND ANALYSIS - POWER, TEMPERATURE AND RELIABILITY

Time: 9:00am - 5:00pm || Room: 17AB || Event Type: Workshop
Track: Embedded Systems, Design || Topic Area: Cyber-Physical Systems, System Architectures & SoC, Codesign & System Design

ORGANIZERS:

Adam Morawiec - *ECSI, Belmont, France*
Laurent Maillet-Contoz - *STMicroelectronics, Grenoble, France*
Kim Grüttner - *OFFIS – Institute for Information Technology, Oldenburg, Germany*
Gjalt de Jong - *ArchWorks, Diegem, Belgium*

The integration of heterogeneous electronic systems composed of SW and HW requires not only a proper handling of system functionality, but also an appropriate expression and analysis of various extra-functional properties: timing, energy consumption, thermal behavior, reliability, cost and others as well as performance aspects related to caching, non-determinism, probabilistic effects.

The workshop addresses cross-domain aspects related to the design and verification framework covering methodology, interoperable tools, flows, interfaces and standards that enable formalization, specification, annotation and refinement of functional and extra-functional properties of a system. Special emphasis will be given to formalization and expression of power, temperature, reliability, degradation and aging.

Several research and industry efforts address (parts of) the problem. However, there is a need for community-wide cooperation to establish a holistic vision on extra-functional property treatment, and to agree on research and development directions and further on validation of applicable solutions and standardization.

This event will support collaboration between main actors from system and microelectronics industry, EDA and research.

The workshop is inviting submissions of short abstracts on industrial and scientific work in progress and practical solution and experiences.

Main topics:

- Extra-functional property modeling (power, temperature, reliability, aging, …)
- Power and temperature analysis at SoC level: future needs and requirements
- Evolution and extensions of standards like UPF, IP-XACT to express extra-functional properties
- Power and temperature simulation and analysis at system-level
- System level reliability and aging models
- Reliability from transistor to RTL level: e.g. NBTI models including basic physical properties

SPEAKERS:

Eugenio Villar - *Univ. de Cantabria, Santander, Spain*
Kim Grüttner - *OFFIS – Institute for Information Technology, Oldenburg, Germany*
Daniel Lorenz - *OFFIS – Institute for Information Technology, Oldenburg, Germany*
Ralph Weissnegger - *CISC Semiconductor GmbH, Graz, Austria*
Laurent Maillet-Contoz - *STMicroelectronics, Grenoble, France*
Franco Fummi - *EDALab s.r.l., Verona, Italy*
Emmanuel Vaumorin - *Magillem Design Services, Paris, France*
Roland Jancke - *Fraunhofer IIS, Dresden, Germany*
Michael Pronath - *MunEDA GmbH, Munich, Germany*
Gilson Wirth - *Univ. Federal do Rio Grande do Sul, Rio Grande, Brazil*

W4 WORKSHOP 4: ACM/IEEE DAC WORKSHOP ON INTERNET OF THINGS (IOT)

Time: 9:00am - 6:00pm || Room: 18AB || Event Type: Workshop || Track: IoT, Design
Topic Area: General Interest, Emerging Technologies, Circuit Design

ORGANIZER:

Rasit Topaloglu - *IBM Corp., Hopewell Junction, NY*

As more low-power and internet-connected gadgets and sensors are integrated into our lives, there still is not a consensus of how to co-design these. This workshop focuses on three areas of the internet of things (IoT), and in particular the design and automation aspects within them. These areas, which will likely be key to advancements in the IoT arena, are: security, low-power, and system design. The workshop features a set of invited speakers and panels. With our speakers, we strive to understand key issues and known solutions within the above mentioned areas of research and product design. End goals of the workshop are to understand about design and automation needs and issues beyond what may be directly visible to the DAC community and try to bring them in towards a solution.

Program Committee:
Farinaz Koushanfar - *Univ. of California at San Diego, La Jolla, CA*
Peng Li - *Texas A&M Univ., College Station, TX*
Subhasish Mitra - *Stanford Univ., Stanford, CA*
David Z. Pan - *Univ. of Texas at Austin, TX*
Rasit O. Topaloglu - *IBM Corp., Hopewell Junction, NY*

SPEAKERS:

Pradip Bose - *IBM Research, Yorktown Heights, NY*
Sandip Ray - *Intel Corp., Hillsboro, OR*
Martin Saint-Laurent - *Qualcomm, Inc., Austin, TX*
Edgar Sanchez-Sinencio - *Texas A&M Univ., College Station, TX*
Hamed Soroush - *Real-Time Innovations, Sunnyvale, CA*
Vamsi Talla - *Univ. of Washington, Seattle, WA*
Mohit Tiwari - *Univ. of Texas at Austin, TX*
Yuan Xie - *Univ. of California, Santa Barbara, CA*

W5

WORKSHOP 5: LOW-POWER IMAGE RECOGNITION CHALLENGE (LPIRC)

Time: 9:00am - 5:00pm || Room: 14 || Event Type: Workshop
Track: Design, Embedded Systems || Topic Area: Low-Power & Reliability, System Architectures & SoC

ORGANIZERS:

Yung-Hsiang Lu - *Purdue Univ., West Lafayette, IN*
Alexander Berg - *Univ. of North Carolina, Chapel Hill, NC*
David Z. Pan - *Univ. of Texas at Austin, TX*
Daniel Hammerstrom - *Defense Advanced Research Projects Agency, Arlington, VA*
Greg Lemming - *Intel Corp., Issaquah, WA*
David Atienza Alonso - *Swiss Federal Institute of Technology, Lausanne, Switzerland*
Massimo Alioto - *National Univ. of Singapore, Singapore*

The second Low-Power Image Recognition Challenge (LPIRC) will be held at the 2016 Design Automation Conference in Austin, Texas. Cameras have become available in many embedded and mobile systems, including vehicles, smartphones, wearable devices, and aerial robots. It is desirable to have the capability of detecting and identifying objects in images acquired from such devices. Since energy is limited in mobile systems, efficiency and energy conservation are primordial.

The winners must demonstrate high accuracy in image recognition using the least amount of energy. Each image contains one or several objects. The objects are chosen from different categories. A contestant must identify the objects by their categories as well as marking the objects by bounding boxes. The energy is measured by a high-speed power meter. This is an onsite competition and participants must bring their own systems.

LPIRC 2016 has three tracks. The first two tracks (1) offloading and (2) non-offloading are the same as in LPIRC 2015. The test images are sent through a network. In the third, new track, the test images are shown on a computer screen and the contestants must use cameras to obtain the input images.

The first LPIRC was held at the 2015 Design Automation Conference on June 7, 2015 in San Francisco, California. Thirty-four people registered as ten teams from four different countries. In total, twenty solutions were presented.

A special session at the International Conference on Computer-Aided Design 2015 was devoted to the introduction and description of the first LPIRC. The top two winners of the first LPIRC presented their solutions.

WELCOME TO AUSTIN!

Austin is the capital of Texas, home of the University of Texas at Austin and gateway to the beautiful Hill Country. As the Live Music Capital of the World, the city has a soundtrack all its own.

More than 250 live music venues flourish with rock, indie, pop and Tejano. Top notch restaurants with legendary barbeque and farm-to-table cuisine whet your appetite. Find out more at austintexas.org.

MONDAY, JUNE 6

OPENING SESSION & AWARDS PRESENTATION

Time: 8:45am - 9:15am || Room: Ballroom A || Topic Area: General Interest

Join us as we set the stage for the 53rd DAC! DAC's Executive Committee will highlight the conference's events, and the award presentations will recognize success and excellence for individuals in the industry.

2015 PHIL KAUFMAN AWARD FOR DISTINGUISHED CONTRIBUTIONS TO EDA

Dr. Walden Rhines, Chairman and CEO of Mentor Graphics Corporation Wilsonville, Oregon

Dr. Rhines is being recognized for growing the EDA and integrated circuit (IC) design industries through his efforts as a leading voice of EDA and for pioneering the evolution of IC design to system-on-chip (SoC) design.

IEEE CEDA OUTSTANDING SERVICE AWARD

Anne Cirkel, Mentor Graphics

For outstanding service to the EDA community as DAC General Chair in 2015.

IEEE CEDA OUTSTANDING SERVICE AWARD

Krithi Ramamritham, Indian Institute of Technology, Bombay

For outstanding service to the EDA community as Editor-in-Chief of IEEE Embedded Systems Letters from 2011 to 2015.

IEEE FELLOW

Xiaobo Sharon Hu, University of Notre Dame

For contributions to resource management for embedded systems.

IEEE FELLOW

Jiang Hu, Texas A&M University

For contributions to gate, interconnect and clock network optimization in VLSI circuits.

IEEE FELLOW

Peng Li, Texas A&M University

For contributions to the analysis and modeling of integrated circuits and systems.

IEEE FELLOW

Chris Rowen, Cadence Design Systems

For leadership in the development of microprocessors and reduced instruction set computers

IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS DONALD O. PEDERSON BEST PAPER AWARD

Shupeng Sun, Xin Li, Hongzhou Liu, Kangsheng Luo, and Ben Gu

"Fast Statistical Analysis of Rare Circuit Failure Events via Scaled-Sigma Sampling for High-Dimensional Variation Space," Vol. 34, Issue 7, pp. 1096 - 1109, July 2015.

A. RICHARD NEWTON TECHNICAL IMPACT AWARD IN ELECTRONIC DESIGN AUTOMATION

Chandu Visweswariah, IBM; Kaushik Ravindran, National Instruments; Kerim Kalafala, IBM; Steven G. Walker, IBM; Sambasivan Narayan, Apple

Sponsored by the IEEE Council on EDA and the ACM Special Interest Group on Design Automation.

For pioneering contributions to statistical static timing analysis.

C. Visweswariah, K. Ravindran, K. Kalafala, S. G. Walker, S. Narayan, "First-Order Incremental Block-Based Statistical Timing Analysis." Proc. of the 41st Design Automation Conference, pp. 331 – 336, June 2004.

ACM TODAES 2016 BEST PAPER AWARD

Chung-Wei Lin, UC Berkeley, Bowen Zheng, UC Riverside, Qi Zhu, UC Riverside, Alberto Sangiovanni-Vincentelli, UC Berkeley

Security-Aware Design Methodology and Optimization for Automotive Systems

Vol. 21, Issue 1, November 2015

2016 ACM SIGDA OUTSTANDING NEW FACULTY AWARD

Prof. Swaroop Ghosh, University of South Florida

In recognition of a junior faculty member who demonstrates outstanding potential as an educator and/or researcher in the field of electronic design automation.

2016 ACM SIGDA OUTSTANDING PHD DISSERTATION AWARD IN ELECTRONIC DESIGN AUTOMATION

Dr. Zheng Zhang – "Uncertainty Quantification for Integrated Circuits and Microelectromechanical Systems," Massachusetts Institute of Technology

Advisor: Luca Daniel

In recognition of an outstanding Ph.D. dissertation that makes the most substantial contribution to the theory and/or application in the field of electronic design automation.

ACM FELLOW

Naehyuck Chang, KAIST

For contributions to low-power computing systems.

ACM FELLOW

Kevin Skadron, University of Virginia

For contributions in power and thermal-aware modeling, design and benchmarking of microprocessors, including GPUs.

ACM FELLOW

Tei-Wei Kuo, Research Center for Information Technology Innovation, Academia Sinica

For contributions to performance and reliability enhancement of flash-memory storage systems.

ACM SIGDA DISTINGUISHED SERVICE AWARD

Dr. Steven Levitan

In recognition of a lifetime of devoted service to ACM SIGDA and the Electronic Design Automation community. This award will be received by Anna Balazs.

2016 MARIE R. PISTILLI WOMEN IN ENGINEERING ACHIEVEMENT AWARD

Soha Hassoun, Professor and Chair of the Department of Computer Science at Tufts University

This annual award, named for Marie R. Pistilli, the former organizer of DAC, recognizes individuals who have visibly helped advance women in Electronic Design.

P.O. PISTILLI UNDERGRADUATE SCHOLARSHIPS FOR ADVANCEMENT IN COMPUTER SCIENCE AND ELECTRICAL ENGINEERING

Nicole Amoako, Columbia University

The objective of the P.O. Pistilli Undergraduate Scholarship for Advancement in Computer Science and Electrical Engineering is to increase the pool of professionals in Electrical and Computer Engineering and Computer Science from under-represented groups (female, African-American, Hispanic, Native American, and disabled students). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. DAC normally funds a $4000 scholarship, renewable up to five years, to graduating high school seniors who have a 3.00 GPA or better (on a 4.00 scale).

KEYNOTE: REVOLUTION AHEAD – WHAT IT TAKES TO ENABLE SECURELY CONNECTED, SELF-DRIVING CARS

Lars Reger - *NXP Semiconductors, Hamburg, Germany*

Time: 9:15am - 10:00am || Room: Ballroom A
Track: Automotive, Security || Topic Area: Cyber-Physical Systems, General Interest, System Software

Few industries are as primed for radical change in the years ahead as the worldwide automotive market. Advanced driver assistance system (ADAS) features are increasingly common in entry-level/affordable new car models, and today's high-end vehicles commonly receive over-the-air software updates and feature semi-autonomous driving functionality. Meanwhile, Silicon Valley start-ups and established auto OEMs alike are rushing to deliver the first true "self-driving" cars. Among the most critical technologies driving this revolution are:

- Highly integrated CMOS-based radar solutions that can replace today's bulky, power-consuming hardware for radar-based ADAS with sensors the size of postage stamps – for self-driving cars cocoons of such sensors are needed to enable a reliable 360 surround view of the vehicle environment
- Gigabit Ethernet in-car communication technology enabling deterministic performance and real-time transport of massive
  data sets.
- Advancements in vehicle-to-vehicle (V2V) and vehicle-to-infrastructure (V2I) technologies that support secure data exchanges between high-speed vehicles and roadside infrastructure.
- Increasingly rapid adoption of next-generation RFID and Near Field Communication (NFC) technologies for a broad range of connectivity innovations.

However, despite the rapid advancement of these Connected Car technologies, the era of autonomous vehicles cannot truly arrive until consumers really trust that their vehicles are safe against hacking. This discussion will present an in-depth examination of the specific technologies driving the autonomous vehicles revolution of the future, while detailing the security, reliability and safety requirements necessary to realize its full potential.

Biography: Lars Reger is Chief Technology Officer of NXP's Automotive business unit. NXP is the global technology leader in the secure connected car with a market leading product portfolio in secure and smart car access, car infotainment, advanced driver assistance systems, in-vehicle networks, and sensors. As CTO, Lars is responsible for managing R&D and new business activities for NXP Automotive.

Prior to joining NXP in 2008, Lars gained deep insight into the microelectronics industry – with a strong focus on the automotive sector – in various functions with Siemens, Infineon, Siemens VDO and Continental. Before joining NXP, Lars was Director of Business Development and Product Management within the Connectivity business unit at Continental. His past roles at Infineon included Head of the Process and Product Engineering departments, Project Manager for Mobile System Chips, and Director of IP Management. He began his career with Siemens Semiconductors as Product Engineer in 1997. Lars holds a university degree in physics from Rheinische-Friedrich-Wilhelms University of Bonn and an executive MBA from London Business School.

1 DESIGN TRACK: CUSTOM HARDWARE FOR ALGORITHMIC TRADING

Time: 10:30am - 12:00pm || Room: Ballroom E || Event Type: Invited Presentations
Track: Design, Embedded Systems || Topic Area: Emerging Technologies, Logic & High-Level Synthesis, Business

CHAIR:
Davor Frank - *Solarflare Communications, New York, NY*

In today's financial markets there is a constant, growing trend in the amount of data and the speed at which that data must be handled. Participants in these markets are confronted with ingesting and processing this data in an increasingly competitive landscape where the speed at which this data is processed is one of the major drivers of success. Algorithmic trading systems are deployed to address this challenge, but traditional software running on commodity hardware is not sufficient to maintain a competitive advantage in this environment. Increasingly, organizations are turning to custom hardware to address these problems. In this session, you will hear industry practitioners discuss how hardware solutions are being utilized in this space.

1.1 Trading Fast and Slow – Implications for Technology In Complex Financial Application Development (10:30)
Mike Strickland - *Intel Programmable Solutions Group, San Jose, CA*
Stephen Weston - *Intel Programmable Solutions Group, London, United Kingdom*

1.2 Case Study For Use of Hardware Platform In Algorithmic Trading (11:00)
Luc Burgun - *NovaSparks, Paris, France*

1.3 An Agile FPGA Development Workflow (11:30)
Todd Strader - *Two Sigma Investments, LP, New York, NY*

Thank You to Our Sponsor:

2 DESIGN TRACK: TIMING OPTIMIZATION & SIGNOFF

Time: 10:30am - 12:00pm || Room: Ballroom F || Event Type: Reviewed Presentations
Track: EDA, Design || Topic Area: Physical Design, Modeling, Simulation & Timing

CHAIR:
Greg Ford - *GLOBALFOUNDRIES, Santa Clara, CA*

Timing in IP and at chip level in recent technology nodes has become increasingly complex. It has become necessary to incorporate many more physical effects into the modeling of timing, and this has affected both signoff and optimization in significant ways. This session will cover variation modeling in signoff, as well as optimization concerns like path sensitivity analysis and power-aware vt and size optimization techniques. Both chip and IP level timing closure and timing constraint management will be discussed.

2.1 Physical Aware Logic Difference Extraction in ECO Synthesis for Industrial High Performance Designs (10:30)
George Antony - *IBM Systems and Technology Group & Indian Institute of Technology Madras, Bangalore, India*
Sridhar H. Rangarajan - *IBM Systems and Technology Group, Bangalore, India*
Nitin Chandrachoodan - *Indian Institute of Technology Madras, Chennai, India*
Shyam Ramji - *IBM Systems and Technology Group, Poughkeepsie, NY*

2.2 IP Timing Constraints Promotion Challenges (A method to automatically generate SoC Timing Constraints) (10:45)
Ichiro Shiihara, **Tatsuya Nakae** - *Socionext, Inc., Yokohama, Japan*
Takanori Inaba - *Socionext, Inc., Kyoto, Japan*

2.3 Vt and Size Optimization Considering Dynamic Power and Minimum Width Constraints (11:00)
George Gonzalez, Mahesh Sharma - *Advanced Micro Devices, Inc., Austin, TX*
Erhan Ergin - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Sabeesh Balagangadharan - *Advanced Micro Devices, Inc., Bangalore, India*
Tim Puzey, William Keshlear - *Advanced Micro Devices, Inc., Austin, TX*
Amartya Mazumdar - *Advanced Micro Devices, Inc., Bangalore, India*
Robert Cole - *Advanced Micro Devices, Inc., Boxborough, MA*

2.4 Path Sensitivity Analysis and Optimization for SOC Wide-Range Operation (11:15)
Jiyoun Kim, Eunju Hwang, Mijeong Lim, Kyungtae Do - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*

2.5 Sensitivity Usage in Statistical Static Timing Signoff (11:30)
Robert Allen - *IBM Systems and Technology Group, Essex Jct., VT*
Nathan Buck - *IBM Corp., Underhill, VT*
Eric Foreman - *IBM Systems and Technology Group, Essex Jct., VT*
Stephen Shuma - *IBM Corp., Essex Jct., VT*

2.6 Accurate Signoff with Advanced Variation Methodology (11:45)
Moon Su Kim, Eun Yeung Yu - *Samsung Electronics Co., Ltd., Suwon, Republic of Korea*
Eunbyeol Kim - *Samsung Electronics Co., Ltd., Hwaseong, Republic of Korea*
Ayhan Multu - *Synopsys, Inc., San Jose, CA*

Q&A Poster Session
Monday, June 6 5:00 - 6:00pm - Exhibit Floor

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3 IP TRACK: IP TRENDS AND REQUIREMENTS

Time: 10:30am - 12:00pm || Room: Ballroom G || Event Type: Invited Presentations
Track: IP, Design || Topic Area: Business, General Interest

CHAIR:
Simon Rance - *ARM Ltd., Dallas, TX*

IP Trends and requirements are continuously evolving to address the needs of our daily life from health, environment, and automotive to entertainment and communications.

In this session, we will see presentations that demonstrate leading-edge trends and requirements covering the Internet of Everything (IoE), which is emerging as the next frontier of connectivity to conquer, as well as functional safety as an emerging requirement for SoC Designers and vendors of silicon IP. The final presentation will address current interconnect IP trends and see how specific system architecture and verification requirements can help choose which interconnect IP and configuration is best suited.

3.1 IOE and How to Power it (10:30)
Jamil Kawa - *Synopsys, Inc., Mountain View, CA*

3.2 How to choose which Interconnect IP and configuration is best suited for my system architecture needs and application requirements (11:00)
Nick Heaton - *Cadence Design Systems, Inc., San Jose, CA*

3.3 Functional safety - and what that means for an IP (11:30)
Andrew Hopkins, Lauri Ora - *ARM Ltd., Cambridge, United Kingdom*

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SKY TALK: WIRELESS IMPLANTABLE MICROSYSTEMS: MINIMALLY INVASIVE INTERFACES TO THE BRAIN

Time: 1:00pm - 1:30pm || Room: DAC Pavilion - Booth 1839 || Event Type: SKY Talk
Track: IoT, Embedded Systems || Topic Area: Circuit Design, Cyber-Physical Systems, Emerging Technologies

Smart and connected medical implants are the next frontier in the Internet of Things (IoT) and are set to revolutionize healthcare. Advancing our ability to interface technology with biological environments will enable patients to be monitored and receive treatment at home, and in the long term, have chronically implanted electronic devices seamlessly integrate with their everyday lives. As an example, clinically viable and minimally invasive neural interfaces stand to transform disease care for patients of neurological conditions. Recently there has been an explosion of research in Brain-Machine Interfaces (BMI) that has shown incredible results in using electronic signals from the motor cortex of the brain to control artificial limbs, providing hope for patients with spinal cord injuries. A major impediment to clinical translation is that state-of-the-art clinical neural interfaces are large, wired and require open-skull operation which leaves the patient at risk of infection and unable to move. Future, less invasive interfaces with increased numbers of electrodes, signal processing, and wireless connectivity will enable advanced prosthetics, disease control and completely new user-computer interfaces.

Substantial improvements in neural implant longevity are needed to transition BMI systems from research labs to clinical practice. In this talk I will describe the development of a minimally invasive, wireless neural implant to enable chronic and stable neural recording. The implant is based on micro-electrocorticography (µECoG), an electrophysiological technique where electrical potentials are recorded from the surface of the cerebral cortex, reducing cortical scarring when compared with microelectrode recording techniques that pierce into the cortex. Wireless powering and readout are combined with a flexible, microfabricated antenna and electrode array with an ultra-low power integrated circuit. The low power consumption of the integrated circuit enables remote powering well below established IEEE and FCC safety limits, while the small size and flexibility of the implant minimizes the foreign body response. The improved implant safety and longevity gives wireless µECoG excellent prospects to become the technology of choice for clinically relevant neural interfaces in the foreseeable future.

SPEAKER:
Rikky Muller - *Univ. of California, Berkeley & Cortera Neurotechnologies, Berkeley, CA*

4 DESIGN TRACK: EVOLVING INFRASTRUCTURE IN THE AGE OF CLOUD AND IOT

Time: 1:30pm - 3:00pm || Room: Ballroom E || Event Type: Invited Presentations
Track: Design, IoT || Topic Area: General Interest, Emerging Technologies

CHAIR:
Joseph P. Skudlarek - *Mentor Graphics Corp., Wilsonville, OR*

The path dictated by The Learning Curve (Moore's Law being one version) has led to systems of ever-increasing sophistication. Cloud and IoT represent two of the latest manifestations of this trend which bring us increased hardware and software complexity, shorter product lifecycles, and growing security concerns all of which eventually lead to steadily increasing compute and bandwidth requirements during design and operation phases for systems and networks. This session explores evolution of infrastructure from three perspectives: (i) digital enterprise to enable ideation, realization and utilization to achieve business goals in the age of IoT; (ii) virtualization of the network edge a.k.a. Fog Computing which underwrites the growth of IoT; (iii) embedding of security in individual workloads migrated to a cloud environment.

4.1 How the Internet of Things is Driving the Semiconductor Industry (1:30)
Sia Langrudi - *Siemens Corp., San Jose, CA*

4.2 Challenges for Next Generation Fog and IoT Computing (2:00)
Mark Douglas - *NXP Semiconductors, Austin, TX*

4.3 Accelerating and securing Cloud workloads using general purpose acceleration engines (2:30)
Srini Addepalli - *Intel Corp., Santa Clara, CA*

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5 DESIGN TRACK: POWER MANAGEMENT IN ADVANCED IC DESIGN

Time: 1:30pm - 3:00pm || Room: Ballroom F || Event Type: Reviewed Presentations
Track: EDA, Design || Topic Area: Low-Power & Reliability, Modeling, Simulation & Timing

CHAIR:
Stephen Quay - *IBM Corp., Austin, TX*

Addressing power has become a critical and challenging concern for designs at advanced technology nodes. This requires accurate modeling and analysis of complex effects, as well as circuit design and optimization at various design stages to mitigate power. Topics in this session address self-heating in high-performance microprocessors, power and EM characterization of standard-cells, and block-, gate-, and post-layout transistor-level thermal analysis techniques. Also presented are novel power grid structures for wire bonded designs and post-silicon, work-load induced leakage power characterization for advanced microprocessors.

5.1 End to End Self Heating Analysis Methodology and Toolset for High Performance Microprocessor Designs (1:30)
Nagu Dhanwada - *IBM Corp., Poughkeepsie, NY*
Leon Sigal - *IBM Research, Yorktown Heights, NY*
William Dungan - *IBM Corp., Poughkeepsie, NY*
Michael Scheuermann - *IBM Research, Yorktown Heights, NY*
Arun Joseph - *IBM Systems and Technology Group, Bangalore, India*
Arjen Mets - *IBM Corp., Yorktown Heights, NY*
Sungjae Lee - *IBM Corp., Albany, NY*
Karl Moody - *IBM Corp., Essex Junction, VT*
Shashidhar Reddy - *IBM Corp., Bangalore, India*
Kartik Acharya - *IBM Systems and Technology Group, Sandy Springs, GA*
Erich C. Schanzenbach - *IBM Corp., Poughkeepsie, NY*
Andrew Bianchi - *IBM Corp., Austin, TX*
Richard Wachnik - *IBM Corp., Poughkeepsie, NY*
James Warnock - *IBM Corp., Yorktown Heights, NY*
Derrick Smith - *IBM Corp., Austin, TX*

5.2 Standard Cell Power and Signal EM Qualification Methodology (1:45)
Yau Kok Lai, Foong Tek Chan, Yin Hao Liew - *BaySand Inc., Penang, Malaysia*
Sankar Ramachandran - *ANSYS, Inc., Bangalore, India*

5.3 Fast On-Die Statistical Thermal Hotspot Analysis: Considering Local Statistical Variations (2:00)
Palkesh Jain, Manoj Mehrotra - *Qualcomm India Pvt. Ltd., Bangalore, India*

5.4 Transient Thermal Analysis Flow for Digital and Analog IPs in Gate-level and Transistor-level (2:15)
Yonghwan Kim - *Samsung Electronics Co., Ltd., Seoul, Republic of Korea*
Joohee Choung, Wook Kim, Kyungtae Do - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*

5.5 Novel power grid structures for a wire bonded chip (2:30)
Marc DeWilde - *Texas Instruments, Inc., Plano, TX*
Jason Hoff - *Texas Instruments, Inc., Woodruff, WI*

5.6 Experimental Characterization of Workload-induced Logic States on Chip Leakage Power of a Server Class Microprocessor (2:45)
Arun Joseph, Rahul Rao, Anand Haridass - *IBM Systems and Technology Group, Bangalore, India*
Spandana Rachamalla - *IBM Corp., Bangalore, India*
Diyanesh B. - *IBM Systems and Technology Group, Bangalore, India*

Q&A Poster Session
Monday, June 6 5:00 - 6:00pm - Exhibit Floor

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6 IP TRACK: MIPI ALLIANCE AND IP: A PERSPECTIVE FOR THE MOBILE AND MOBILE-INFLUENCED MARKETS

Time: 1:30pm - 3:00pm || Room: Ballroom G || Event Type: Embedded Tutorial || Track: IP, Design
Topic Area: General Interest, Business

CHAIR:
Claude Moughanni - *Lattice Semiconductor Corp., San Jose, CA*
ORGANIZER:
Peter Lefkin - *MIPI Alliance, Flemington, NJ*

This tutorial will provide attendees with:

1) An overview of MIPI Alliance

2) MIPI Specification Framework and Roadmap, and

3) A technical tutorial on two of MIPI Alliance's most widely adopted specifications (Camera and Display), and two of MIPI Alliance's newest specifications (Audio and Sensor).

Three principles adhered to in the development of MIPI Specifications include: Low Power, High Bandwidth and Low EMI. Developers and managers who are interested in the ever-expanding world of mobile and mobile-influenced devices need to leverage the ecosystem of technology interfaces for their designs.

SPEAKERS:
Peter Lefkin - *MIPI Alliance, Flemington, NJ*
Hezi Saar - *Synopsys, Inc., Mountain View, CA*
Sachin Dhingra - *Cadence Design Systems, Inc., San Jose, CA*

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7 DESIGN TRACK: EFFECTIVE USE OF A MEMORY PROTECTION UNIT (MPU) IN SAFETY-CRITICAL C/C++ CODE

Time: 3:30pm - 5:00pm || Room: Ballroom E || Event Type: Embedded Tutorial
Track: Embedded Systems, Automotive || Topic Area: System Software, System Architectures & SoC

A memory protection unit (MPU) is a hardware module present in some microcontrollers, to enable software to control access to areas of physical memory known as regions. These regions can vary in size and typically can be as small as 32 bytes, in modern MPUs. Current approaches to use an MPU in an RTOS environment do not have enough flexibility to leverage this small region size granularity, to provide more effective data protection at the data object level or even at the software component level. The set of memory areas (regions) that a given application thread (task) is supposed to access may be different at different points in the execution of the thread, and it depends on the software components that the thread invokes.

This tutorial will teach a new approach for using modern MPUs more effectively in C/C++ code. This approach is based on component-level and object-level data protection. Concrete code examples for the Kinetis MPU and the ARMv7-M MPU will be presented.

SPEAKER:

German Rivera - *NXP Semiconductors, Austin, TX*

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8 DESIGN TRACK: DESIGN CHALLENGES IN IOT WORLD

Time: 3:30pm - 5:00pm || Room: Ballroom F || Event Type: Invited Presentations
Track: Design, IoT || Topic Area: Circuit Design, General Interest

CHAIR:

Yiyu Shi - *Univ. of Notre Dame, IN*

ORGANIZER:

Yiyu Shi - *Univ. of Notre Dame, IN*

The Internet of Things (IoT) has become a major driving force behind technology innovations spanning multiple disciplines. By connecting multiple IP addressable physical objects embedded with electronics, software, sensors and connectivity, it achieves smart, reliable and secure services. It connects many different concepts and applications at different scales, including but not limited to batteries, wearable devices, cameras and surveillance, education, logistics, transportation, building, autos and power grids. This session includes three talks from leading research groups in academia and industry, showcasing various cutting-edge silicon designs that push IoT forward. The first talk features an interesting single layer 3D touch sensing system. The second talk shows a creative 28 nm high speed range SRAM design for large-scale machine learning in hardware, enabling compact smart devices. The last talk addresses the topic of energy issue of the IoT. Here is an interesting idea about how to use the natural signal as the energy of event trigger in the application of environment monitoring. That will be an answer to eliminate idle loop power consumption of IoT devices.

8.1 Airtouch: A Novel Single Layer 3D Touch Sensing System for Human/Mobile Devices Interactions (3:30)
Li Du - *Univ. of California, Los Angeles, CA*
Albert Liu, **Kye Cheung** - *Kneron, San Diego, CA*

8.2 A 2.2 GHz SRAM with High Temperature Variation Immunity for Deep Learning Application under 28nm (4:00)
Chun Chen Liu, Yen-Hsiang Wang, YiLei Li, Chien-Heng Wong, Tien Pei Chou - *Univ. of California, Los Angeles, CA*
Young-Kai Chen - *Bell Labs, Murray Hill, NJ*
M.-C. Frank Chang - *Univ. of California, Los Angeles, CA*

8.3 Wireless sensor nodes for environmental monitoring in Internet of Things (4:30)
Tzi-Cker Chiueh, Li-Ren Huang - *Industrial Technology Research Institute, Hsinchu, Taiwan*

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9 IP TRACK: LOW POWER IP

Time: 3:30pm - 4:00pm || Room: Ballroom G || Event Type: Reviewed Presentations
Track: IP, IP || Topic Area: Low-Power & Reliability

CHAIR:

Farzad Zarrinfar - *Mentor Graphics Corp., San Jose, CA*

Join us as we explore how the "Impact of Leakage & biasing on Power in 22FDX Process" and how "Analog Driven Power Estimation for Mixed Signal IPs" matter to IP designers today.

9.1 Impact of Leakage & biasing on Power in 22FDX Process (3:30)
Krishnan Subramanian, Nagaprasad Ponna, Tirumala Srikanth Singari - *INVECAS, Inc., Bangalore, India*
Sankar Ramachandran - *Apache Design, Inc., A Subsidiary of ANSYS, Inc., Bangalore, India*

9.2 Analog Driven Power Estimation for Mixed Signal IPs (3:45)
Shovan Maity, Rupak Ghayal, Santosh Nene, Babu Ramki S. - *Intel Corp., Bangalore, India*

Q&A Poster Session
Monday, June 6 5:00 - 6:00pm - Exhibit Floor

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10 IP TRACK: MINIMIZING SOC POWER CONSUMPTION: A TOP DOWN DESIGN METHODOLOGY OR BOTTOMS UP STARTING WITH PROCESS SELECTION PROBLEM?

Time: 4:00pm - 5:00pm || Room: Ballroom G || Event Type: Panel || Track: IP, Design
Topic Area: Low-Power & Reliability, General Interest, Codesign & System Design

MODERATOR:
Ann Mutschler - *Semiconductor Engineering, Louisville, KY*

ORGANIZER:
Farzad Zarrinfar - *Mentor Graphics Corp., Fremont, CA*

In this panel, implementation techniques and tradeoffs for designing ultra low-power SOCs, ASSPs, and ASICs will be discussed. These techniques are critical for battery-powered devices, and other devices that are sensitive to thermal management as well as reduction of packaging cost. IP suppliers and EDA vendors now offer low-power IPs as well as advanced high-level design methodology and emulation to estimate, optimize and synthesize from C/C++/SystemC to RTL. Topics such as FinFET and FDSOI processes for low voltage applications will be compared with planar CMOS. Optimization of these advance techniques for various applications such as portable gaming, IOT, automotive, sensor hub, 5G/LTE wireless, networking, portable multimedia, wearable computing will be discussed. Low power techniques are paramount for gaining and keeping market share.

PANELISTS:
Aditya Mukherjee - *Microsoft Corp., Mountain View, CA*
Saurabh Kumar Shrimal - *Mentor Graphics (India) Pvt. Ltd., Noida, India*
Carlos Mazure - *SOI Industry Consortium & Soitec, Grenoble, France*
Ronald Martino - *NXP Semiconductors, Austin, TX*
Lluis Paris - *Taiwan Semiconductor Manufacturing Co., Ltd., San Jose, CA*

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DESIGN/IP TRACK POSTER SESSION

Time: 5:00pm - 6:00pm || Room: Exhibit Floor || Event Type: Poster Session || Track: Design, IP
Topic Area: General Interest

During the poster presentation, you will interact directly with poster presenters in a small group setting.

As the limited time available in the Design/IP Track session program was exceeded by the quantity of great submitted content, we present the following posters in the Design/IP Track Poster Session held Monday, June 6 from 5:00 to 6:00pm on the Exhibit Floor.

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11.1 Ad-libbing for socv: A 28nm multi-track LIBRARY Characterization/QC experience
Krishna Panda - *Texas Instruments, Inc., Plano, TX*

11.2 Impact of Package Parasitics on Power Noise for Automotive Designs
Steven Watkins - *NXP Semiconductors, Austin, TX*
Kaushal Kishore - *ANSYS, Inc., Austin, TX*

11.3 Thermal-Aware EM Methodology
Imran Qureshi - *Centaur Technology, Austin, TX*
Kartik Iyer - *ANSYS, Inc., Austin, TX*

11.4 Physical planning of IO interface for 3D stacking of packaged devices
Sirpi Srinivasan - *Open-Silicon, Inc., Milpitas, CA*

11.6 An on-chip level analysis method based on geometric information for EMI-aware design
Dongchul Kim, Sungwook Moon, Bo Pu, Jinho Kim - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

11.7 Layout density verification for seam-less Hard-IP Integration
Samichi S., Madan Lal - *Intel Corp.& Intel Technology India Pvt. Ltd, Bangalore, India*

11.8 Full-Featured Debug Cross Triggering
Eric Rentschler - *Mentor Graphics Corp., Steamboat Springs, CO*

11.9 Hierarchical Power and IR Drop Analysis for Mega-Size Mixed-Signal Design
Ralph Chen, Allen Gu, Kitty Chen - *Semiconductor Manufacturing International Corp., Shanghai, China*
Xinggang Liu, Xiaoli Chen, Xiaolu Liu, Qianyi Zhang - *Cadence Design Systems, Inc., Shanghai, China*

11.11 Supply Noise Induced On-Chip Jitter Analysis
Taehoon Kim - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Sunny Arora - *ANSYS, Inc., Noida, India*
Yonghyun Kang - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Daehyun Jung - *ANSYS, Inc., Seoul, Republic of Korea*
Seonha Lee - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

11.12 Effective Power Grid design using Redhawk-GPS
Ravi Sankar Kerla - *Broadcom Corp., Banglore, India*

DESIGN/IP TRACK POSTER SESSION

11.13 System level Signal Integrity effects from shared supply for DRAM and NAND devices
Cornelia R. Golovanov - *Seagate Technology, LLC, Allentown, PA*
Pritesh Pawaskar - *Seagate Technology, LLC, Pune, India*
Chris Ortiz - *ANSYS, Inc. & Apache Design, Inc., A Subsidiary of ANSYS, Inc., San Jose, CA*

11.14 Optimizing existing PDN to recover area of SoC in Production
Abhishek Nigam - *STMicroelectronics & HCL Technologies, Noida, India*
Anant Narain - *Apache Design, Inc., A Subsidiary of ANSYS, Inc., Noida, India*
Fabrizio Viglione - *STMicroelectronics, Crolles, France*
Shiv Om Sharma - *STMicroelectronics, Greater Noida, India*
Atul Bhargava - *STMicroelectronics, Greater Noida, India*

11.15 Using an Accurate Multi-Mode Chip Power Model to Analyze Power Integrity Differences between On-Board Voltage Regulator Modules (VRMs) and In-Package Integrated Voltage Regulators (IVRs)
Ashwin Chintaluri - *Georgia Institute of Technology, Atlanta, GA*
Harish Gopalakrishnan - *Oracle Labs, Austin, TX*
Hesam F. Moghadam - *Oracle Labs, Belmont, CA*
Chris Ortiz - *ANSYS, Inc., Austin, TX*

11.16 An Approach for Early Detection of Power Issues and Automation of UPF Flow
Anusha Renduchinthala, Surat S. Devulapalli, Mohita Batra, **Akhilesh Chandra Mishra**, Rangarajan Ramanujam - *STMicroelectronics, Greater Noida, India*
Sujay Deb - *Indraprastha Institute of Information Technology, Delhi, India*

11.17 Managing Complex Hierarchical Design Data
Greg Ford - *GLOBALFOUNDRIES, Santa Clara, CA*
Bertram L. Bradley - *GLOBALFOUNDRIES, Austin, TX*

11.30 SW/FW Automated Test Framework and Debug Toolkit for System Testing
Horace Chan, Brian Vandergriend - *Microsemi Corp., Burnaby, BC, Canada*

11.31 The clock is ticking: Are the clocks alive?
Ayon Dey, **Praveen Wadikar**, Kamal Jeet - *NVIDIA Corp., Bangalore, India*

11.32 Consistency maintenance and change propagation in System on Chip development
Aurélien Chichignoud - *STMicroelectronics & CEA-LIST, Grenoble, France*
Florian Noyrit - *CEA-LIST, Gif-sur-Yvette, France*
Laurent Maillet-Contoz - *STMicroelectronics, Grenoble Cedex, France*
Francois Terrier - *CEA-LIST, Gif sur Yvette, France*

11.33 Case Study: Transition from VHDL to UVM Testbench for FPGAs
Shaela Rahman - *Baker Hughes Inc., Houston, TX*

11.34 Power Management in 28nm SOC using Temperature Compensated Adaptive Voltage Scaling
Jose Flores, Shenghe Zhao - *Texas Instruments, Inc., Dallas, TX*

11.35 RTL Power Estimation and Reduction for Block and Clock Tree Optimization
Mark Silla - *Advanced Micro Devices, Inc., Austin, TX*

11.36 Design, Verification and Emulation of an Island-Based Network Processor
Ron Swartzentruber - *Netronome, Boxborough, MA*

11.37 Reaching Coverage Closure with Formal
Doug Smith - *Mentor Graphics Corp., Austin, TX*

11.38 Automated UVM Testbench for State Machine Verification
Kiruthika C., Deepak Kumar EV, Ranganath Kempanahally - *elitePLUS Semiconductors Technologies Pvt Ltd., Bangalore, India*

11.39 RTL Power Reduction for IEEE 802.11ad WiGig® Chipset
Craig Farnsworth, Simon Chan - *Peraso Technologies Inc., Toronto, ON, Canada*

11.40 Coverage Analysis for Power Scenarios
Lakshminarayana Kamarthi, Jianfeng Liu, Kyungtae Do, Young Duk Kim, Jinpyo Park - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Vikas Tyagi, Saurabh Kumar Shrimal, Mohammed Fahad - *Mentor Graphics (India) Pvt. Ltd., Noida, India*

11.41 Formal Methodology of Validating Dynamic Clock Gating Scheme using Hierarchical flow
Manik Tyagi, Deepak Jindal, Maruthi Srinivas Narasimhan - *Qualcomm India Pvt. Ltd., Bengaluru, India*
Mahesh Parmar - *Synopsys India Pvt. Ltd., Bengaluru, India*
Sudipta Kundu - *Synopsys, Inc., Hillsboro, OR*

11.42 Agile Chip Level Verification Of Non-Mainline Functions With An Enhanced Modularity Approach
Matteo Michel - *IBM Deutschland Research & Development GmbH, Chemnitz, Germany*

11.43 A Framework for Parameter Verification Gap Analysis in SoC Design
Prokash Ghosh, Siddhant Kumar - *NXP Semiconductors & Freescale Semiconductor, Inc., Noida, India*
Arup Chakraborty - *NXP Semiconductors & Freescale Semiconductor, Inc., Austin, TX*

11.44 A Practical Application of Combinatorial Testing in EDA
Hong Yang, David Newmark - *Advanced Micro Devices, Inc., Austin, TX*

11.45 Many-Core Distributed Platform: The Road to Graceful Hardware
Nizar Dahir, **Pedro B. Campos**, Colin Bonney, Martin Trefzer, Andy M. Tyrrell, Gianluca Tempesti - *Univ. of York, United Kingdom*

MONDAY TUTORIALS

T1

TUTORIAL 1: MODEL-BASED DESIGN AND ANALYSIS OF AUTOMOTIVE CYBER PHYSICAL SYSTEMS

Time: 10:30am - 12:00pm || Room: 12AB || Event Type: Monday Tutorial
Track: Automotive, Embedded Systems || Topic Area: Cyber-Physical Systems, Codesign & System Design, Modeling, Simulation & Timing

ORGANIZERS:

Dip Goswami - *Eindhoven Univ. of Technology, Eindhoven, The Netherlands*
Mohammad Abdullah Al Faruque - *Univ. of California, Irvine, CA*
Arne Hamann - *Robert Bosch GmbH, Renningen, Germany*

Typical automotive architectures consist of over 100 ECUs (electronic control units) communicating over a system made up of several buses and gateways implementing different protocols such as FlexRay, CAN, Ethernet etc. Scheduling policies and parameters need to be specified for the ECUs and the buses. Control applications are designed using a model-based approach using Matlab/Simulink targeting such architectures. Controller synthesis problems subject to take into account platform-specific properties.

In particular, the timing constraints derived from the control design need to be translated into platform constraints to be satisfied by the control-related tasks and messages. In practice, the controller and its embedded implementation design are often performed in isolation. As pointed out by some of the recent research results, such design isolation often results in large resource over-dimensioning which is critical for cost-sensitive automotive domain.

One essence of cyber-physical design paradigm is to bridge the gap between control theory and their embedded implementations by so-called control/architecture co-design. A large body of recent works has shown potential benefit of such co-design approach. In this tutorial, we will illustrate several co-design procedures for the automotive cyber-physical systems where the control designs are in sync with the implementation architecture and the architecture design efficiently accommodates all control performance specifications.

The first part of the tutorial will talk about automotive E/E architectures. On computation side, typical ECUs and the real-time operating systems will be covered. On networking side, various communication bus protocols such as Ethernet and CAN will be discussed. Based on this, it will be illustrated how the performance of automotive E/E architecture is evaluated (using formal analysis and simulation) in the current state of practice. Finally, current research challenges will be illustrated with a number of examples.

The second part of the tutorial will talk about various control/architectures co-design procedure to perform various trade-off analysis between resource usage and control performance. In particular, we will illustrate how a richer sampling scheme can be exploited to enable trade-off between the resource and performance with various automotive use-cases.

The third part of the tutorial will talk about control and battery management system (BMS) co-design in an Electric Vehicle (EV). To be particular, we will focus on the battery lifetime and efficiency as the design constraints in view of an industrial use-case of EV climate control. This part will discuss how the abstraction and complexity of the modeling are important and how it may affect the control functionality in terms of performance, computation, and memory resource requirements.

SPEAKERS:

Arne Hamann - *Robert Bosch GmbH, Renningen, Germany*
Dip Goswami - *Eindhoven Univ. of Technology, Eindhoven, The Netherlands*
Mohammad Al Faruque - *Univ. of California, Irvine, CA*

**Tutorials require special registration.*

T2 TUTORIAL 2: LINUX PORTING, BRING UP AND DRIVER DEVELOPMENT

Time: 10:30am - 12:00pm || Room: 13AB || Event Type: Monday Tutorial
Track: Embedded Systems, Design || Topic Area: System Software, System Architectures & SoC, Codesign & System Design

ORGANIZER:

Larry Lapides - *Imperas Software Ltd., Dublin, CA*

Key topics: Linux for embedded systems, including SMP Linux. Driver development for Linux, both static and dynamic (Loadable Kernel Modules, or LKMs) drivers. Testing of Linux and drivers.

Linux has become the general purpose operating system of choice for embedded systems, and is almost always supported for high end SoCs developed by the semiconductor vendors. Most vendors use the open source Linux distribution, then build a custom distribution representing the device tree supported for the specific SoC, and including the necessary drivers for the peripherals on the SoC, as well as supporting other customizations and unique features. The operating system is complicated further with multicore processors and symmetric multiprocessor (SMP) Linux. Just because everyone supports Linux, does not make porting and bring up an easy task. To put it another way: Just because you get to the Linux prompt doesn't mean everything is working.

This tutorial will be presented in three sections. In the first section (by Imagination Technologies), the various components of bringing up Linux on a new platform will be covered. These include the Bootrom, U-boot bootloader, Linux Kernel and Linux Buildroot. A walk-through of bringing up Linux on new hardware will be presented. The walk-through will also introduce the various tools used to assist in completing board bring-up easily.

Driver development is the focus of the second section of the tutorial (Posedge Software). An overview of development of both static and dynamic drivers (Loadable Kernel Modules, or LKMs) will be covered. A virtual platform environment will be used to highlight key points in the development methodology, including co-debug of driver software and peripheral hardware models.

The final section (Imperas) will discuss the development of a robust test environment using the virtual platform technology. The virtual platform provides a complementary approach to porting and bring up on hardware. The benefits of controllability, observability and repeatability for virtual platform use will be covered. Specific OS-aware tools will also be highlighted, plus other tools such as non-intrusive memory monitors and the use of software assertions and code and functional coverage techniques for the operating system and drivers.

SPEAKERS:

Zubair Lutfullah Kakakhel - *Imagination Technologies Ltd., Leeds, United Kingdom*
Henry Von Bank - *Posedge Software, Inc., Rogers, MN*
Simon Davidmann - *Imperas Software Ltd., Thame, United Kingdom*

T3 TUTORIAL 3: INFLECTIONS IN PHYSICAL DESIGN: PAST, PRESENT & FUTURE

Time: 10:30am - 12:00pm || Room: 15 || Event Type: Monday Tutorial || Track: EDA, Design
Topic Area: Physical Design

System-on-chip (SoC) complexity has been steadily growing in the last several years due to ever increasing design integration and relentless pursuit of Moore's law by the semiconductor industry. Especially, the mobile SoCs and server class SoCs have gone through huge transformations in their capabilities in the last decade or so. This has led to many innovations in designing and implementing the IPs that make up the systems.

The EDA industry has kept up with the pace and some companies have recently launched major tool changes that offer higher capacity, turn-around-time and many advanced features that are needed for finfet and multi-patterning process generations. In this tutorial, we will discuss how physical design has evolved so far to meet the demand, and our vision for addressing the needs of designers in the years to come.

SPEAKERS:

Raj Sambandam - *Intel Corp., Folsom, CA*
Vivek Rajan - *Intel Corp., Hillsboro, OR*

**Tutorials require special registration.*

T4 TUTORIAL 4: OVERCOMING CHALLENGES OF FPGA PROTOTYPING

Time: 10:30am - 12:00pm || Room: 19AB || Event Type: Monday Tutorial
Track: EDA, Design || Topic Area: Test & Verification, System Software

ORGANIZER:

Rob van Blommestein - *S2C, Inc., San Jose, CA*

Due to both simulation speed and modeling accuracy limitations, designers are increasingly finding it difficult to rely only on software simulations to verify that their hardware design is correct. Running your SoC design on a FPGA prototype is the most reliable way to ensure that your design is functionally correct.

Early software and/or firmware development on FPGA prototypes, pre-silicon, has become more important as many unforeseen software bugs stem from the complexity of integrating operating system (OS), applications, and hardware. An at-speed FPGA prototype allows for many extra months of rigorous software development and testing at the crucial software-hardware integration stage.

FPGA prototyping is also critical if your SoC design utilizes many commercial IPs making prototyping on FPGAs the most reliable method to ensure all these IPs work well together.

FPGA prototypes can also be used as demo platforms to the SoC customers for getting them interested in the chip you build and allow you to work with them on improving features before chip tape-out.

However, FPGA prototyping does come with some challenges: Long Bring-Up Time Performance Reusability Design Partitioning Debug-ability.

This tutorial will show how designers can address these challenges and utilize FPGA prototyping to reach success. Real-word case studies will be explored to exemplify specific ways how FPGA prototyping can be optimized.

SPEAKERS:

Mon-Ren Chene - *S2C, Inc., San Jose, CA*
Bruno Bratti - *Wave Computing, Campbell, CA*
Allen Sha - *M31 Technology Corp., Santa Clara, CA*

T5 TUTORIAL 5: TAMING THE DARK HORSE: VOLTAGE-MARGIN MINIMIZATION FOR MODERN "REAL-WORLD" ENERGY-EFFICIENT COMPUTING

Time: 10:30am - 12:00pm || Room: 17AB || Event Type: Monday Tutorial
Track: Design, IP || Topic Area: Circuit Design, Physical Design, System Architectures & SoC

ORGANIZER:

Visvesh Sathe - *Univ. of Washington, Seattle, WA*

The past decade has seen a great deal of attention and effort focussed on circuits, architectures and methodologies for energy-efficient and low power computing across a broad range of applications from ultra-low power devices to high-end servers. As designers continue to seek and evaluate low power technologies to enable the next generation of computing, the traditionally unheralded problem of voltage margin minimization has emerged to become one of the most significant sources of inefficiency and dissipation. Real-world integrated systems are margined, or guard-banded to address many sources of noise and variability including process, temperature, aging, and supply voltage noise and offsets.

The trend toward multiple, fine-grained voltage domains, and aggressively voltage-scaled systems has exacerbated the problem. Voltage-margin minimization is a central component of modern low power design. Indeed, many recent low power efforts in the industry have moved beyond methodology and circuit design to address voltage margin minimization! In this tutorial, we propose a modern treatment of low-power design by actively managing supply-voltage variations. In contrast with text-book approaches, we examine a blend of well-established and emerging solutions that have proven to be effective in real-world constrained systems.

The tutorial is organized in two parts. In the first, we begin by analyzing the main contributors toward voltage margins, including practical sources that are related to IC test and product deployment. We closely examine the source of voltage supply noise in particular, the dominant source of voltage margining, presenting the power delivery network of the dual-core 64bit ARM Cortex-A57 platform as a case study. We then discuss a variety of circuit-architecture techniques used to directly and indirectly reduce voltage supply noise margins. High-density decap technology, active decap, supply-resonance avoidance, operation-throttling and adaptive clocking techniques to mitigate supply voltage noise. We also examine techniques adopted to address process and temperature variability in modern systems through the use of Critical Path Monitors (CPM) circuits, and the Razor architecture. These techniques will be presented in the context of production designs and their constraints for a system-aware treatment of the subject.

In the second section, we focus on Integrated Voltage Regulation (IVR) circuits. As designers grapple with more aggressive voltage scaling in the presence of supply variation, Integrated Voltage Regulation (IVR) has emerged as the key to achieving fine spatio-temporal control of SoC supply voltages. IVR has already been deployed for energy-efficient operation in high-performance systems (Intel Haswell), and the trend to incorporate IVR to support finer voltage domains continues. We examine recent developments and challenges in the area of integrated voltage regulation across the three major voltage regulator technologies: switching-inductor converters, switched-capacitor converters, and low-dropout (linear) regulators.

This tutorial provides an overview of low power circuit and architecture techniques with a system-level context. It is designed to be readily accessible to graduate students and practicing engineers alike, with a blend of well-established and emerging approaches to low power design.

SPEAKERS:

Visvesh Sathe - *Univ. of Washington, Seattle, WA*
Shidhartha Das - *ARM Ltd., Cambridge, United Kingdom*

**Tutorials require special registration.*

T6

TUTORIAL 6: ADVANCES IN POST SILICON DIAGNOSIS TECHNOLOGIES IN NANO-SCALE ERA

***PART 1:* Time: 1:30pm - 3:00pm || Room: 12AB**
***PART 2:* Time: 3:30pm - 5:00pm || Room: 12AB**
Event Type: Monday Tutorial || Track: EDA, Design || Topic Area: Test & Verification, Emerging Technologies, Lithography & DFM

ORGANIZER:

Enamul Amyeen - *Intel Corp., Hillsboro, OR*

Post Silicon diagnosis drives the isolation of manufacturing defects and provides feedbacks for process improvement and is critical for enabling Moore's law and semiconductor technology scaling. Due to the increasing complexity of nano-scale manufacturing fabrication, the need for faster root-cause of issues is essential for volume production ramp to meet the product time to market demand.

Over the last several years, many innovations have been made and novel solutions are emerging for better and faster defect isolation. With the advent of new transistor devices, lithography, and fabrication processes, the demand for improving the defect isolation and faster yield learning will continue to grow in coming years.

In this tutorial, we will review the basics of diagnosis approaches, and advancements in post silicon diagnosis field.

In addition to diagnosis quality improvement, increased focus has been made to volume processing of diagnosis results for yield learning. This has resulted in introduction of new DFT technologies to obtain and process massive amount of fail data, and to provide better controllability and observability of failures to narrow down the defect suspects. Diagnosis algorithms are optimized to provide speed-ups in analysis time. Advancements are made in fault modeling to abstract the complex defect behavior and logical analysis of failures are being incorporated with layout analysis for finer pruning of diagnosis candidates. Hybrid approach of using logical simulation in conjunction with circuit simulation resulted in better isolation of front end and backend defects.

Along with diagnosis technology improvements, complementary efforts have been geared towards customized test content to improve diagnostic resolution. We will review emerging techniques of learning based diagnosis approach which combining with process sensitivity, DFM constraints, and lithography simulation will be the key for driving the innovations for future technology generations.

The tutorial is intended for engineers and test practitioners including academics working in test and diagnosis, post silicon debug, fault isolation, failure analysis, and manufacturing yield. The DAC audience will get the opportunity to know the state of the art diagnosis technologies, and how they are shaping the design and process evolution and manufacturing yield learning in nano-scale era.

SPEAKERS:

Shawn Blanton - *Carnegie Mellon Univ., Pittsburgh, PA*
Enamul Amyeen - *Intel Corp., Hillsboro, OR*
Srikanth Venkataraman - *Intel Corp., Hillsboro, OR*

T7

TUTORIAL 7: THE CONTINUING ARMS RACE: A JOURNEY IN THE WORLD OF RUNTIME EXPLOITS AND DEFENSES

***PART 1:* Time: 1:30pm - 3:00pm || Room: 13AB**
***PART 2:* Time: 3:30pm - 5:00pm || Room: 13AB**
Event Type: Monday Tutorial || Track: Security || Topic Area: System Software

ORGANIZER:

Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*

Today we are facing an increasing dependency of our lives on IT systems. The rapidly growing number of electronic devices of different form factors, vast number of applications and services and the desire for continuous connectivity has significantly increased both the software complexity and the cyberattack surface, as millions of lines of codes are generated that can be potentially vulnerable.

In this context, memory corruption attacks play a vital role. They have been persisting more than three decades and constitute a pre-dominant attack vector on diverse computing platforms. Further, they are increasingly launched against mobile and embedded devices.

While traditional attacks required the attacker to inject malicious code into the memory space of an application, modern attacks only reuse existing code. For instance, return-oriented programming combines small code pieces to generate malicious programs based on benign program code. Consequently, these attacks are highly challenging to detect, and apply to Harvard-based architectures because no malicious code needs to be injected. Traditional exploit mitigation defenses such as data execution prevention and memory randomization cannot stop these attacks.

However, a number of advanced defenses based on control-flow integrity, code pointer integrity, and fine-grained memory randomization have been recently proposed; some of them are based on hardware software co-design principles to increase both efficiency and effectiveness.

In this tutorial, we provide an overview of the state-of-the-art memory exploitation techniques and defenses. We start with the main principles of memory exploitation covering stack smashing, return-into-libc, and return-oriented programming. Next, we present modern defense techniques such as control-flow integrity and memory randomization. In particular, we present and discuss hardware-based defense techniques in this area of which some have been recently incorporated into modern processors. In the second part of this tutorial, we continue with a hands-on lab where attendees will have the opportunity to construct proof-of-concept memory exploits.

SPEAKERS:

Lucas Davi - *Technische Univ. Darmstadt, Germany*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*

**Tutorials require special registration.*

T8

TUTORIAL 8: HOW PORTABLE STIMULUS ADDRESSES KEY VERIFICATION, TEST REUSE, AND PORTABILITY CHALLENGES

***PART 1:* Time: 1:30pm - 3:00pm || Room: 15**
***PART 2:* Time: 3:30pm - 5:00pm || Room: 15**
Event Type: Monday Tutorial || Track: EDA, Design || Topic Area: Test & Verification, System Software, Emerging Technologies

ORGANIZERS:

Tom Anderson - *Breker Verification Systems, Inc., San Jose, CA*
Larry Melling - *Cadence Design Systems, Inc., San Jose, CA*

Portability of reusable test cases has long been a goal for semiconductor verification and validation teams. No one wants to "reinvent the wheel" by having to rewrite similar tests again and again. The widely accepted Accellera Universal Verification Methodology (UVM) standard enabled reuse of testbench components and constrained-random tests at the IP and block level, but limitations in terms of reuse at subsystem and full-chip level, and lack of portability across execution platforms, required a fresh look at addressing the portable stimulus and test challenge.

The upcoming Accellera portable test and stimulus standard (PSS) specification will permit the creation of a reusable model for a variety of users across different levels of integration under different configurations. This model will enable the generation of different test implementations for multiple execution platforms, including IP simulation, full system-on-chip (SoC) simulation, emulation, FPGA prototyping, and silicon. With such a standard in place, EDA vendors can produce tools that automatically generate stimulus, results checks, and coverage metrics tuned for a particular target platform.

This tutorial will examine unique portable stimulus challenges such as linking verification to diagnostics and software, portability to every platform, and resource management.

The tutorial will outline a set of common usage examples that emphasize specific verification, reuse, and portability challenges. Verification challenges include randomization of both data and control flow. Reuse challenges include migrating tests from IP level to SoC. Portability challenges include growing tests to improve coverage when running on faster platforms and executing at the full platform speed. Finally, the tutorial will show how portable stimulus can address the usage examples.

Attendees will learn:
- Unique challenges for a portable stimulus solution
- How a PSS model can capture complex use cases
- How a PSS model enables automation
- How a PSS model can leverage existing low-level sequences or drivers
- How a PSS model enables execution of tests across multiple platforms
- How coverage is defined within a PSS model

SPEAKERS:

Faris Khudakjie - *Intel Corp., Hudson, MA*
Adnan Hamid - *Breker Verification Systems, Inc., San Jose, CA*
Tom Fitzpatrick - *Mentor Graphics Corp., Wilsonville, OR*
Steve Chappell - *Synopsys, Inc., Mountain View, CA*
Sharon Rosenberg - *Cadence Design Systems, Inc., San Jose, CA*

**Tutorials require special registration.*

T9

TUTORIAL 9: ENERGY-EFFICIENT PROTOCOLS FOR THE INTERNET OF THINGS

***PART 1:* Time: 1:30pm - 3:00pm || Room: 19AB**
***PART 2:* Time: 3:30pm - 5:00pm || Room: 19AB**
Event Type: Monday Tutorial || Track: IoT, Embedded Systems
Topic Area: Cyber-Physical Systems, Codesign & System Design, Emerging Technologies

ORGANIZER:

Ibrahim Elfadel - *Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates*

The Internet of Things has become the Internet of Everything and the Internet of All Things. It is predicted that by the end of 2020, the number of smart objects globally connected will reach 212 billions. Machine-to-machine (M2M) internet traffic is expected to reach up to 45% of all internet traffic. By its universal and all-inclusive nature, IoT growth over the past 5 years has been enabled by the development, design, and implementation of a heterogeneous set of data communication architectures.

In its simplest and most direct form, the IoT communication stack is comprised of three layers: the sensor/actuator layer, the network layer, and the service layer.

For each of these layers, many, sometimes too many, protocols and standards have been proposed and implemented with some being derived from existing networking and data communication protocols, including those of the Internet of People, while others are novel and meant to address the specific technical issues of the M2M internet.

The objective of this tutorial is to help the DAC audience make sense of the alphabet soup of platforms, protocols, standards, services, and architectures currently in use or under development for IoT.

The tutorial will take a holistic view of IoT with the goal of providing the attendees with the essential information needed to configure an IoT service, comprising a physical layer, a communication layer, and a software layer. Such configuration will of course depend on the IoT use case itself and several real-world use cases will be presented.

The content of this tutorial is as follows:

1. IoT market landscape: present and future business opportunities.
2. IoT architectures: from data to services.
3. IoT common standards: CoAP, MQTT, AMQO, DSS, HTTP, etc. Why is CoAP more energy-efficient than good old HTTP?
4. IoT technologies:
   a. Naming and addressing: EPC and IPv6
   b. Hardware platforms: Arduino, Rasberry PI, BeagleBone, etc.,
   c. Operating systems: Contiki OS, TinyOS, LiteOS, Android, iOS, etc.
5. IoT networking:
   a. Routing protocols for low-power and lossy networks: RPL.
   b. Physical layer: IEEE 802.15.4, 6LowPAN, BlueTooth Low Energy, ZigBee, EPCglobal, Z-wave, IEEE 802.11 (WiFi), Ethernet, MoCA, etc.
   c. Physical link metrics: energy-efficiency, data rate, footprint, M2M synchronization, clock-data recovery, etc.
   d. Emerging technologies: 5G, LoRA, sub-GHz, PIC, etc.
   e. IoT networking metrics: range, data rate, power, reliability, cost
6. IoT software platforms:
   a. Embedded systems
   b. Sensor fusion platforms
   c. Smart gateways
   d. And on to the cloud: Big Data and IoT
7. IoT use cases:
   a. Building automation
   b. Health and fitness
   c. Logistics
   d. Energy
8. IoT future challenges:
   a. Interoperability
   b. Mobility
   c. Scalability
   d. Security and privacy

Plenty of time will be allocated to Q & A.

SPEAKERS:

Ibrahim (Abe) Elfadel - *Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates*
Kwok Wu - *NXP Semiconductors, Austin, TX*

**Tutorials require special registration.*

T10

TUTORIAL 10: HOW TO BUILD IRRESISTIBLE 3D IC PHYSICAL LAYOUTS: TOOLS, METHODOLOGIES, AND CASE STUDIES

PART 1 (TSV-BASED 3D IC): Time: 1:30pm - 3:00pm || Room: 17AB
PART 2 (MONOLITHIC 3D IC): Time: 3:30pm - 5:00pm || Room: 17AB
Event Type: Monday Tutorial || Track: EDA, Design || Topic Area: Physical Design

ORGANIZER:

Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*

3D ICs, after a long wait, is now a reality. Through-silicon-vias (TSV) are found *inside* the bare dies of memory cube products, and they will soon find their ways to logic dies. Moreover, monolithic 3D IC (M3D) technology promises ultra-high density vertical integration that does not rely on micron-scale TSVs, thanks to its nano-scale monolithic inter-tier vias (MIV). This tutorial presents proven physical design and EDA technologies that produce high-quality power, performance, area (PPA), and reliability results for both TSV-based and monolithic 3D ICs.

Our target audiences includes:

(1) EDA vendors that will deliver much-needed 3D IC physical design tools,

(2) Design engineers who desire to build high-quality 3D IC layouts and architectures,

(3) Device engineers who want to offer optimized devices and interconnects for 3D ICs,

(4) Process engineers who are willing to work with designers to improve 3D IC yield and cost, and

(5) Managers who have the power to make it all happen.

SPEAKERS:

Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*
Dusan Petranovic - *Mentor Graphics Corp., Fremont, CA*
Moongon Jung - *Intel Corp., Santa Clara, CA*
Olivier Billoint - *CEA-LETI, Grenoble, France*
Deepak Nayak - *GLOBALFOUNDRIES, Santa Clara, CA*
Saurabh Sinha - *ARM Ltd., Austin, TX*

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*Tutorials require special registration.




TUESDAY, JUNE 7

VISIONARY TALK: LEARNING FROM LIFE: BIOLOGICALLY INSPIRED ELECTRONIC DESIGN

Lou Scheffer - *Howard Hughes Medical Institute, Chevy Chase, MD*

Time: 9:00am - 9:20am || Room: Ballroom A || Track: EDA, Design
Topic Area: General Interest, System Architectures & SoC

Modern electronics does amazing things, but biology routinely performs feats no current electronics can match. Every animal can learn on short timescales, defend against unforeseen threats, self-assemble and repair, all with great resilience. The shortest path to incorporating these features in our gadgets is to understand how biology works, then adapt these techniques to the semiconductor world. Towards this end, biologists are in the midst of reconstructing and understanding the entire nervous system of small animals, while device physicists and software folks work out the devices and algorithms that might duplicate or better what biology has long done. This talk will give an overview of the investigation into biological systems, and some hints, based on our current understanding, of how this might be incorporated into our electronic gizmos.

These techniques have the potential to add capabilities to our systems that are both different and more powerful, than those come from scaling and Moore alone.

Biography: Lou Scheffer got his degrees in EE from Caltech and Stanford, then did IC design for HP, followed by CAD software development at Cadence. Eight years ago, he switched fields to biology, where he now studies the structure and function of the brain. Working at the Howard Hughes Medical Institute, Lou is part of an effort using electron microscopy to reconstruct the detailed circuitry-every neuron and synapse - of the brain of the fruit fly. Lou is the author of numerous papers on EE, physics, SETI, and biology, plus two books, and 35 patents.

KEYNOTE: DRIVING THE NEXT DECADE OF INNOVATIONS IN VISUAL AND ACCELERATED COMPUTING

Sameer Halepete - *NVIDIA Corp., Santa Clara, CA*

Time: 9:20am - 10:00am || Room: Ballroom A || Track: Design, EDA
Topic Area: System Architectures & SoC, Circuit Design, General Interest

The ever-increasing performance demands of performance visual and accelerated computing has resulted in GPUs becoming some of the most complex ASICs being built today. These multi-billion transistor processors push design technologies to their limits and require incredibly robust implementation methodologies. At the same time, there are new performance demands from both the traditional source of gaming thanks to higher resolution displays and virtual reality applications as well as new GPU uses like deep learning and autonomous driving. While we've been able to ride the performance, power and cost gains from process scaling over the last two decades to deliver GPUs with ever increasing capabilities, this rate of process scaling improvement is slowing down. It is clear that the rate of innovations in the design implementation areas will need to pick up if we are to keep delivering performance gains to our customers at the historical rate. In this talk we'll cover the state of the art in visual and accelerated computing, the design approaches we use to implement these highly complex processors and finally propose ideas that will ensure that in spite of slowing process scaling, we're able to continue to deliver GPUs of ever-increasing capabilities over the next decade.

Biography: Sameer Halepete is the Vice President of VLSI Engineering at NVIDIA Corporation. He obtained his BTech degree in Electrical Engineering from the Indian Institute of Technology, Bombay in 1993 and his MS degree in Electrical Engineering from Stanford University in 1995. He joined Sun Microsystems' Advanced Development group in 1995 where he did research in ultra-low-threshold-voltage CMOS circuits. In 1996, he joined Transmeta Corporation where he worked on several generations of VLIW processors that enabled dynamic binary translation. He joined NVIDIA Corporation in 2002 to help build the company's first streaming multiprocessor based GPU which ushered the era of general purpose computing on graphics processors. In 2007, he became Vice President of ASIC Design and has since led several successful GPU projects and multiple successful collaborations with EDA companies to push the state of the art of graphics processors.

12 DESIGNER SOCS: IMPROVING PROCESSOR SYSTEMS

Time: 10:30am - 12:00pm || Room: 12AB || Event Type: Reviewed Presentations || Track: EDA
Topic Area: System Architectures & SoC

CHAIR:
Qi Zhu - *Univ. of California, Riverside, CA*
CO-CHAIR:
Andreas Herkersdorf - *Technische Univ. München, Germany*

This session gives new perspectives on processor systems. The first paper demonstrates that power and performance of one processor model can be inferred from performance counters of another. The second paper partitions shared cache resources in an integrated CPU-GPU system by observing that while some applications may not benefit from additional cache resources, allocating too few resources can degrade the performance of other concurrent applications. The third presentation proposes an improved memory-queue management for real-time applications. The final work introduces a debugging aid based on co-simulation.

*** Indicates Best Paper Candidate**

12.1 Accurate Phase-Level Cross-Platform Power and Performance Estimation* (10:30)
Xinnian Zheng, Lizy K. John, Andreas Gerstlauer - Univ. of Texas at Austin, TX

12.2 Latency Sensitivity-Based Cache Partitioning for Heterogeneous Multi-core Architecture (10:45)
Po-Han Wang, Cheng-Hsuan Li, Chia-Lin Yang - *National Taiwan Univ., Taipei, Taiwan*

12.3 Single-Tier Virtual Queuing: An Efficacious Memory Controller Architecture for MPSoCs with Multiple Realtime Cores (11:00)
Yang Song - *Univ. of California at San Diego, La Jolla, CA*
Kambiz Samadi - *Qualcomm Technologies, Inc., San Diego, CA*
Bill Lin - *Univ. of California at San Diego, La Jolla, CA*

12.4 Debugging and Verifying SoC Designs through Effective Cross-Layer Hardware-Software Co-simulation (11:15)
Keith A. Campbell, Leon He - *Univ. of Illinois at Urbana-Champaign, IL*
Liwei Yang - *Nanyang Technological Univ., Singapore, Singapore*
Swathi T. Gurumani, Kyle Rupnow - *Advanced Digital Sciences Center, Singapore, Singapore*
Deming Chen - *Univ. of Illinois at Urbana-Champaign, IL*

A Q&A poster session will immediately follow the presentations from 11:30am to 12:00pm.

13 MACHINE LEARNING FOR ANALOG CIRCUIT MODELING

Time: 10:30am - 12:00pm || Room: 19AB || Event Type: Reviewed Presentations
Track: EDA, Design || Topic Area: Modeling, Simulation & Timing

CHAIR:
Eric Keiter - *Sandia National Laboratories, Albuquerque, NM*
CO-CHAIR:
Zhuo Feng - *Michigan Technological Univ., Houghton, MI*

This session is devoted to the most recent machine learning algorithms for the development of statistical circuit models that can be used in performance estimation, yield analysis, and variation-aware design. The featured papers in this session use Bayesian and kernel-based techniques to address correlations, deviations from the Gaussian assumption, and nonlinear dependences.

*** Indicates Best Paper Candidate**

13.1 Efficient Performance Modeling via Dual-Prior Bayesian Model Fusion for Analog and Mixed-Signal Circuits (10:30)
Qicheng Huang, Chenlei Fang, Fan Yang, Xuan Zeng - *Fudan Univ., Shanghai, China*
Dian Zhou - *Univ. of Texas at Dallas & Fudan Univ., Dallas, TX*
Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*

13.2 Correlated Bayesian Model Fusion: Efficient Performance Modeling of Large-Scale Tunable Analog/RF Integrated Circuits* (10:45)
Fa Wang, Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*

13.3 Efficient Performance Modeling of Analog Integrated Circuits via Kernel Density Based Sparse Regression (11:00)
Chenlei Fang, Qicheng Huang, Fan Yang, Xuan Zeng - *Fudan Univ., Shanghai, China*
Dian Zhou - *Univ. of Texas at Dallas & Fudan Univ., Dallas, TX*
Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*

13.4 Relevance Vector and Feature Machine for Statistical Analog Circuit Characterization and Built-In Self-Test Optimization (11:15)
Honghuang Lin, Peng Li - *Texas A&M Univ., College Station, TX*

A Q&A poster session will immediately follow the presentations from 11:30am to 12:00pm.

14 PREVENTING AND EXPLOITING ERRORS

Time: 10:30am - 12:00pm || Room: 17AB || Event Type: Reviewed Presentations
Track: Embedded Systems, EDA || Topic Area: Low-Power & Reliability, System Architectures & SoC, General Interest

CHAIR:
Seokhyeong Kang - *Ulsan National Institute of Science and Technology (UNIST), Ulsan, Republic of Korea*

CO-CHAIR:
Miroslav Velev - *Aries Design Automation, LLC, Chicago, IL*

The four papers in the session present exciting recent work on fault tolerance and approximate computing. The first paper proposes a method for exploiting reliability-aware design to suppress aging. The second paper describes techniques for using statistical fault injection in order to evaluate the impact of timing errors on application performance with a case study for an OpenRISC core. The third paper presents an energy-efficient approximate serial encoding for sensor data, inspired by the T0 encoding technique for parallel buses. The fourth paper studies the use of clock overgating for designing approximate circuits.

*** Indicates Best Paper Candidate**

14.1 Reliability-Aware Design to Suppress Aging (10:30)
Hussam Amrouch - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Behnam Khaleghi - *Sharif Univ. of Technology, Tehran, Iran*
Andreas Gerstlauer - *Univ. of Texas at Austin, TX*
Jörg Henkel, **Victor M. van Santen** - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

14.2 Statistical Fault Injection for Impact-Evaluation of Timing Errors on Application Performance (10:45)
Jeremy Constantin - *École Polytechnique Fédérale de Lausanne, Switzerland*
Zheng Wang - *Nanyang Technological Univ., Singapore, Singapore*
Georgios Karakonstantis - *Queen's Univ. Belfast, United Kingdom*
Anupam Chattopadhyay - *Nanyang Technological Univ., Singapore, Singapore*
Andreas Burg - *École Polytechnique Fédérale de Lausanne, Switzerland*

14.3 Serial T0: Approximate Bus Encoding for Energy-Efficient Transmission of Sensor Signals (11:00)
Daniele Jahier Pagliari, Enrico Macii, **Massimo Poncino** - *Politecnico di Torino, Italy*

14.4 Designing Approximate Circuits using Clock Overgating* (11:15)
Younghoon Kim, Swagath Venkataramani, Kaushik Roy, Anand Raghunathan - *Purdue Univ., West Lafayette, IN*

A Q&A poster session will immediately follow the presentations from 11:30am to 12:00pm.

15 WINNING THE MEMORY CHALLENGE: WHICH NON-VOLATILE MEMORY TECHNOLOGY WILL RISE ABOVE?

Time: 10:30am - 12:00pm || Room: 18AB || Event Type: Invited Presentations
Track: Design, EDA || Topic Area: Emerging Technologies

CHAIRS:
Yuan Xie - *Univ. of California, Santa Barbara, CA*
Dmitri Strukov - *Univ. of California, Santa Barbara, CA*

ORGANIZERS:
Yuan Xie - *Univ. of California, Santa Barbara, CA*
Jishen Zhao - *Univ. of California, Santa Cruz, CA*

Emerging non-volatile memory such as PCRAM, ReRAM, or memristor technologies, have been recently studied extensively as promising candidates to replace SSD storage and DRAM memories. The speakers in this session will present their own favorite memory technology and discuss what promising advantages it provides and what hurdles must be overcome to make it the key to changing the landscape in memory designs.

15.1 Crushing the Memory-Storage Hierarchy (10:30)
Stan Williams - *Hewlett-Packard Labs., Palo Alto, CA*

15.2 STT-MRAM: Nonvolatile Information Processing for Energy-efficient Memory Subsystems (11:00)
Seung H. Kang - *Qualcomm, Inc., San Diego, CA*

15.3 Phase Change Memory as a Storage Class Memory (11:30)
Wanki Kim - *IBM Research, Yorktown Heights, NY*

16 THE RISE OF HETEROGENEOUS ARCHITECTURES: FROM EMBEDDED SYSTEMS TO DATA CENTERS

Time: 10:30am - 12:00pm || Room: 18CD || Event Type: Invited Presentations
Track: Design, Embedded Systems || Topic Area: System Architectures & SoC, General Interest, Codesign & System Design

CHAIR:
Todd Austin - *Univ. of Michigan, Ann Arbor, MI*

ORGANIZER:
Luca Carloni - *Columbia Univ., New York, NY*

For most classes of computing systems the distinction between low-power and high-performance design is outdated: from smartphones to cloud servers, systems-on-chip must deliver both. At the tail end of Dennard's scaling, this is becoming an increasingly tall order. Meanwhile, the limits of application parallelism prevents computer architects from scaling up performance by simply integrating more homogeneous processor cores. Instead, the quest for energy-efficient performance requires the integration of a variety of computing engines, including different kinds of processors and many specialized-hardware accelerators, leading to the rise of heterogeneous architectures.

The session will first overview the needs of heterogeneous systems and present a computer-vision application. The second talk addresses the growth of FPGA-based acceleration in heterogeneous data centers and the resulting programming challenges. The last talk proposes a new class of computing platforms to simplify the design and programming of heterogeneous SoCs for embedded applications.

16.1 Energy Efficiency: It is all about the memory (10:30)
Mark Horowitz - *Stanford Univ., Stanford, CA*

16.2 Heterogeneous Datacenters: Options and Opportunities (11:00)
Jason Cong - *Univ. of California, Los Angeles, CA*
Muhuan Huang, Di Wu - *Univ. of California, Los Angeles & Falcon Computing Solutions, Inc., Los Angeles, CA*
Cody Hao Yu - *Univ. of California, Los Angeles, CA*

16.3 The Case for Embedded Scalable Platforms (11:30)
Luca Carloni - *Columbia Univ., New York, NY*

17 DESIGN TRACK: EMBEDDED SYSTEMS - DESIGNS AND TOOLS

Time: 10:30am - 12:00pm || Room: Ballroom E || Event Type: Reviewed Presentations
Track: Embedded Systems || Topic Area: General Interest

CHAIR:
Jan Rellermeyer - *IBM Research, Austin, TX*

CO-CHAIR:
Alicia Strang - *Cadence Design Systems, Inc., Irvine, CA*

Embedded systems and software continues to be an important growth area in the industry. With the emergence of IoT applications there is a visible trend towards increasingly more powerful and sophisticated designs. This session showcases design approaches and novel tooling in key areas of embedded systems like FPGA-based acceleration, embedded vision, and bulk storage.

17.1 Accelerating an IoT Application by using FPGA tightly coupled with CPU (10:30)
Yuki Kobayashi, Takashi Takenaka, Takeo Hosomi, Yuichi Nakamura - *NEC Corp., Kawasaki, Japan*

17.2 Rapid Thermal Validation Solution for Architectural SSD HW/SW design (10:45)
Hyungwoo Lee - *Samsung Electronics Co., Ltd., Gyeonggi-do, Republic of Korea*
Kwanghyo Ahn - *Samsung Electronics Co., Ltd., Hwasung, Republic of Korea*
Jongbae Lee - *Samsung Electronics Co., Ltd., Seoul, Republic of Korea*

17.3 Power modeling by artificial neural network (11:00)
Zhaozhi Yang, Shupeng Zhao - *MediaTek, Inc., Beijing, China*
Yisiou Chen - *MediaTek, Inc., Hsinchu, Taiwan*

17.4 Considerations in Embedded Vision Application Design (11:15)
Ali Osman Ors, Daniel Laroche, **Rabindra Guha** - *NXP Semiconductors, Gatineau, QC, Canada*

17.5 A flexible and high-performance communication between FPGA and CPU for NFV Applications utilizing DPDK RingQueue (11:30)
Seiya Shibata, Takashi Takenaka, Takeo Hosomi, Yuichi Nakamura - *NEC Corp., Kawasaki, Japan*

17.6 Real Time Data-warehouse for Wireless and Embedded Systems (11:45)
Alex Chandra, Ashish Shrivastava, Mark W. Brown, Debashis Bhattacharya, **Alan Gatherer** - *FutureWei Technologies, Inc., Plano, TX*

Q&A Poster Session
Tuesday, June 7, 5:00 - 6:00pm - Exhibit Floor

18 DESIGN TRACK: REUSE AND RELIABILITY: SEMICONDUCTORS TO SUPERCONDUCTORS

Time: 10:30am - 12:00pm || Room: Ballroom F || Event Type: Reviewed Presentations
Track: EDA, Design || Topic Area: Circuit Design, Emerging Technologies, Low-Power & Reliability

CHAIR:
Duo Ding - *Oracle Corp., Austin, TX*

This session presents techniques for design and methodology reuse across product lines and material properties! Also outlined are methods to address chip reliability. It begins with methodologies targeting block and package-level reuse for microprocessors and smartphone chips respectively. Subsequent presentations address power supply noise reduction, ESD verification, and circuit aging analysis for advanced SoCs. The session concludes with a circuit design tool-chain for quantum information processors based on superconducting devices.

18.1 Clock Domain Independent Abstraction and Programmable Clock Division Methodology To Enable Reuse Of Macros In High Performance Processor Designs (10:30)
Naiju K. Abdul - *IBM Systems and Technology Group, Bangalore, India*
Michael Wood - *IBM Systems and Technology Group, Poughkeepsie, NY*
Jack DiLullo - *IBM Systems and Technology Group, Austin, TX*
Adil Bhanji - *IBM Systems and Technology Group, Poughkeepsie, NY*
Manish Verma - *IBM Server and Technology Group, Bangalore, India*

18.2 Integrated chip and package co-analysis for early data-driven package bump & ball optimization on Value-Tier Smartphone products (10:45)
Biswajit Patra, Amrita Brahmachari, Shreshta Ganguly - *Qualcomm India Pvt. Ltd., Bangalore, India*
Ashish Singh, Vinayakam Subramanian - *ANSYS, Inc., Bangalore, India*
Amlan Chakrabarti, Sanatan Chattopadhyay - *Univ. of Calcutta, India*

18.3 ESD Failure Analysis Methodology & Verification for Custom Analog IP (11:00)
Joohee Kim, Norman Chan, Hai Lan - *Rambus, Inc., Sunnyvale, CA*
Karthik Srinivasan, Norman Chang - *ANSYS, Inc., San Jose, CA*

18.4 Full-chip ESD Verification for Complex Multi-domain Storage SoCs (11:15)
Pritesh Pawaskar - *Seagate Technology, LLC, Pune, India*
Shrikrishna N. Mehetre - *Open-Silicon, Inc., Bangalore, India*
Niranjan Pol - *Seagate Technology, LLC, Pune, India*
Anant Narain - *Apache Design, Inc., A Subsidiary of ANSYS, Inc., Noida, India*

18.5 Fabric: Mobile SOC Chip Level Aging Design Methodology for Advanced FinFET Technologies (11:30)
Yiwei Fu, **Yongsheng Sun**, Jianping Guo, Canhui Zhan, Jun Xia - *HiSilicon, Shenzhen, China*
Junhui Zhao, Teong Ming Cheah - *ANSYS, Inc., Shenzhen, China*

18.6 Superconducting mixed-signal circuit design toolchain (11:45)
Mark H. Volkmann, Paul Bunyk, Colin Enderud, Mark W. Johnson, Elena Tolkacheva - *D-Wave Systems Inc., Burnaby, BC, Canada*

Q&A Poster Session
Tuesday, June 7, 5:00 - 6:00pm - Exhibit Floor

Thank You to Our Sponsor:

19 IP TRACK: IP ECOSYSTEM MANAGEMENT

Time: 10:30am - 11:00am || Room: Ballroom G || Event Type: Reviewed Presentations
Track: IP, IP || Topic Area: Business

CHAIR:
Heather Monigan - *Intel Corp., Chandler, AZ*

Join us for a session exploring modern IP management conundrums of "I Didn't Mean to Steal Your IP ..." and Other Cautionary Tales and encrypting IP Cores With Gate-level Simulation Capabilities.

19.1 "I Didn't Mean to Steal Your IP ..." and Other Cautionary Tales (10:30)
Warren Savage - *IPextreme, Campbell, CA*
Eric Stein - *PricewaterhouseCoopers LLP, San Francisco, CA*

19.2 Encrypting IP Cores With Gate-level Simulation Capabilities (10:45)
Parameswaran Ramanathan, Kewal K. Saluja - *Univ. of Wisconsin, Madison, WI*

Q&A Poster Session
Tuesday, June 7, 5:00 - 6:00pm - Exhibit Floor

Thank You to Our Sponsor:

20 IP TRACK: FISH FOOD FOR THOUGHT: IS THE CONSOLIDATION TREND IN THE IP ECOSYSTEM GOOD FOR THE INDUSTRY?

Time: 11:00am - 12:00pm || Room: Ballroom G || Event Type: Panel || Track: IP, EDA
Topic Area: Business, General Interest, Business

MODERATOR:
John Blyler - *IEEE, Portland, OR*

ORGANIZER:
Heather Monigan - *Intel Corp., Chandler, AZ*

In this panel, the panel participants are asked to contemplate and comment on the year-over-year trend of smaller commercial IP companies being gobble up by larger, more established companies. The Commercial IP Ecosystem is growing, and projected to sustain growth, yet the pool seems smaller, year over year. Is this current trend a hindrance or catalyst for innovation? What challenges would IP companies expect when swimming in these waters? What conditions may repopulate the pool? Who ultimately prospers: the investors or end customers?

PANELISTS:
Samir Patel - *Sankalp Semiconductor, Sunnyvale, CA*
Dennis Segers - *Leyden Technologies, Los Altos, CA*
Camille Kokozaki - *Design Rivers, San Jose, CA*
Laxman Vemury - *Lattice Semiconductor Corp., Sunnyvale, CA*
Hezi Saar - *Synopsys, Inc., Mountain View, CA*

Thank You to Our Sponsor:

SKY TALK: RISC-V: INSTRUCTION SETS WANT TO BE FREE

Time: 1:00pm - 1:30pm || Room: DAC Pavilion - Booth 1839 || Event Type: SKY Talk
Track: IoT, IP || Topic Area: System Architectures & SoC, Codesign & System Design, General Interest

The most important interface in a computer system is the instruction set architecture (ISA) as it connects software to hardware. So, given the prevalence of open standards for almost all other important interfaces, why is the ISA still proprietary? We argue that a free ISA is a necessary precursor to future hardware innovation, and there's no good technical reason not to have free, open ISAs just as we have free, open networking standards and free, open operating systems.

The free and open RISC-V ISA began development at UC Berkeley in 2010, with the frozen base user ISA standard released in May 2014, and has since seen rapid uptake around the globe, including the first commercial shipments.

This talk will cover the technical features of the RISC-V ISA design, which has the goals of scaling from the tiniest implementations for IoT up to the largest warehouse-scale computers, with support for extensive customization. We'll also describe three different industry-competitive open-source cores developed at UC Berkeley, all written in Chisel, a productive new open-source hardware design language. Finally, we'll describe the uptake of RISC-V and the development of the RISC-V ecosystem, including the RISC-V Foundation.

SPEAKER:
Krste Asanovic - *Univ. of California, Berkeley & SiFive, Inc., Berkeley, CA*

21 BRAIN-ON-A-CHIP: ARCHITECTURES FOR NEUROMORPHIC COMPUTING AND LEARNING

Time: 1:30pm - 3:00pm || Room: 12AB || Event Type: Reviewed Presentations || Track: EDA
Topic Area: Emerging Technologies

CHAIR:
Yu Wang - *Tsinghua Univ., Beijing, China*

CO-CHAIR:
David Z. Pan - *Univ. of Texas at Austin, TX*

This session covers the state-of-the-art in neuromorphic computing, machine learning and image processing implementations in hardware using both conventional CMOS and emerging technologies.

*** Indicates Best Paper Candidate**

21.1 A New Learning Method for Inference Accuracy, Core Occupation, and Performance Co-optimization on TrueNorth Chip* (1:30)
Wei Wen, Chunpeng Wu, Yandan Wang, Kent Nixon - *Univ. of Pittsburgh, PA*
Qing Wu, Mark Barnell - *Air Force Research Lab, Rome, NY*
Hai Li, Yiran Chen - *Univ. of Pittsburgh, PA*

21.2 Dot-Product Engine for Neuromorphic Computing: Programming 1T1M Crossbar to Accelerate Matrix-Vector Multiplication (1:45)
Miao Hu, John Paul Strachan, Zhiyong Li, Emmanuelle M. Grafals, Noraica Davila, Catherine Graves, Sity Lam - *Hewlett-Packard Labs., Palo Alto, CA*
Ning Ge - *Hewlett-Packard Co., Palo Alto, CA*
Stanley R. Williams - *Hewlett-Packard Labs., Palo Alto, CA*
Jianhua Yang - *Univ. of Massachusetts, Amherst, MA*

21.3 Perform-ML: Performance Optimized Machine Learning by Platform and Content Aware Customization (2:00)
Azalia Mirhoseini, Bita Darvish Rouhani, Ebrahim Songhori - *Rice Univ., Houston, TX*
Farinaz Koushanfar - *Univ. of California at San Diego, La Jolla, CA*

21.4 Low-Power Approximate Convolution Computing Unit with Domain-Wall Motion Based "Spin-Memristor" for Image Processing Applications (2:15)
Yong Shim, Abhronil Sengupta, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

A Q&A poster session will immediately follow the presentations from 2:30pm to 3:00pm.

22 SLICE AND DICE - ADVANCES IN VERIFICATION AND TEST

Time: 1:30pm - 3:00pm || Room: 19AB || Event Type: Reviewed Presentations || Track: EDA
Topic Area: Test & Verification

CHAIR:
Rolf Drechsler - *Univ. of Bremen & DFKI GmbH, Germany*
CO-CHAIR:
Harry Foster - *Mentor Graphics Corp., Plano, TX*

Design validation today is critically dependent on effective partitioning techniques and scalable validation methods to cope with the complexity of modern computing systems. This session looks at effective partitioning and slicing techniques for various domains, as well as efficient techniques for improving scalability of validation and testing tools. The first two papers focus on design partitioning at different abstraction levels. The third paper is about bug-masking analysis during processor verification. The last paper describes a method to accelerate fault injection analysis.

*** Indicates Best Paper Candidate**

22.1 A Framework for Verification of SystemC TLM Programs with Model Slicing: A Case Study (1:30)
Reza Hajisheykhi, Mohammad Roohitavaf - *Michigan State Univ., East Lansing, MI*
Ali Ebnenasir - *Michigan Technological Univ., Houghton, MI*
Sandeep Kulkarni - *Michigan State Univ., East Lansing, MI*

22.2 Design Partitioning for Large-Scale Equivalence Checking and Functional Correction* (1:45)
Grace Wu, Yi-Tin Sun, Jie-Hong (Roland) Jiang - *National Taiwan Univ., Taipei, Taiwan*

22.3 Probabilistic Bug-Masking Analysis for Post-Silicon Tests in Microprocessor Verification (2:00)
Doowon Lee - *Univ. of Michigan, Ann Arbor, MI*
Tom Kolan, Arkadiy Morgenshtein, Vitali Sokhin, Ronny Morad, Avi Ziv - *IBM Research, Haifa, Israel*
Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

22.4 Fault Injection Acceleration by Simultaneous Injection of Non-interacting Faults (2:15)
Mojtaba Ebrahimi, MohammadHadi Moshrefpour, **Mohammad Saber Golanbari**, Mehdi B. Tahoori - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

A Q&A poster session will immediately follow the presentations from 2:30pm to 3:00pm.

23 ENVIRONMENT-AWARE, REACTIVE AND SECURE AUTOMOTIVE SYSTEMS

Time: 1:30pm - 3:00pm || Room: 17AB || Event Type: Reviewed Presentations
Track: Automotive, Embedded Systems, Security || Topic Area: Cyber-Physical Systems, System Software, Codesign & System Design

CHAIR:
Ramesh S - *General Motors Research and Development, Warren, MI*
CO-CHAIR:
Huafeng Yu - *Toyota InfoTechnology Center, Mountain View, CA*

Modern automotive systems need to meet the challenges of autonomous driving by precise localization, effective detection and identification of the road and the surrounding objects, as well as deterministic and predictable timing.

The four papers in this session provide innovative solutions for the problem of efficient sensor processing; predictable and reliable transmission of data over Ethernet; caching policies that allow for probabilistic timing analysis; and secure and accurate localization.

*** Indicates Best Paper Candidate**

23.1 Privacy Preserving Localization for Smart Automotive Systems (1:30)
Siam Umar Hussain, Farinaz Koushanfar - *Univ. of California at San Diego, La Jolla, CA*

23.2 Integration of Multi-Sensor Occupancy Grids into Automotive ECUs (1:45)
Tiana Rakotovao - *CEA-LETI Minatec & Inria Grenoble - Rhône-Alpes, Grenoble, France*
Julien Mottin, Diego Puschini - *CEA-LETI Minatec, Grenoble, France*
Christian Laugier - *Inria Grenoble - Rhône-Alpes, Saint Ismier, France*

23.3 Formal Reliability Analysis of Switched Ethernet Automotive Networks under Transient Transmission Errors* (2:00)
Fedor Smirnov, Michael Glaß - *Friedrich-Alexander-Univ. Erlangen-Nürnberg, Germany*
Felix Reimann - *Audi Electronics Venture GmbH, Gaimersheim, Germany*
Jürgen Teich - *Friedrich-Alexander-Univ. Erlangen-Nürnberg, Germany*

23.4 Random Modulo: a New Processor Cache Design for Real-Time Critical Systems (2:15)
Carles Hernandez, Jaume Abella - *Barcelona Supercomputing Center, Barcelona, Spain*
Andrea Gianarro, Jan Andersson - *Cobham Gaisler, Gothenburg, Sweden*
Francisco J. Cazorla - *Barcelona Supercomputing Center, Barcelona, Spain*

A Q&A poster session will immediately follow the presentations from 2:30pm to 3:00pm.

24 CROSS-LAYER RELIABILITY AWARE DESIGN, OPTIMIZATION AND DYNAMIC MANAGEMENT

Time: 1:30pm - 3:00pm || Room: 18AB || Event Type: Invited Presentations
Track: EDA, Embedded Systems || Topic Area: Low-Power & Reliability, Modeling, Simulation & Timing, General Interest

CHAIRS:
Mehul Shroff - *NXP Semiconductors, Austin, TX*
Ertugrul Demircan - *NXP Semiconductors, Austin, TX*

ORGANIZER:
Sheldon X.-D. Tan - *Univ. of California, Riverside, CA*

Reliability has become a significant challenge for design of current nanometer integrated circuits (ICs). Existing technologies for ensuring reliability will not be able to satisfy the competing requirements for future ICs as they typically operate in one layer under worst-case assumptions about other layers in the design stacks. This potentially leads to inefficiencies that will make these techniques impractical in future fabrication processes. This session will present several recent advances in holistic cross-layer design approaches for reliability management and mitigation. The presented topics range from cross-layer modeling and optimization for electromigration reliability; design for soft-error reliability considering device, circuit and architecture levels; reliability and modeling and optimization for many long-term failure effects at physics, circuits, and architecture intersections and cross-layer variability mitigation techniques for 10nm and beyond technologies.

24.1 Cross-Layer Modeling and Optimization for Electromigration Induced Reliability (1:30)
Taeyoung Kim, Zeyu Sun, Chase Cook, Hengyang Zhao, Ruiwen Li, Daniel Wong, **Sheldon X.-D. Tan** - *Univ. of California, Riverside, CA*

24.2 Optimizing Device Reliability Effects at the Intersection of Physics, Circuits, and Architecture (1:50)
Sachin Sapatnekar, Deepashree Sengupta, Vivek Mishra - *Univ. of Minnesota, Minneapolis, MN*

24.3 Tackling Variability Issues at 10nm and Beyond Through a Cross-Layer Approach (2:10)
Mondira (Mandy) Pant, Bill Bowhill, Arijit Biswas - *Intel Corp., Hudson, MA*

24.4 Cross-layer Approaches for Soft Error Modeling and Mitigation (2:30)
Mojtaba Ebrahimi, **Mehdi B. Tahoori** - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

25 SOMETHING FOR NOTHING: HARVESTING ENERGY FROM THE ENVIRONMENT

Time: 1:30pm - 3:00pm || Room: 18CD || Event Type: Invited Presentations
Track: Embedded Systems, IoT || Topic Area: Emerging Technologies

CHAIR:
Saurabh Sinha - *ARM Ltd., Austin, TX*

ORGANIZER:
Rob Aitken - *ARM, Inc., San Jose, CA*

Energy harvesting offers the possibility of an unlimited supply of free energy, but actually realizing this potential requires significant effort. This session looks at energy harvesting from three perspectives: what's out there in terms of the harvesters themselves, what's needed to convert the notoriously unreliable power from harvesters into something usable by a conventional system, and finally how might future compute systems be structured to take better advantage of the harvester behavior.

25.1 Additively Manufactured Wireless Self-Powered (Energy-Harvesting) Platforms for Communication, Sensing and Radar Applications (1:30)
Manos M. Tentzeris - *Georgia Institute of Technology, Atlanta, GA*

25.2 Power Extraction Circuits for Optimal Energy Harvesting (2:00)
Yogesh Ramadass - *Texas Instruments, Inc., Santa Clara, CA*

25.3 Energy Harvesting and Transient Computing: A Paradigm Shift for Embedded Systems? (2:30)
Geoff Merrett - *Univ. of Southampton, United Kingdom*

26 DESIGN TRACK: EMBEDDED SECURITY: DOES THE INDUSTRY CARE?

Time: 1:30pm - 3:00pm || Room: Ballroom E || Event Type: Invited Presentations
Track: Security, Embedded Systems || Topic Area: General Interest, System Software, Codesign & System Design

CHAIR:
Saverio Fazzari - *Booz Allen Hamilton, Inc., Arlington, VA*

ORGANIZER:
Ramesh Karri - *New York Univ., Brooklyn, NY*

This designer track session brings hardware, software and embedded system designers to discuss what is and what is not important in terms of security. They will discuss security challenges in IOT supply chain, IOT systems and embedded software. The first speaker will talk about system (from software to hardware) level security. The second speaker will discuss how to enhance the supply chain to ensure security throughout the IoT device life cycle.

26.1 Securing the IoT device lifecycle using hardware root of trust (1:30)
Dimitrios Pendarakis - *IBM T.J. Watson Research Center, Yorktown, NY*

26.2 Enhancing the supply chain to ensure security throughout the IoT device life cycle (2:00)
Jim Alfred - *BlackBerry, Toronto, ON, Canada*

26.3 IoT: A Security Researcher's Take (2:30)
Greg Franson - *Cisco Systems, Inc., Austin, TX*

27 DESIGN TRACK: NEW SIGN-OFF FLOW CHALLENGES IN ADVANCED DESIGN NODE

Time: 1:30pm - 3:00pm || Room: Ballroom F || Event Type: Invited Presentations
Track: EDA, Design || Topic Area: Modeling, Simulation & Timing, Low-Power & Reliability

CHAIR:
Scott Taylor - *Qualcomm Technologies, Inc., Austin, TX*

Electrical (timing and power) sign-off of nanometer chips is an increasingly complex and arduous task. Multiple factors contribute to the difficulty: increased process variations leading to an explosion of process corners and OCV problems, significant waveform effects on circuit and interconnect delay, multi-vdd designs, ultra-low voltage operation, increased on-chip voltage fluctuations, and signifcant inter-play between chip and package. These challenges are faced across the entire design ecosystem: foundries, library providers, design and IP teams, and EDA vendors. Innovative methods are required in library modeling, design practices and sign-off recipes, and EDA tools and methodologies for successful tape-outs and good yields.

The speakers in this session are industry leaders from foundry, library and design arenas. They will address the prevalent and emerging problems in electrical sign-off, and the solution strategies being developed and deployed within their purview.

27.1 Challenges for LVF characterization and STA at ULV (1:30)
Florentin Dartu - *Taiwan Semiconductor Manufacturing Co., Ltd., Austin, TX*

27.2 A Low Voltage Sign-off Timing Methodology Using LVF Models (2:00)
Marlin Frederick, Jr. - *ARM, Inc., Austin, TX*
Jim Dodrill - *ARM, Inc., Dripping Springs, TX*
Igor Keller - *Cadence Design Systems, Inc., San Jose, CA*

27.3 Power aspects (2:30)
Shane Stelmach - *Texas Instruments, Inc., Dallas, TX*

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28 IP TRACK: DESIGNING WITH RISC-V

Time: 1:30pm - 3:00pm || Room: Ballroom G || Event Type: Embedded Tutorial || Track: IP, Design
Topic Area: General Interest, Emerging Technologies

CHAIR:
Andrea Kroll - *Cadence Design Systems, Inc., San Jose, CA*

ORGANIZER:
Rick O'Connor - *RISC-V Foundation, Berkeley, CA*

This session consists of a brief RISC-V Overview followed by four tutorial presentations covering the following:

1. RISC-V Overview
2. RISC-V Tool chain & OS environment
3. RISC-V Security Enhancements using Bluespec
4. RISC-V Rocket Core using Xilinx FPGAs

SPEAKERS:
Rick O'Connor - *RISC-V Foundation, Berkeley, CA*
Andrew Waterman - *SiFive, Inc., San Fransisco, CA*
Andre DeHon - *Draper, Cambridge, MA*
Alex Bradbury - *lowRISC, Cambridge, United Kingdom*

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29 NOC IT OUT OF THE PARK

Time: 3:30pm - 5:30pm || Room: 12AB || Event Type: Reviewed Presentations || Track: EDA
Topic Area: NoC & On-Chip Interconnects

CHAIR:
Umit Ogras - *Arizona State Univ., Tempe, AZ*

CO-CHAIR:
Paul Gratz - *Texas A&M Univ., College Station, TX*

This session is composed of six presentations exploring new applications and technologies for Networks-on-Chip. Innovative architectures, memory solutions and data compression, as well as new networks based on photonic technology are discussed. The presented solutions consider key metrics such as energy-efficiency, process variation, cross-talk, data congestion and latency.

*** Indicates Best Paper Candidate**

29.1 A Low-Cost Conflict-Free NoC for GPGPUs (3:30)
Xia Zhao - *Ghent Univ. & National Univ. of Defense Technology, Ghent, Belgium*
Sheng Ma - *National Univ. of Defense Technology, Changsha, China*
Yuxi Liu - *Ghent Univ. & Peking Univ., Ghent, Belgium*
Lieven Eeckhout - *Ghent Univ., Ghent, Belgium*
Zhiying Wang - *National Univ. of Defense Technology, Changsha, China*

29.2 Notifying Memories: a case-study on Data-Flow Applications with NoC Interfaces Implementation (3:45)
Kevin J. M. Martin, Mostafa Rizk - *Lab-STICC & Univ. de Bretagne SUD, Lorient, France*
Jean-Philippe Diguet - *Lab-STICC & Centre National de la Recherche Scientifique, Lorient, France*
Martha Johanna Sepulveda - *Technische Univ. München, Germany*

29.3 Quest for High-Performance Bufferless NoCs with Single-Cycle Express Paths and Self-Learning Throttling* (4:00)
Bhavya K. Daya - *Massachusetts Institute of Technology & Intel Corp., Hillsboro, OR*
Li-Shiuan Peh, Anantha Chandrakasan - *Massachusetts Institute of Technology, Cambridge, MA*

29.4 DISCO: A Low Overhead In-Network Data Compressor for Energy-Efficient Chip Multi-Processors (4:15)
Ying Wang - *Chinese Academy of Sciences & Institute of Computing Technology, Beijing, China*
Huawei Li, Yinhe Han, Jun Zhou, Xiaowei Li - *Institute of Computing Technology & Chinese Academy of Sciences & Univ. of Chinese Academy of Sciences, Beijing, China*

29.5 Achieving Lightweight Multicast in Asynchronous Networks-on-Chip Using Local Speculation (4:30)
Kshitij Bhardwaj, Steven M. Nowick - *Columbia Univ., New York, NY*

29.6 PICO: Mitigating Heterodyne Crosstalk Due to Process Variations and Intermodulation Effects in Photonic NoCs (4:45)
Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha - *Colorado State Univ., Fort Collins, CO*

A Q&A poster session will immediately follow the presentations from 5:00pm to 5:30pm.

30 PROBABLY OR PROVABLY? ADVANCES IN DFM

Time: 3:30pm - 5:30pm || Room: 19AB || Event Type: Reviewed Presentations || Track: EDA
Topic Area: Lithography & DFM, Low-Power & Reliability

CHAIR:
Duo Ding - *Oracle Corp., Austin, TX*

CO-CHAIR:
Saurabh Sinha - *ARM, Inc., Austin, TX*

While there seem to be many unsurmountable challenges in the More-Moore age, there is also a growing number of solutions to meet the demands of circuit design and manufacturing. This session covers many 'probable' DFM and reliability analysis techniques with 'provable' outcomes, from multi-patterning and directed self-assembly, to dielectric breakdown, electromigration and soft errors due to cosmic rays.

*** Indicates Best Paper Candidate**

30.1 Multiple Patterning Layout Decomposition Considering Complex Coloring Rules* (3:30)
Hua-Yu Chang - *Synopsys, Inc., Hsinchu, Taiwan*
Iris Hui-Ru Jiang - *National Chiao Tung Univ., Hsinchu, Taiwan*

30.2 Redundant Via Insertion for Multiple-Patterning Directed-Self-Assembly Lithography (3:45)
Seongbo Shim, Woohyun Chung, Youngsoo Shin - *KAIST, Daejeon, Republic of Korea*

30.3 Self-Aligned Double Patterning-Aware Detailed Routing with Double Via Insertion and Via Manufacturability Consideration (4:00)
Yixiao Ding, Chris Chu - *Iowa State Univ., Ames, IA*
Wai-Kei Mak - *National Tsing Hua Univ., Hsinchu, Taiwan*

30.4 Predicting Electromigration Mortality Under Temperature and Product Lifetime Specifications (4:15)
Vivek Mishra, Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

30.5 A Monte Carlo Simulation Flow for SEU Analysis of Sequential Circuits (4:30)
Meng Li, Ye Wang, Michael Orshansky - *Univ. of Texas at Austin, TX*

30.6 Physics-Based Full-Chip TDDB Assessment for BEOL Interconnects (4:45)
Xin Huang - *Univ. of California, Riverside, CA*
Valeriy Sukharev - *Mentor Graphics Corp., Fremont, CA*
Zhongdong Qi, Taeyoung Kim, Sheldon X.-D. Tan - *Univ. of California, Riverside, CA*

A Q&A poster session will immediately follow the presentations from 5:00pm to 5:30pm.

31 EMBEDDED SOFTWARE FOR RELIABILITY AND PERFORMANCE

Time: 3:30pm - 5:30pm || Room: 17AB || Event Type: Reviewed Presentations
Track: Embedded Systems || Topic Area: System Software, Low-Power & Reliability

CHAIR:
Oliver Bringmann - *Eberhard Karls Univ. Tubingen, Germany*

CO-CHAIR:
Jian-Jia Chen - *Technische Univ. Dortmund, Germany*

Reliability and performance are critical concerns for modern embedded system software. This session presents novel compiler and run-time techniques for improved device reliability, protection from soft errors, on-chip thermal management, and reduced aging. The session also introduces approaches for maximizing system performance by advanced compilation and dynamic scheduling methods for automatic code parallelization, optimized multi-threading, effective timing speculation, and improved energy savings in mobile devices.

*** Indicates Best Paper Candidate**

31.1 ageOpt-RMT: Compiler-Driven Variation-Aware Aging Optimization for Redundant Multithreading (3:30)
Florian Kriebel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Semeen Rehman - *Technische Univ. Dresden, Germany*
Muhammad Shafique, Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

31.2 Improving Mobile Gaming Performance through Cooperative CPU-GPU Thermal Management* (3:45)
Alok Prakash - *National Univ. of Singapore, Singapore*
Hussam Amrouch, Muhammad Shafique - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Tulika Mitra - *National Univ. of Singapore, Singapore*
Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

31.3 nZDC: A Compiler technique for near Zero silent Data Corruption (4:00)
Moslem Didehban - *Arizona State Univ., Tempe, AZ*
Aviral Shrivastava - *Arizona State Univ., Phoenix, AZ*

31.4 Automatic Parallelization and Accelerator Offloading for Embedded Applications on Heterogeneous MPSoCs (4:15)
Miguel Angel Aguilar, Rainer Leupers, Gerd Ascheid - *RWTH Aachen Univ., Aachen, Germany*
Luis Gabriel Murillo - *Silexica Software Solutions GmbH, Aachen, Germany*

31.5 Similarity-Based Wakeup Management for Mobile Systems in Connected Standby (4:30)
Chun-Hao Kao, **Sheng-Wei Cheng** - *National Taiwan Univ., Taipei, Taiwan*
Pi-Cheng Hsiu - *Academia Sinica, Taipei, Taiwan*

31.6 Synergistic Timing Speculation for Multi-threaded Programs (4:45)
Atif Yasin - *Utah State Univ., Logan, UT*
Jeff J. Zhang - *New York Univ., Brooklyn, NY*
Hu Chen, Sanghamitra Roy - *Utah State Univ., Logan, UT*
Siddharth Garg - *New York Univ., Brooklyn, NY*
Koushik Chakraborty - *Utah State Univ., Logan, UT*

A Q&A poster session will immediately follow the presentations from 5:00pm to 5:30pm.

32 TSVS ARE SO 2010 - THE REALITY OF 3D-IC

Time: 3:30pm - 4:30pm || Room: 18AB || Event Type: Panel || Track: Design, EDA
Topic Area: Physical Design

MODERATOR:
Edward Sperling - *Semiconductor Engineering, San Jose, CA*

ORGANIZER:
Laura Parker - *Mentor Graphics Corp., Portland, OR*

It is an exciting time in packaging, with new approaches emerging continuously. The driving force is to support consumer, mobile applications that require thinner, higher density packages without sacrificing the performance of the IC. The emergence of the Internet of Things (IoT) will only increase the pressure for continued innovation in packaging.

Today there is a wide range of packaging including: Wafer Level Chip Scale, Wafer Level Fan Out, Panel Level Fan Out, Chip Last Fan Out, Flip Chip, interposer 2.5D, 3D and the list goes on and on. So will one win out or can the ecosystem continue to support an ever broadening range of styles and custom approaches? This panel will present views on this pressing issue from the designer perspective, packaging, tools, and foundry.

PANELISTS:
John Hunt - *ASE Inc., Tempe, AZ*
David Z. Pan - *Univ. of Texas at Austin, TX*
Max Min - *Samsung Electronics Co., Ltd., Milpitas, CA*

33 WHAT'S THE FUTURE OF DFT?

Time: 4:30pm - 5:30pm || Room: 18AB || Event Type: Panel || Track: EDA
Topic Area: Test & Verification

MODERATOR:
Shawn Blanton - *Carnegie Mellon Univ., Pittsburgh, PA*

ORGANIZER:
Rob Aitken - *ARM, Inc., San Jose, CA*

Design-for-testability (DFT) has progressed over the last 25 years from an expensive adder to be included only if quality demanded it to a mandatory feature of every design. High quality tools are available from EDA vendors and there is a substantial and diverse body of research behind them. Still, when most people think of DFT, they think of scan chains, and scan-based DFT seems to be a done deal.

Given that, what is the future of the DFT business? There are many challenges that get lumped together as part of test (yield, performance/power characterization/optimization, debug/diagnosis/validation, analog measurement, DFM compliance, etc.), so DFT is more than just building scan chains, but is that where the future lies? The panel looks at the issues and explores how we might expect the DFT business to evolve going forward.

PANELISTS:
Jeff Rearick - *Advanced Micro Devices, Inc., Fort Collins, CO*
Joe Sawicki - *Mentor Graphics Corp., Wilsonville, OR*
Anne Gattiker - *IBM Research, Austin, TX*
David Park - *Optimal Plus Inc., San Jose, CA*

34 FUTURE VEHICULAR NETWORKS - SAFETY AND SECURITY

Time: 3:30pm - 5:30pm || Room: 18CD || Event Type: Invited Presentations
Track: Automotive, Security || Topic Area: Cyber-Physical Systems

CHAIR:
Selma Saidi - *Technical Univ. of Hamburg, Germany*

ORGANIZER:
Rolf Ernst - *Technische Univ. Braunschweig, Germany*

Next-generation vehicular networks are anticipated to comprise a single high-bandwidth communication backbone, which is used by both critical and non-critical traffic. These networks require advanced safety mechanisms, such as isolation between different criticality levels and fail-operational network behavior to provide a reliable communication infrastructure, e.g. for highly automated and autonomous driving.

In the future, vehicular networks will even extend beyond the individual vehicle. In vehicle-to-vehicle and vehicle-to-infrastructure scenarios, cars become part of a larger network. Connected vehicles have strict security requirements to guarantee authenticity, integrity, and confidentiality of the data entering and leaving the vehicle.

This session presents new ideas and discusses advanced methods to implement and analyze the safety and security of next-generation vehicular networks.

34.1 Cooperation or Competition? Coexistence of Safety and Security in Next-Generation Ethernet-Based Automotive Networks (3:30)
Chung-Wei Lin, Huafeng Yu - *Toyota InfoTechnology Center, Mountain View, CA*

34.2 Towards Fail-Operational Ethernet Based In-Vehicle Networks (4:00)
Mischa Möstl, Daniel Thiele, **Rolf Ernst** - *Technische Univ. Braunschweig, Germany*

34.3 Secure Updates for Automotive ECUs (4:30)
Lars Wolleschensky - *ESCRYPT Inc., Ann Arbor, MI*
André Osterhues - *ESCRYPT Inc., Bochum, Germany*

34.4 Extending Communication Beyond Vehicles - The Road To Automated Driving (5:00)
Steffen Müller, Timo van Roermund, Mark Steigemann - *NXP Semiconductors, Hamburg, Germany*

35 DESIGN TRACK: THE GREAT SIMULATION/EMULATION FACEOFF

Time: 3:30pm - 5:00pm || Room: Ballroom E || Event Type: Panel || Track: Design, EDA
Topic Area: Modeling, Simulation & Timing, Test & Verification, General Interest

MODERATOR:
John Sanguinetti - *Adapt-IP, Campbell, CA*

From all appearances, emulation is about to take over domination of the verification space from the 30-year old work horse, simulation. The number of use models is expanding, as well as features and capabilities. Simulation experts, however, aren't eager to wave the white flag and, in fact, point to the rapid adoption of formal verification that continues simulation's value.

Questions to be debated:

- Will emulation take over from simulation and be the dominant tool in a verification flow?
- If not emulation, where does simulation go to continue to be an effective verification tool?
- Does augmenting simulation with emulation or formal verification provide the most benefit?
- Which combination will dominate future verification flows?

The format will be entertaining but informative with differing views and some conflict. Panelists will describe the various use models for emulation and explain how and why simulation has been so effective for so long. They will debate whether the simulation/formal verification flow works more effectively than a simulation/emulation flow. Finally, they will be asked to present their views on the evolution of verification in general and predictions about what's coming next.

John Sanguinetti, a noted simulation expert, will serve as moderator and have questions to stimulate the discussion, including how formal verification provides an orthogonal approach to simulation's capabilities. Conversely, he will press panelists to explain why emulation doesn't support formal verification as yet and, instead, focuses on execution performance. He will question the panel on the usability of each for hardware development and hardware/software integration, verification and the flexibility of both. Availability is another question that will be asked of the panel — are both available to every engineer or used as a team tool? And, what are the training requirements? Cost considerations will be explored as the panel attempts to sort through the total cost of each, the cost per engineer and the cost per upgrade. Finally, John Sanguinetti will ask each panelist what is missing from the verification flow, such as emulation's inability to offer support for analog and whether that will be possible in the future. Or, whether it will be a long-term hindrance.

PANELISTS:
Alex Starr - *Advanced Micro Devices, Inc., Boxborough, MA*
Frank Schirmeister - *Cadence Design Systems, Inc., San Jose, CA*
Ronny Morad - *IBM Research - Haifa, Israel*
Stephen Bailey - *Mentor Graphics Corp., Longmont, CO*
Dave Kelf - *OneSpin Solutions GmbH, San Jose, CA*

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36 DESIGN TRACK: DESIGN CHALLENGES IN ADVANCED NODES: FOUNDRY PERSPECTIVE

Time: 3:30pm - 5:00pm || Room: Ballroom F || Event Type: Invited Presentations
Track: Design, EDA || Topic Area: Lithography & DFM, Physical Design, Low-Power & Reliability

CHAIR:
Rajendran Panda - *Oracle Corp., Austin, TX*

ORGANIZER:
Bertram Bradley - *GLOBALFOUNDRIES, Austin, TX*

In this invited speaker session we will hear from executives and fellows at 3 leading Foundry and Design companies. Featured speakers from GlobalFoundries, IBM, and SMIC will describe challenges in their latest and most prominent design efforts. Topics will include technical and business-driven challenges in moving to the latest technology nodes, and each company's perspective in how they are overcoming obstacles and driving towards new benchmarks in size, speed, and performance.

36.1 Back-End Design Challenges in 14nm and Beyond: A Foundry Perspective (3:30)
Jeanne Trinko-Mechler - *GLOBALFOUNDRIES, Essex Junction, VT*

36.2 Challenges and Solutions To a New Era of Intellisense (4:00)
Tianshen Tang - *Semiconductor Manufacturing International Corp., Shanghai, China*

36.3 Design challenges for high-end micro-processors at the leading edge (4:30)
Leon Stok - *IBM Corp., Poughkeepsie, NY*

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37 IP TRACK: EVOLVING IP INTERCONNECTS & VERIFICATION

Time: 3:30pm - 5:00pm || Room: Ballroom G || Event Type: Reviewed Presentations
Track: IP, IP || Topic Area: Circuit Design, Test & Verification

CHAIR:
Andrea Kroll - *Cadence Design Systems, Inc., San Jose, CA*

Join us for a varied session that explores the evolution and progression of interconnect IP's and the challenges facing IP synthesis and verification.

37.1 Breaking Through 'The Memory Wall' - HBM IP Subsystem (3:30)
Dhananjay Wagh, Bhupesh Dasila - *Open-Silicon, Inc., Milpitas, CA*

37.2 Is USB Relevant to IoT? (3:45)
Nivin George - *Synopsys, Inc., Bangalore, India*
Venkataraghavan Krishnan - *Synopsys, Inc., Mountain View, CA*

37.3 High-Level Synthesis Enabling the Design of a Scalable Wi-Fi HaLow™ IP Product Family for Boosting IoT (4:00)
Dejan M. Dumic - *Methods2Business BV, Eindhoven, The Netherlands*
Farhad Mighani - *Adapt-IP, San Jose, CA*
Marleen J. Boonen, Nemanja Kondic - *Methods2Business BV, Eindhoven, The Netherlands*
Daniel Kesler - *Methods2Business BV, Novi Sad, Serbia*
Miroslav Drobac - *Methods2Business BV, Eindhoven, The Netherlands*

37.4 Case Study: Right-sized Security for IoT (4:15)
Mike Eftimakis - *ARM Ltd., Cambridge, United Kingdom*

37.5 Functional verification challenges with Mixed-signal IPs (4:30)
Chirag Dhruv, **Chris Kung**, Sanket Shah - *Lattice Semiconductor Corp., San Jose, CA*

37.6 Acceleration of Cell Library Production (4:45)
Elliot E. Koch - *NVIDIA Corp., Santa Clara, CA*

Q&A poster session: Tuesday, June 7, 5:00 - 6:00pm on the Exhibit Floor.

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DESIGN/IP TRACK POSTER SESSION

Time: 5:00pm - 6:00pm || Room: Exhibit Floor || Event Type: Poster Session || Track: Design, IP
Topic Area: General Interest

During the poster presentation, you will interact directly with poster presenters in a small group setting.

As the limited time available in the Design/IP Track session program was exceeded by the quantity of great submitted content, we present the following posters in the Design/IP Track Poster Session held Tuesday, June 7 from 5:00 to 6:00pm on the Exhibit Floor.

38.1 NanoTime On-Chip Variation Methodology for High-Performance CPU Macros
Vibhor Mittal, David Newmark, Sundar Rangarajan, Teja Singh - *Advanced Micro Devices, Inc., Austin, TX*

38.2 Clock Trees with Low Process Variation
Bertram L. Bradley - *GLOBALFOUNDRIES, Austin, TX*
Gary Ellis - *Encore Semi Inc. & GLOBALFOUNDRIES, Norman, OK*
Greg Ford - *GLOBALFOUNDRIES, Santa Clara, CA*
Mark Lasher - *GLOBALFOUNDRIES, Williston, VT*

38.3 CTS Challenges for complex generated clocks
Jasmeet Singh, Sanjeev K. Meesala, Divakar Mourya - *Xilinx Inc., Hyderabad, India*

38.4 Validation of Timing Constraint Variability in Statistical Library Characterization
Suriya T. Skariah - *IBM Systems and Technology Group, Bangalore, India*
James Warnock - *IBM Corp., Yorktown Height, NY*
Vasant B. Rao - *IBM Systems and Technology Group, Poughkeepsie, NY*
Sachin K. Gupta - *IBM Systems and Technology Group, Bangalore, India*
James Sundquist - *IBM Systems and Technology Group, Essex Junction, VT*

38.5 Memristor-based Threshold Gate Adders
Lauren Guckert, Earl Swartzlander - *Univ. of Texas at Austin, TX*

38.6 Clock Domain Bridge Static Timing Analysis
Miles Simpson - *Microsoft Corp., Mountain View, CA*

38.7 Die Sizing Bound By Peripheral Bumps And IPs
Kavana V. - *Open-Silicon, Inc., Milpitas, CA*

38.9 Pruning for Macro Characterization
Wei Huang Zhu - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Lyren Brown, David Newmark - *Advanced Micro Devices, Inc., Austin, TX*

38.10 A Practical Methodology for Postroute Timing Fixing in 16nm
Xiaoyue Wang - *Huawei Technologies Co., Ltd., Kanata, ON, Canada*

38.11 Accelerate holistic and In-Context Fullchip Power Integrity analysis with Distributed Machine Process
Rishikanth Mekala - *ANSYS, Inc., Canonsburg, PA*
Ranganadh V. Mudumbai - *Xilinx Inc. & ANSYS, Inc., San Jose, CA*
Tracy Vaughan - *Xilinx Inc., Austin, TX*

38.12 Light-Weight Floorplan HTML Viewer
Andrew Bianchi, Jose A. Paredes - *IBM Corp., Austin, TX*

38.13 Power and Test Time reduction through Codec Sharing and Core Wrapping
Shiv K. Vats - *STMicroelectronics, Greater Noida, India*
Rahul Anand - *Synopsys, Inc. & Synopsys India Pvt. Ltd., Hyderabad, India*
Marco Casarsa - *STMicroelectronics S.R.L., Agrate Brianza, Italy*
Salvatore Talluto - *Synopsys Italia S.R.L., Agrate Brianza, Italy*
Harish Kumar - *STMicroelectronics, Greater Noida, India*

38.14 Maximizing Execution Efficiency by Automated Partition Convergence
Ambar Mukherji, Niraj A. Mehta - *Intel Corp., Bangalore, India*

38.15 Accelerating DFM Convergence with In-Design Pattern Fixing Flow
Karthik Krishnamoorthy, Piyush Pathak, Fadi Batarseh - *GLOBALFOUNDRIES, Santa Clara, CA*
Ahmed Omran - *GLOBALFOUNDRIES & Mentor Graphics Corp., Santa Clara, CA*
Uwe P. Schroeder - *GLOBALFOUNDRIES, Santa Clara, CA*
Ya-Chieh Lai, Jason Sweis, Jac Paul Condella, Philippe Hurat - *Cadence Design Systems, Inc., San Jose, CA*

38.16 PLL design using automatic analog migration tool
Akira Suzuki, **Nobuto Ono**, Tomoyuki Kato, Hiroyuki Rokugawa, Yukichi Todoroki, Kazuhiro Miura - *Jedat, Inc., Tokyo, Japan*

38.18 Thermal Aware FIT Computation
David Newmark, William Peterson - *Advanced Micro Devices, Inc., Austin, TX*
Kartik Iyer - *ANSYS, Inc., Austin, TX*

38.19 Voltage Drop Aware Early Power Grid Optimization on DSP core of 14nm Smartphone chip
Rajesh Mallina, Aravind Ramanujam, Manoj Gunwani - *Qualcomm India Pvt. Ltd., Bangalore, India*
Vinayakam Subramanian, Mahesh V. Yatagiri - *ANSYS, Inc., Bangalore, India*

38.32 Parameters, UVM, Coverage & Emulation – Take Two and Call Me In the Morning
Michael Horn - *Mentor Graphics Corp., Longmont, CO*
Hans van der Schoot - *Mentor Graphics Corp., Ottawa, ON, Canada*
Bryan Ramirez - *Mentor Graphics Corp., Longmont, CO*

38.35 Shifting Left – A Smart direction for emulator friendly design methodology
Manimaran N. - *Intel Corp., Bangalore, India*
Venkata S. B - *I2R-BYD Joint Lab, Bangalore, India*
Chunduri R. Mohan - *Intel Corp., Folsom, CA*
Deepmala Sachan - *Intel Corp., Bangalore, India*

38.36 Optimizing Regression Testing
Daniel Hansson - *Verifyter AB, Lund, Sweden*

38.37 A 1V 800MHz 140Kb Register File Compiler using Variation Aware Self-Timing in 40nm Bulk CMOS
Rachit V. Dave, Vivek Kumar Dikshit - *Synopsys, Inc. & Synopsys India Pvt. Ltd., Noida, India*
Prashant Dubey - *Synopsys India Pvt. Ltd., Noida, India*

DESIGN/IP TRACK POSTER SESSION

38.38 Power Sequence Verification: Free SoCs from Power Sequence Leakage Bugs
Jianfeng Liu, Minyoung Mo, Kyungtae Do - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*

38.39 A Static Approach to Verifying Isolation Clamp Values
Shang-Wei Tu - *MediaTek, Inc., Hsinchu, Taiwan*
Chia-Cheng Wu, Hsin-Pei Wang, Chun-Yao Wang - *National Tsing Hua Univ., Hsinchu, Taiwan*

38.40 Planning and Empowering Hierarchical Testing of ASICs
Kavitha Shankar, Hardik Bhagat - *GLOBALFOUNDRIES, Bangalore, India*
Kelly A. Ockunzzi - *GLOBALFOUNDRIES, Essex Junction, VT*
Richard Grupp - *GLOBALFOUNDRIES, Burlington, VT*

38.41 Augmenting Test Logic Validation usingStatic Connectivity Verification
Ambrish C. Pal, Ajay Dimri - *STMicroelectronics, Greater Noida, India*
Anuj Kumar, Navneet Chaurasia, Sami Akthar - *Synopsys, Inc., Noida, India*

WORK-IN-PROGRESS POSTER SESSION

Time: 6:00pm - 7:00pm || Room: Trinity St. Foyer || Event Type: Poster Session || Track: EDA
Topic Area: General Interest

The DAC Work-in-Progress (WIP) poster session aims to provide authors an opportunity to network with peer feedback on current work and preliminary results. Join the presenters in the Foyer for their presentations.

100.1 Eza-Secure Processor for IoT Applications
Anoop S. Dutta, Harsha N. Kondajji - *EmuPro Consulting Private Limited, Bengaluru, India*

100.2 CLB: A Compiler-assisted Look-ahead Branch-prediction for Mobile Application Processors
Kyu Jung, Paul Jung - *Adaptmicrosys LLC, Erie, PA*

100.3 A Novel Model Order Reduction Using Genetic Algorithm
Ahmed Adel - *Alexandria Univ., Alex, Egypt*
Khaled Mohamed - *Mentor Graphics Corp., Cairo, Egypt*

100.4 Protocol Capability Check using Formal
Penny Yang, Yuya Kao, Nan-Sheng Huang - *MediaTek, Inc., Hsinchu, Taiwan*
Kaowen Liu - *MediaTek, Inc., San Jose, CA*

100.5 Modeling and measuring the aging degradation of an Adaptive Frequency Scaling system
Mauricio Altieri - *CEA-LETI, Grenoble, France*
Suzanne Lesecq - *CEA-LETI Minatec & Univ. Grenoble Alpes, Grenoble, France*
Olivier Heron - *CEA-LIST, Palaiseau, France*
Edith Beigne, **Diego Puschini** - *CEA-LETI Minatec, Grenoble, France*

100.6 Design of an Interoperable Real-time Simulation (iRTS) Platform for Wireless Hardware-in-the-loop Simulations with an Autonomous Electric Vehicle
Ankurkumar Patel, Fnu Qinggele, **Yong-Kyu Jung** - *Gannon Univ., Erie, PA*

100.7 Learning-on-chip using Fixed Point Arithmetic for Neural Network Accelerators
Marcia Sahaya Louis, Thomas Unger, Jonathan Appavoo, Ajay Joshi, **Schuyler Eldridge** - *Boston Univ., Boston, MA*

100.8 Progressive Generation of Canonical Sum of Products Using a SAT Solver
Ana Petkovska - *École Polytechnique Fédérale de Lausanne, Switzerland*
David Novo - *Laboratoire d'Informatique de Robotique et de Microelectronique de Montpellier, France*
Muhsen Owaida - *École Polytechnique Fédérale de Lausanne, Switzerland*
Alan Mishchenko - *Univ. of California, Berkeley, CA*
Paolo Ienne - *École Polytechnique Fédérale de Lausanne, Switzerland*

100.9 A Fast Symbolic Transformation based Algorithm for Reversible Logic Synthesis
Mathias Soeken - *École Polytechnique Fédérale de Lausanne, Switzerland*
Gerhard W. Dueck - *Univ. of New Brunswick, Fredericton, NB, Canada*
Michael Miller - *Univ. of Victoria, BC, Canada*

100.10 A Comparative Analysis of Front-End and Back-End Compatible Silicon Photonic On-Chip Interconnects
Ishan Thakkar, Sai Vineel Reddy Chittamuru, Sudeep Pasricha - *Colorado State Univ., Fort Collins, CO*

100.11 Pelgrid: A Grid-Based Pelgrom-Inspired Model for Chip Variance
Kelly A. Livingston - *Univ. of Delaware, Elkton, MD*
Jose Mansalve Diaz, Stephane Zuckerman, Guang R. Gao - *Univ. of Delaware, Newark, DE*

WORK-IN-PROGRESS POSTER SESSION

100.12 Highly-dense Mixed Grained Reconfigurable Architecture with Via-switch
Junshi Hotate, Takashi Kishimoto, Toshiki Higashi, Hiroyuki Ochi - *Ritsumeikan Univ. & Japan Science and Technology Agency, Kusatsu, Japan*
Ryutaro Doi - *Osaka Univ. & Japan Science and Technology Agency, Suita, Japan*
Munehiro Tada, Tadahiko Sugibayashi - *NEC Corp. & Japan Science and Technology Agency, Tsukuba, Japan*
Kazutoshi Wakabayashi - *NEC Corp. & Japan Science and Technology Agency, Kawasaki, Japan*
Hidetoshi Onodera - *Kyoto Univ., Kyoto, Japan*
Yukio Mitsuyama - *Kochi Univ. & Japan Science and Technology Agency, Komi, Japan*
Masanori Hashimoto - *Osaka Univ. & Japan Science and Technology Agency, Suita, Japan*

100.13 A Dynamic MAC with prediction based bandwidth allocation mechanism for Wireless Network-on-Chip
Naseef Mansoor, Ranjith Murugesen, Avery Francois, Amlan Ganguly - *Rochester Institute of Technology, Rochester, NY*

100.14 A Hardware-based Technique for Efficient Implicit Information Flow Tracking
Jangseop Shin, Ingoo Heo - *Seoul National Univ., Seoul, Republic of Korea*
Yu-Yuan Chen - *Princeton Univ., Princeton, NJ*
Jinyong Lee - *Seoul National Univ., Seoul, Republic of Korea*
Ruby Lee - *Princeton Univ., Princeton, NJ*
Yunheung Paek - *Seoul National Univ., Seoul, Republic of Korea*

100.15 Virtual Prototyping of Smart Systems through Automatic Abstraction and Mixed-Signal Scheduling
Michele Lora, Enrico Fraccaroli - *Univ. of Verona, Italy*
Franco Fummi - *Univ. of Verona & EDALab s.r.l., Italy*

100.16 Temporal Logic Monitors as Neural Filters
Konstantin Selyunin, Denise Ratasich, Ezio Bartocci, Radu Grosu - *Vienna Univ. of Technology, Vienna, Austria*

100.17 A Configurable and Synthesizable Internet-of-Things Bus Architecture (IBUS) for Integrating Industrial Standard IPs
Xiaokun Yang, Jean H. Andrian - *Florida International Univ., Miami, FL*

100.18 Approximate C-Brain:Eliminating the Computation Redundancy in Energy-efficient Approximate Deep Learning Accelerator
Bosheng Liu, **Ying Wang**, Yinhe Han, Xin Zhao, Lili Song - *Chinese Academy of Sciences & Institute of Computing Technology, Beijing, China*
Xiaowei Li - *Institute of Computing Technology & Chinese Academy of Sciences, Beijing, China*

100.19 CMCS: Current-Mode Clock Synthesis
Riadul Islam, Matthew R. Guthaus - *Univ. of California, Santa Cruz, CA*

100.20 BaGu: Partial Computation Reuse for Approximate Computing
Xin He - *Institute of Computing Technology & Chinese Academy of Sciences & Univ. of Chinese Academy of Sciences, Beijing, China*
Guihai Yan - *Institute of Computing Technology, Beijing, China*
Yinhe Han, Xiaowei Li - *Chinese Academy of Sciences & Institute of Computing Technology, Beijing, China*

100.21 A Refinement-Based Approach to Testing of Hardware and Low-level Software Designs
Mitesh Jain, Panagiotis Manolios - *Northeastern Univ., Boston, MA*

100.22 Lithography Hotspot Detection using Histogram of Oriented Light Propagation and Two-Staged Cascade Classifier
Yoichi Tomioka - *Univ. of Aizu, Aizu-Wakamatsu City, Japan*
Tetsuaki Matsunawa, Chikaaki Kodama, Shigeki Nojima - *Toshiba Corp., Yokohama, Japan*

100.23 Bi-objective Optimization of Performance and Energy for Applications Mapping on CGRAs
Jiangyuan J. Gu, Shouyi Yin, Leibo L. Liu, Shaojun S. Wei - *Tsinghua Univ., Beijing, China*

100.24 Evaluation of Synchronous Dataflow Graph Mappings onto Distributed Memory Architectures
Youen Lesparre, Alix Munier Kordon - *LIP6 Laboratory, CNRS, Univ. Pierre et Marie Curie, Paris, France*
Jean-Marc Delosme - *Univ.d'Evry-Val-d'Essonne, France*

100.25 Voltage Noise Induced DRAM Soft Error Reduction Technique for 3D-CPUs
Tiantao Lu, Caleb M. Serafy, **Zhiyuan Yang**, Ankur Srivastava - *Univ. of Maryland, Collge Park, MD*

100.26 Adaptive Frame-Rate Optimization for Low Energy Object Tracking
Yusuke Inoue, Takatsugu Ono, Koji Inoue - *Kyushu Univ., Fukuoka, Japan*

100.27 A Case for Standard-Cell Based RAMs in Highly-Ported Superscalar Processor Structures
Sungkwan Ku, Elliott Forbes, Rangeen Basu Roy Chowdhury, Eric Rotenberg - *North Carolina State Univ., Raleigh, NC*

100.28 XMAT: A 6T XOR-MAT based 2R-1W SRAM for High Bandwidth Network Applications
Ramandeep Kaur - *STMicroelectronics, New Delhi, India*
Alexander Fell - *Indian Institute of Science, New Delhi, India*
Harsh Rawat - *STMicroelectronics, Greater Noida, India*

100.29 Diagnosis for Defective Reconfigurable Single-Electron Transistor Arrays
Yun-Jui Li, **Ching-Yi Huang** - *National Tsing Hua Univ., Hsinchu, Taiwan*
Yung-Chih Chen - *Yuan Ze Univ., Taoyuan, Taiwan*
Chun-Yao Wang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Vijaykrishnan Narayanan, Suman Datta - *Pennsylvania State Univ., University Park, PA*

100.30 A Data Locality-aware Design Framework for Reconfigurable Sparse Matrix-Vector Multiplication Kernel
Sicheng Li, Yandan Wang - *Univ. of Pittsburgh, PA*
Wujie Wen - *Florida International Univ., Miami, FL*
Yu Wang - *Tsinghua Univ., Beijing, China*
Qinru Qiu - *Syracuse Univ., Syracuse, NY*
Yiran Chen, Hai Li - *Univ. of Pittsburgh, PA*

100.31 Algorithm Recognition to Support Embedded Code Optimization
Maria H. Rodriguez Blanco, Gerd Ascheid, Rainer Leupers - *RWTH Aachen Univ., Aachen, Germany*

100.32 Crypt-Delay: Encrypting IP Cores with Capabilities for Gate-level Logic and Delay Simulations
Parameswaran Ramanathan, Kewal K. Saluja - *Univ. of Wisconsin, Madison, WI*

100.33 Generation and Use of Statistical Timing Macro-models considering Slew and Load Variability
Debjit Sinha - *IBM Corp., Poughkeepsie, NY*
Vladimir Zolotov - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Jin Hu - *IBM Corp., Hopewell Junction, NY*
Sheshashayee K. Raghunathan - *IBM Corp., Bangalore, India*
Adil Bhanji - *IBM Corp., Poughkeepsie, NY*
Christine Casey - *IBM Corp., Research Triangle Park, NC*

100.34 Exploring Flash Devices to Implement Digital Circuits
Monther Abusultan, Sunil Khatri - *Texas A&M Univ., College Station, TX*

WORK-IN-PROGRESS POSTER SESSION

100.35 VeMap: Automatic Indoor Floor Map Construction via Smartphone-based Vehicle Tracking
Ruipeng Gao, **Guojie Luo** - *Peking Univ., Beijing, China*
Fan Ye - *Stony Brook Univ., Stony Brook, New York*

100.36 An Energy-Efficient Computational Reliability Model for Dynamically Evolving Human-Centered Monitoring
Ramyar Saeedi - *Wright State Univ., Pullman, WA*
Ramin Fallahzadeh, Parastoo Alinia, Hassan Ghasemzadeh - *Washington State Univ., Pullman, WA*

100.37 Synchronous Independent Write Cache: A Novel SSD-aware Write Cache for RAID
Junghee Lee - *Univ. of Texas at San Antonio, TX*
Youngjae Kim - *Ajou Univ., Suwon, Republic of Korea*
Kalidas Ganesh - *Univ. of Texas at San Antonio, TX*
Joon-Young Paik - *Ajou Univ., Suwon, Republic of Korea*

100.38 Exact Timing Analysis for Concurrent Systems
Wenmian Hua, Rajit Manohar - *Cornell Univ., Ithaca, NY*

100.39 DFT and ATPG of Two-pattern Tests for Dual-rail Asynchronous Circuits
Ying-Hsu Wang, Kuan-Yen Huang, **Ting-Yu Shen**, James Chien-Mo Li - *National Taiwan Univ., Taipei City, Taiwan*

100.40 Fabric: Mobile SOC Chip Level Aging Design Methodology for Advanced FinFET Technologies
Yiwei Fu, Yongsheng Sun, Jianping Guo, Canhui Zhan, Jun Xia - *HiSilicon, Shenzhen, China*
Junhui Zhao - *ANSYS, Inc., Shenzhen, China*
Teong Ming Chenah - *Apache Design, Inc., A Subsidiary of ANSYS, Inc., Shanghai, China*

100.41 A Dynamic Latency-Aware Load-Balanced Strategy in 2.5D NoC Architecture
Chen Li, Sheng Ma, Yang Guo - *National Univ. of Defense Technology, Changsha, China*
Xia Zhao - *Ghent Univ. & National Univ. of Defense Technology, Ghent, Belgium*

100.42 Hardware Trojan Localization using Polynomials
Farimah Farahmandi, Yuanwen Huang, **Prabhat Mishra** - *Univ. of Florida, Gainesville, FL*

100.43 3D Floorplanning with Timing-Driven Voltage Assignment
Johann Knechtel, Abdullah M. Heyari, Ibrahim (Abe) Elfadel - *Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates*
Jens Lienig - *Technische Univ. Dresden, Germany*

100.44 3D-SHIELD: 3D Security Layers for Protecting Thermal Side-Channel Leakage
Peng Gu, Dylan Stow, Russell Barnes - *Univ. of California, Santa Barbara, CA*
Eren Kursun - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Yuan Xie - *Univ. of California, Santa Barbara, CA*

100.45 Neuro-noc: Neural Network based Predictive Routing for Network-on-Chip Architectures
Michel A. Kinsy - *Univ. of Oregon & Massachusetts Institute of Technology, Eugene, OR*
Sena A. Koehnen, **Shreeya Khadka**, Brian J. Gravelle - *Univ. of Oregon, Eugene, OR*

100.46 The Design and Implementation of a 4Kb STT-MRAM with Innovative 200nm Nano-ring Shaped MTJs
Zheng Li, Xiuyuan Bi - *Univ. of Pittsburgh, PA*
Jianying Qin, Peng Guo, Wenjie Kong, Wenshan Zhan, Xiufeng Han - *Chinese Academy of Sciences, Beijing, China*
Hong Zhang, Lingling Wang, Hanming Wu - *Semiconductor Manufacturing International Corp., Shanghai, China*
Hai Li, **Yiran Chen** - *Univ. of Pittsburgh, PA*

100.47 Split-Manufacturing of Printed Circuit Boards
Anirudh S. Iyengar - *Univ. of South Florida, Tampa, FL*
Fengchao Zhang - *Univ. of Florida, Gainesville, FL*
Swaroop Ghosh - *Univ. of South Florida, Tampa, FL*
Swarup Bhunia - *Univ. of Florida, Gainesville, FL*

100.48 Design Space Exploration on Accelerator-Rich Heterogeneous Architecture
Liang Wang, Kevin Skadron - *Univ. of Virginia, Charlottesville, VA*

100.49 Realizing Erase-free SLC Flash Memory with Rewritable Programming Design
Yu-Ming Chang, Yung-Chun Li, Ping-Hsien Lin, Hsiang-Pang Li, - *Macronix International Co., Ltd., Hsinchu, Taiwan*
Yuan-Hao Chang - *Academia Sinica, Taipei, Taiwan*

100.50 HAP: a Heterogeneity-Conscious Runtime System for Adaptive Pipeline Parallelism
Jinsu Park, Woongki Baek - *Ulsan National Institute of Science and Technology (UNIST), Ulsan, Republic of Korea*

100.51 Model Based Guiding Pattern Synthesis for Robust and On-Target Directed Self-Assembly
Joydeep Mitra - *Mentor Graphics Corp. & Univ. of Texas at Austin, Austin, TX*
Andres Torres - *Mentor Graphics Corp., Wilsonville, OR*
Yuansheng Ma - *Mentor Graphics Corp., Fremont, CA*
David Z. Pan - *Univ. of Texas at Austin, TX*

100.52 IO Scheduling with Reduced Mapping Cache Overhead in Flash Based Storage Systems
Cheng Ji, Chao Wu - *City Univ. of Hong Kong, Hong Kong*
Li-Pin Chang - *National Chiao Tung Univ., Hsinchu, Taiwan*
Liang Shi - *Chongqing Univ., Chongqing, China*
Chun Jason Xue - *City Univ. of Hong Kong, Hong Kong*

100.53 TinySPICE+: Scaling Up Statistical SPICE Simulations on GPU Leveraging Shared-Memory Based Sparse Matrix Solution Techniques
Lengfei Han, Zhuo Feng - *Michigan Technological Univ., Houghton, MI*

100.54 A Case for Active Interposers: Modeling and Analysis of Interposer Resiliency Requirements
Taniya H. Siddiqua, **Gabriel H. Loh** - *Advanced Micro Devices, Inc., Bellevue, WA*

100.55 Towards Formal Verification of Circuits Reliability Using SMT-Based Techniques
Ghaith Bany Hamad - *École Polytechnique de Montréal, QC, Canada*
Ghaith Kazma, Otmane Ait Mohamed - *Concordia Univ., Montreal, QC, Canada*
Yvon Savaria - *École Polytechnique de Montréal, QC, Canada*

WEDNESDAY, JUNE 8

KEYNOTE: THE CHALLENGE TO DEVELOP TRULY GREAT PRODUCTS

Mark Papermaster - *Advanced Micro Devices, Inc., Sunnyvale, CA*

Time: 9:00am - 10:00am || Room: Ballroom A || Track: Design, EDA
Topic Area: General Interest

Mark Papermaster, CTO and SVP of Technology and Engineering at AMD, will take a closer look at various challenges companies face when they set out to build winning products. Drawing up on more than 30 years of engineering experience, Mark explores innovation and what defines a great product, as well as his thoughts on the role of leadership to create an environment to enable both disruptive thinking combined with strong execution. He will describe three key elements, along with examples of his experience at IBM, Apple, Cisco, and AMD.

The first is goal clarity and definition that will distinguish the design as a great product. This requires discipline to think through not just the product itself, but how it will be used. The experience matters. The high level design then has to be rigorous to lay out a plan of the enabling factors, and the big problems to be solved.

Second is establishing a team that's set up for success. Plotting out the right leadership, skills, geography, and culture is key.

Finally, execution always has to be prioritized. You can't afford to miss the product's market window. What you measure and milestone is what you care about – it sets the behavior of the team.

Mark will summarize by highlighting how the evolution of innovation and great products of the last several decades has set the stage for a huge inflection point in computing. We are now entering the era of immersive computing which will fundamentally change the role computing plays in our daily lives.

Biography: Mark Papermaster is chief technology officer and senior vice president at AMD, responsible for corporate technical direction, and AMD intellectual property (IP) and system-on-chip (SOC) product research and development. His more than 30 years of engineering experience includes significant leadership roles managing the development of a wide range of products, from mobile devices to high-performance servers. Before joining AMD in October 2011, Papermaster was the leader of Cisco's Silicon Engineering Group, the organization responsible for silicon strategy, architecture, and development for the company's switching and routing businesses.

In prior roles, Papermaster served as Apple senior vice president of Devices Hardware Engineering, where he was responsible for the iPod products, and iPhone hardware development. He also held a number of senior leadership positions at IBM, serving on the company's Technical Leadership Team and overseeing development of the company's key microprocessor and server technologies.

Specializing in electrical engineering, Papermaster received his bachelor's degree from the University of Texas and master's degree from the University of Vermont. He is a member of the University of Texas Cockrell School of Engineering Advisory Board, Olin College Presidents Council, and the Juvenile Diabetes Research Foundation.

39 ACCELERATED SIMULATION FOR CIRCUIT RELIABILITY AND STABILITY

Time: 10:30am - 12:00pm || Room: 12AB || Event Type: Reviewed Presentations || Track: EDA
Topic Area: Modeling, Simulation & Timing

CHAIR:
Sheldon X.-D. Tan - *Univ. of California, Riverside, CA*

CO-CHAIR:
Janet Meiling Roveda - *Univ. of Arizona, Tucson, AZ*

The analysis of circuit stability and reliability is increasingly important, especially for large-scale designs. This session's topics include power supply stability, soft error in logic circuits, thermal noise in ultra-low voltage designs, and the sparsification of spectral graphs used in various design problems.

*** Indicates Best Paper Candidate**

39.1 Distributed On-chip Voltage Regulation: Theoretical Stability Foundation, Over-design Reduction and Performance Optimization* (10:30)
Xin Zhan, Peng Li, Edgar Sanchez-Sinencio - *Texas A&M Univ., College Station, TX*

39.2 Accelerating Soft-Error-Rate (SER) Estimation in the Presence of Single Event Transients (10:45)
Ji Li - *Univ. of Southern California, Los Angeles, CA*
Jeffrey Draper - *Univ. of Southern California, Marina del Rey, CA*

39.3 A Fast Simulator for the Analysis of Sub-Threshold Thermal Noise Transients (11:00)
Marco Donato, R. Iris Bahar, William Patterson, Alexander Zaslavsky - *Brown Univ., Providence, RI*

39.4 Spectral Graph Sparsification in Nearly-Linear Time Leveraging Efficient Spectral Perturbation Analysis (11:15)
Zhuo Feng - *Michigan Technological Univ., Houghton, MI*

A Q&A poster session will immediately follow the presentations from 11:30am to 12:00pm.

40 IMPROVING TEST EFFICIENCY

Time: 10:30am - 12:00pm || Room: 19AB || Event Type: Reviewed Presentations || Track: EDA
Topic Area: Test & Verification, Modeling, Simulation & Timing

CHAIR:
Janusz Rajski - *Mentor Graphics Corp., Portland, OR*
Hai Zhou - *Northwestern Univ., Evanston, IL*

This session presents a new delay testing and configuration approach to a new probing scheme for wafer-scale chips to reduce the cost of probes, a new approach to reduce the overhead of response compaction by exploiting x-value correlation, improvement of chip yield and lifetime under delay variations and aging, and a new late-stage approach for scan chain design.

*** Indicates Best Paper Candidate**

40.1 Efficient Probing Schemes for Fine-Pitch Pads of InFO Wafer-Level Chip-Scale Package (10:30)
Yu-Chieh Huang, Bing-Yang Lin, Cheng-Wen Wu - *National Tsing Hua Univ., Hsinchu, Taiwan*
Mincent Lee, Hao Chen, Hung-Chih Lin, Ching-Nen Peng, Min-Jer Wang - *Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan*

40.2 Reducing Control Bit Overhead for X-Masking/X-Canceling Hybrid Architecture via Pattern Partitioning (10:45)
Jin-Hyun Kang - *Sungkyunkwan Univ., Suwon, Republic of Korea*
Nur Touba - *Univ. of Texas at Austin, TX*
Joon-Sung Yang - *Sungkyunkwan Univ., Suwon, Republic of Korea*

40.3 EffiTest: Efficient Delay Test and Statistical Prediction for Configuring Post-silicon Tunable Buffers (11:00)
Grace Li Zhang, Bing Li, Ulf Schlichtmann - *Technische Univ. München, Germany*

40.4 Comprehensive Optimization of Scan Chain Timing During Late-Stage IC Implementation (11:15)
Kun Young Chung, Andrew B. Kahng, **Jiajia Li** - *Univ. of California at San Diego, La Jolla, CA*

A Q&A poster session will immediately follow the presentations from 11:30am to 12:00pm.

41 TACKLING REAL-WORLD CHALLENGES: PERFORMANCE, RELIABILITY AND POWER IN MEMORY

Time: 10:30am - 12:00pm || Room: 17AB || Event Type: Reviewed Presentations
Track: Embedded Systems || Topic Area: System Architectures & SoC

CHAIR:
Chun Jason Xue - *City Univ. of Hong Kong, Hong Kong*
CO-CHAIR:
Hyung Gyu Lee - *Daegu Univ., Republic of Korea*

Continued scaling and developments in memory devices impose significant challenges on using these devices in practice. This session tackles some of the most prominent limitations faced in the field today, in terms of performance, reliability and power, contributing real-world solutions for real-world challenges. The topics include reducing power through lossy encoding, improving lifetime and performance of NAND storage, prefetching in coarse-grain reconfigurable architectures, and partitioning memory for better bandwidth utilization in GPUs.

*** Indicates Best Paper Candidate**

41.1 Reducing Serial I/O Power in Error-Tolerant Applications by Efficient Lossy Encoding (10:30)
Phillip Stanley-Marbell, Martin Rinard - *Massachusetts Institute of Technology, Cambridge, MA*

41.2 Improving Performance and Lifetime of NAND Storage Systems Using Relaxed Program Sequence* (10:45)
Jisung Park, Jaeyong Jeong - *Seoul National Univ., Seoul, Republic of Korea*
Sungjin Lee - *Massachusetts Institute of Technology, Cambridge, MA*
Youngsun Song, Jihong Kim - *Seoul National Univ., Seoul, Republic of Korea*

41.3 Data Cache Prefetching via Context Directed Pattern Matching for Coarse-Grained Reconfigurable Arrays (11:00)
Chen Yang, Leibo Liu, Shouyi Yin, Shaojun Wei - *Tsinghua Univ., Beijing, China*

41.4 TEMP: Thread Batch Enabled Memory Partitioning for GPU (11:15)
Mengjie Mao - *Univ. of Pittsburgh, PA*
Wujie Wen - *Florida International Univ., Miami, FL*
Xiaoxiao Liu - *Univ. of Pittsburgh, PA*
Jingtong Hu - *Oklahoma State Univ., Stillwater, OK*
Danghui Wang - *Northwestern Polytechnical Univ., Xi'an, China*
Yiran Chen, Hai Li - *Univ. of Pittsburgh, PA*

A Q&A poster session will immediately follow the presentations from 11:30am to 12:00pm.

42 HARDWARE VERIFICATION OF SECURITY ASPECTS

Time: 10:30am - 12:00pm || Room: 18AB || Event Type: Invited Presentations
Track: EDA, Security || Topic Area: Test & Verification, System Architectures & SoC

CHAIR:
Prabhat Mishra - *Univ. of Florida, Gainesville, FL*
ORGANIZER:
Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

The world of hardware-security vulnerabilities is built primarily upon the bugs in our designs. Thus, there is a great opportunity for the verification community to become involved in the development of more secure hardware. However, this goal requires a redirection of efforts beyond traditional functional verification bugs, and towards security vulnerability bugs. Speakers in the session will highlight the differences between these two worlds and demonstrate how core verification talents can help deliver secure designs.

42.1 Security Challenges and Strategies in High Volume ICs (10:30)
Dhinesh Manoharan, Sohrab Aftabjahani - *Intel Corp., Portland, OR*

42.2 Scalable Formal Methods for Hardware Security Verification (11:00)
Rajeev Ranjan, Victor Markus Purri, Fernanda Braga - *Cadence Design Systems, Inc., San Jose, CA*

42.3 Specification and Modeling for Systems-on-Chip Security Verification (11:30)
Sharad Malik, Pramod Subramanyan - *Princeton Univ., Princeton, NJ*

43 ENABLING THE INTERNET OF THINGS: CONTEXT-AWARENESS IN SENSING, COMMUNICATION AND COMPUTING

Time: 10:30am - 12:00pm || Room: 18CD || Event Type: Invited Presentations || Track: IoT, Design
Topic Area: Codesign & System Design, Cyber-Physical Systems, Emerging Technologies

CHAIR:
Rangharajan Venkatesan - *NVIDIA Corp., San Jose, CA*

ORGANIZER:
Shreyas Sen - *Purdue Univ., West Lafayette, IN*

Realizing the IoT vision of tens of billions of connected devices requires significant changes in the computing paradigm. At the edges of the network, leaf node devices will need to respond to rapid changes in operating conditions and computational/communication demands, while simultaneously controlling energy consumption. Self-learning systems possess these attributes and show strong promise for the IoT. This special-session will present recent advances of such context-aware, self-learning systems for IoT, each talk going into the sensing, communication and computation, respectively. The first talk highlights the challenges and opportunities of data acquisition in IoT nodes and focus on intelligent sensors (speech and vision). The second talk presents advances in context-adaptive communication to support widely varying IoT data loads. The third talk discusses novel analog structures that are able to self-learn and perform neuromorphic computations.

43.1 "Always On" Sensors for the Internet of Smart Things (10:30)
Arijit Raychowdhury, Soham Desai, Anvesha Amravati, Ningyuan Cao - *Georgia Institute of Technology, Atlanta, GA*

43.2 Context-Aware Energy-Efficient Communication for IoT Sensor Nodes (11:00)
Shreyas Sen - *Purdue Univ., West Lafayette, IN*

43.3 Online Learning and Neuromorphic Computing Using Memristors (11:30)
Wei Lu - *Crossbar, Inc. & Univ. of Michigan, Santa Clara, CA*

44 DESIGN TRACK: SIMULATION AND FORMAL: THE BEST OF BOTH WORLDS

Time: 10:30am - 12:00pm || Room: Ballroom E || Event Type: Reviewed Presentations
Track: Design || Topic Area: Test & Verification, Modeling, Simulation & Timing

CHAIR:
Jennifer Hwang - *QuickLogic Corp., Sunnyvale, CA*

A verification engineer has many tricks in his/her bag when hunting down that elusive bug. Not any one approach can cover it all. Listen to different techniques and solutions from simulation to formal to SVA and add new tricks to your verification bag of "tricks."

44.1 Case Study of End-to-End Formal Verification Methodology (10:30)
Jake Maas, Nirabh Regmi, Krishnan Palaniswami, Ashish Kulkarni - *Microsoft Corp., Redmond, WA*

44.2 Bus verification automation platform for complex bus scenario (10:45)
Junxia Wang, Eve Wang, Yunyang Song, Wenting Hou, **Kaowen Liu** - *MediaTek, Inc., Beijing, China*

44.3 Formal Verification Techniques For Predictable And Accelerated Giga-Scale SOC Design Closure Avoiding Gate-Level Simulation (11:00)
Satish Kumar Rompicharla, Kundan Kumar, Srikanth Nimmagadda, Shankar R. Sawant - *Intel Corp., Bangalore, India*

44.4 Static Analysis of Uncoverable code – Accelerate Formal & Simulation Sign off (11:15)
Deepanjan Roy - *NVIDIA Corp., Bangalore, India*
Raja Mahadevan, Sanjana Bhattacharya - *Synopsys India Pvt. Ltd., Bangalore, India*

44.5 Verifying Design Hotspots with SystemVerilog Checkers (11:30)
Roger Sabbagh - *Huawei Technologies Co., Ltd., Ottawa, ON, Canada*
Ping Yeung - *Mentor Graphics Corp., Fremont, CA*

44.6 It's about Time: Verifying Clocks Using Formal (11:45)
Ashish Darbari - *Imagination Technologies Ltd., Kings Langley, United Kingdom*

Q&A Poster Session
Wednesday, June 8, 5:00 - 6:00pm - Exhibit Floor

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45 DESIGN TRACK: BACK-END DESIGN TOOLS & TECHNIQUES- INNOVATION INCREASING DESIGN EFFICIENCY

Time: 10:30am - 12:00pm || Room: Ballroom F || Event Type: Reviewed Presentations
Track: EDA, Design || Topic Area: Physical Design, Modeling, Simulation & Timing

CHAIR:
Gary Ellis - *Encore Semi Inc., Norman, OK*

This session will cover various techniques utilized to create a more efficient design. Subjects range from adaptive power grids, to modular approach for physical implementation, to incremental clock network tuning for lower latency and better skew. Also covered in this session will be large-scale hierarchical issues like testability and re-use, as well as wiring resource sharing across hierarchical boundaries.

45.1 Modular Approach to Physical Implementation of Core and Cache Infrastructure on POWER8 (10:30)
Ryan M. Kruse, Ryan Nett, Gerald Strevig, Amanda Venton, Arkadiusz Slanda, Christopher J. Catalino, Joan Maharas - *IBM Systems and Technology Group, Austin, TX*

45.2 Multi-objective Incremental Clock Network Optimization Using Multiple Voltage Threshold Technique (10:45)
Sangdo Park - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Hyung-Ock Kim, Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*

45.3 A Convergent Pin Optimization Methodology for Hierarchical Design Closure (11:00)
Shyam Ramji - *IBM Systems and Technology Group, Poughkeepsie, NY*
Randall J. Darden - *IBM Systems and Technology Group, Springfield, MO*
Eddy St Juste, Christopher J. Berry - *IBM Systems and Technology Group, Poughkeepsie, NY*

45.4 Design Methodology Targeting Clock Propagation Issues for Quick and Reliable Signoff (11:15)
Pawan Sehgal - *STMicroelectronics, Greater Noida, India*
Aditi Sharma - *STMicroelectronics, New Delhi, India*
Rangarajan Ramanujam, Akhilesh Chandra Mishra - *STMicroelectronics, Greater Noida, India*
Sujay Deb - *Indraprastha Institute of Information Technology, Delhi, India*

45.5 Strategies for Sharing Design Resources through Chip Hierarchy (11:30)
Ryan M. Kruse, Ryan Nett, **Gerald Strevig**, Amanda Venton, Arkadiusz Slanda, Christopher J. Catalino, Joan Maharas, Rashmi Finavia - *IBM Systems and Technology Group, Austin, TX*

45.6 Approaches for automated and reusable IP functional test rule development across multiple instances of IP within and across ASIC designs (11:45)
Malinky Ghosh - *GLOBALFOUNDRIES, Wappingers Falls, NY*
Kelly Ockunzzi - *GLOBALFOUNDRIES, Burlington, VT*

Q&A Poster Session
Wednesday, June 8, 5:00 - 6:00pm - Exhibit Floor

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46 IP TRACK: SYSTEM IP CONFIGURATION AND VERIFICATION

Time: 10:30am - 11:00am || Room: Ballroom G || Event Type: Reviewed Presentations
Track: IP, IP || Topic Area: Test & Verification, Circuit Design, System Architectures & SoC

CHAIR:
Priyank Shukla - *Cadence Design Systems, Inc., San Jose, CA*

Join us as we explore how Intelligent IP Configuration and Verification of Infinitely Configurable Cache Coherent Interconnect IP's can improve system design for our modern IP Engineers.

46.1 Intelligent IP Configuration (10:30)
Simon Rance - *ARM Ltd., Plano, TX*
David Murray - *ARM Ltd., Galway, Ireland*

46.2 Verification of infinitely configurable cache coherent interconnect IP (10:45)
Rohit Bansal - *Arteris, Inc., Campbell, CA*

Q&A Poster Session
Wednesday, June 8, 5:00 - 6:00pm - Exhibit Floor

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47 IP TRACK: OPEN SOURCE: SOFTWARE, MODULES, SYSTEMS, AND NOW IP AND CHIPS?

Time: 11:00am - 12:00pm || Room: Ballroom G || Event Type: Panel || Track: IP, Design
Topic Area: General Interest, Business

MODERATOR:

Don Dingee - *SemiWiki.com, San Antonio, TX*

ORGANIZER:

Priyank Shukla - *Cadence Design Systems, Inc., San Jose, CA*

Open source code transformed software development, and spawned makers with low-cost hardware modules, mostly running on proprietary chips. Large systems are moving toward open source - still, mostly on proprietary chips. Open source processor core IP is now causing a stir. Is "open" an inevitable future for chips, a change the industry needs? Does co-optimizing open source software and hardware IP have benefits, pre-silicon? Or is open source IP a distraction, a model that will not work on a large scale? What lessons from other open efforts may help decide? Our panel will share their experience, observations, and predictions.

PANELISTS:

John Leidel - *Texas Tech Univ., Lubbock, TX*
Randy Swanberg - *IBM Corp., Austin, TX*
Paul Teich - *TIRIAS Research, Austin, TX*
Aaron Sullivan - *Rackspace US, Inc., Austin, TX*
Chris Aniszczyk - *Cloud Native Computing Foundation & Linux Foundation, Austin, TX*

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SKY TALK: SECURITY AT DIFFERENT LAYERS OF ABSTRACTIONS: APPLICATION, OPERATING SYSTEMS, AND HARDWARE

Time: 1:00pm - 1:30pm || Room: DAC Pavilion - Booth 1839 || Event Type: SKY Talk
Track: Security, Embedded Systems || Topic Area: Business

When it comes to computer security, attackers often seek out weaknesses at the abstraction boundaries in a system. Therefore, boundaries between layers such as the hardware, operating system, and application have a significant security impact. This talk will address how security is influenced by different dimensions of computing including hardware and software abstractions and scale, along with how threat models can help to manage this complexity.

It concludes with a perspective on the largest security problems of the day: the ability for one entity to prove their security posture to another, simplifying security, and addressing the talent shortage. This talk is accessible to anyone interested in security and how it impacts the broad computing ecosystem.

SPEAKER:

Bryan Payne - *Netflix, Los Gatos, CA*

48 ESCAPE FROM DESIGN MEDIOCRITY - BETTER TOOLS FOR POWER AND RELIABILITY

Time: 1:30pm - 3:00pm || Room: 12AB || Event Type: Reviewed Presentations
Track: EDA, Embedded Systems || Topic Area: System Architectures & SoC, Low-Power & Reliability

CHAIR:

Franco Fummi - *Univ. of Verona, Italy*

CO-CHAIR:

Massimo Poncino - *Politecnico di Torino, Italy*

The session presents novel solutions to enable more accurate modeling and analysis of power and reliability aspects of a design. The presentations range from surveying techniques for reliability and soft-errors, to modeling short-term aging effects and STT-RAM devices, and extensions to architectural simulators to model power-supply noise.

*** Indicates Best Paper Candidate**

48.1 CLEAR: Cross-Layer Exploration for Architecting Resilience - Combining Hardware and Software Techniques to Tolerate Soft Errors in Processor Cores (1:30)
Eric Cheng - *Stanford Univ. Stanford, CA*
Shahrzad Mirkhani - *Stanford Univ. & Univ. of Texas at Austin, Stanford, CA*
Lukasz Szafaryn - *Univ. of Virginia, Charlottesville, VA*
Chen-Yong Cher - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Hyungmin Cho - *Stanford Univ., Stanford, CA*
Kevin Skadron, Mircea R. Stan - *Univ. of Virginia, Charlottesville, VA*
Klas Lilja - *Robust Chip Inc., Pleasanton, CA*
Jacob Abraham - *Univ. of Texas at Austin, TX*
Pradip Bose - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Subhasish Mitra - *Stanford Univ., Stanford, CA*

48.2 Designing Guardbands for Instantaneous Aging Effects (1:45)
Victor M. van Santen, Hussam Amrouch - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Javier Martin Martinez, Montserrat Nafria - *Univ. Autònoma de Barcelona, Bellaterra, Spain*
Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

48.3 NVSim-VXs: An Improved NVSim for Variation Aware STT-RAM Simulation (2:00)
Enes Eken, LingHao Song, Ismail Bayram - *Univ. of Pittsburgh, PA*
Cong Xu - *Hewlett-Packard Labs., Palo Alto, CA*
Wujie Wen - *Florida International Univ., Miami, FL*
Yuan Xie - *Univ. of California, Santa Barbara, CA*
Yiran Chen - *Univ. of Pittsburgh, PA*

48.4 A Novel Cross-Layer Framework for Early-Stage Power Delivery and Architecture Co-Exploration* (2:15)
Cheng Zhuo - *Zhejiang Univ., Hangzhou, China*
Kassan Unda, Yiyu Shi - *Univ. of Notre Dame, IN*
Wei-Kai Shih - *Intel Corp., Hillsboro, OR*

A Q&A poster session will immediately follow the presentations from 2:30pm to 3:00pm.

49 DR. GARBLE AND MR. LEAKAGE IN THE MYSTERY OF SECURE CPUs

Time: 1:30pm - 3:00pm || Room: 19AB || Event Type: Reviewed Presentations Track: Security, Embedded Systems || Topic Area: System Architectures & SoC, System Software, Modeling, Simulation & Timing

CHAIR:
Anand Rajan - *Intel Corp., Hillsboro, OR*

CO-CHAIR:
Daniel Holcomb - *Univ. of Massachusetts, Amherst, MA*

This session highlights the urgency of addressing information leakage from processors. It presents leakage prevention techniques such as garbled processor architectures, cache partitioning and cryptographic control flow integrity.

*** Indicates Best Paper Candidate**

49.1 A High-resolution Side-Channel Attack on Last Level Cache* (1:30)
Mehmet Kayaalp - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Nael Abu-Ghazaleh - *Univ. of California, Riverside, CA*
Dmitry Ponomarev - *SUNY Binghamton, NY*
Aamer Jaleel - *NVIDIA Corp. Wesfford, MA*

49.2 Garbled CPU: A MIPS Processor for Secure Computation in Hardware (1:45)
Ebrahim M. Songhori - *Rice Univ., Houston, TX*
Shaza Zeitouni, Ghada Dessouky, Thomas Schneider,
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*
Farinaz Koushanfar - *Univ. of California at San Diego, La Jolla, CA*

49.3 SecDCP: Secure Dynamic Cache Partitioning for Efficient Timing Channel Protection (2:00)
Yao Wang - *Cornell Univ., Johnson City, NY*
Andrew Ferraiuolo - *Cornell Univ., Ithaca, NY*
Danfeng Zhang - *Pennsylvania State Univ., University Park, PA*
Andrew Myers, Edward Suh - *Cornell Univ., Ithaca, NY*

49.4 Physical Unclonable Functions-based Linear Encryption against Code Reuse Attacks (2:15)
Pengfei Qiu, Yongqiang Lyu - *Tsinghua Univ., Beijing, China*
Jiliang Zhang, Xingwei Wang - *Northeastern Univ., Shenyang, China*
Di Zhai - *Beijing Univ. of Posts and Telecommunications, Beijing, China*
Dongsheng Wang - *Tsinghua Univ., Beijing, China*
Gang Qu - *Univ. of Maryland, College Park, MD*

A Q&A poster session will immediately follow the presentations from 2:30pm to 3:00pm.

50 MOORE'S LAW MARCHING ON - CIRCUIT TECHNIQUES BEYOND TRADITIONAL CMOS

Time: 1:30pm - 3:00pm || Room: 17AB || Event Type: Reviewed Presentations || Track: Design Topic Area: Circuit Design, Low-Power & Reliability

CHAIR:
Peng Li - *Texas A&M Univ., College Station, TX*

CO-CHAIR:
Chen-Yong Cher - *IBM T.J. Watson Research Center, Yorktown Heights, NY*

Dennard scaling has stopped, but Moore's law must march on! Several technology alternatives are competing to take the crown as successor to traditional CMOS, but each brings a host of new circuit design challenges. This session presents four such alternatives along with their risks and circuit solutions: near threshold FinFETs, monolithic 3D integration, voltage stacking, and ultra-thin body FD-SOI.

50.1 Near-Threshold Computing in FinFET Technologies: Opportunities for Improved Voltage Scalability (1:30)
Nathaniel Pinckney - *Univ. of Michigan, Ann Arbor, MI*
Lucian Shifren - *ARM Ltd., San Jose, CA*
Brian Cline - *ARM Ltd., Austin, TX*
Saurabh Sinha - *ARM, Inc., Austin, TX*
Supreet Jeloka, Ronald Dreslinski, Trevor Mudge, Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

50.2 Match-making for Monolithic 3D IC: Finding the Right Technology Node (1:45)
Kyungwook Chang - *Georgia Institute of Technology, Atlanta, GA*
Saurabh Sinha - *ARM, Inc., Austin, TX*
Brian Cline - *ARM Ltd., Austin, TX*
Greg Yeric - *ARM, Inc., Austin, TX*
Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*

50.3 Lower Power by Voltage Stacking: A fine-grained System Design Approach (2:00)
Kristof Blutman, Ajay Kapoor, Jacinto Garcia Martinez, Hamed Fatemi, José Pineda de Gyvez - *NXP Semiconductors, Eindhoven, The Netherlands*

50.4 Leveraging FDSOI through Body Bias Domain Partitioning and Bias Search (2:15)
Johannes M. Kuehn - *Eberhard Karls Univ. Tubingen & Keio Univ., Tuebingen, Germany*
Hideharu Amano - *Keio Univ., Yokohama, Japan*
Oliver Bringmann - *Univ. Tübingen, Germany*
Wolfgang Rosenstiel - *Eberhard Karls Univ. Tubingen, Germany*

A Q&A poster session will immediately follow the presentations from 2:30pm to 3:00pm.

51 SEMICONDUCTOR SECURITY: PROTECT THE HARDWARE!

Time: 1:30pm - 3:00pm || Room: 18AB || Event Type: Panel || Track: Security, EDA
Topic Area: General Interest

MODERATOR:
Celia Merzbacher - *Semiconductor Research Corp., Durham, NC*

ORGANIZER:
William Joyner - *Semiconductor Research Corp., Durham, NC*

Though cybersecurity has focused on software vulnerability, recent attacks on "the bare metal" have brought increased attention to protecting the hardware itself: from counterfeiters, from malicious companies/governments, from disgruntled engineers, and from a host of other sources. Research efforts to characterize and address hardware attacks are now beginning to bear fruit.

PANELISTS:
Farinaz Koushanfar - *Univ. of California at San Diego, La Jolla, CA*
Claire Vishik - *Intel Corp., Austin, TX*
Ruby Lee - *Princeton Univ., Princeton, NJ*
Nina Amla - *National Science Foundation, Arlington, VA*
Donna Dodson - *National Institute of Standards and Technology, Gaithersburg, MD*

52 DESIGN AUTOMATION ON THE ROAD TOWARDS AUTOMATED DRIVING

Time: 1:30pm - 3:00pm || Room: 18CD || Event Type: Invited Presentations
Track: Automotive, Embedded Systems || Topic Area: Cyber-Physical Systems, Codesign & System Design

CHAIR:
Dirk Ziegenbein - *Robert Bosch GmbH, Renningen, Germany*

ORGANIZERS:
Michael Huebner - *Ruhr Univ. Bochum, Germany*
Dirk Ziegenbein - *Robert Bosch GmbH, Renningen, Germany*

As driver assistance systems more and more advance towards automated driving capabilities, the computational performance demanded by these applications exceeds by far the demand of previous vehicle control systems. Thus, these systems are increasingly based on heterogeneous parallel hardware solutions, which allow to handle such compute intensive tasks. At the same time, requirements of functional safety and security become also more stringent. The challenge for the Design Automation community is to provide suitable methodologies and tools that support developers in handling this high design complexity. This special session discusses the challenges of developing advanced driver assistance and automated driving systems from the viewpoint of a vehicle manufacturer. Further, a system supplier and a tool provider present current approaches as well as upcoming solutions from system-level modeling to automated software distribution.

52.1 Automotive Electronics and Software Development Challenges for Automated Vehicle Systems (1:30)
Joseph D'Ambrosio - *General Motors Research and Development, Warren, MI*

52.2 A Model-Based Design Approach for an Advanced Driver Assistance System (2:00)
Achim Rettberg, Ina Podolski - *HELLA KGaA Hueck & Co., Lippstadt, Germany*
Jörg Krüger - *INGenX Technologies GmbH, Stade, Germany*
Martin Fernholz - *HELLA KGaA Hueck & Co., Lippstadt, Germany*

52.3 Automated SW Distribution for Automated Driving (2:30)
Maximilian Odendahl - *Silexica Software Solutions GmbH, Aachen, Germany*

53 DESIGN TRACK: HOW TO VERIFY THE GORDIAN'S KNOT OF SYSTEM COMPLEXITY

Time: 1:30pm - 3:00pm || Room: Ballroom E || Event Type: Invited Presentations
Track: Design, EDA || Topic Area: Test & Verification

CHAIR:
Ashish Darbari - *Imagination Technologies Ltd., Kings Langley, United Kingdom*

Gordian's Knot is known to all as the ultimate "intractable problem." Untangling or "cutting the knot" is the search for discovering alternative solutions to just such an unsolvable problem. Verification of system complexity can encompass just such an intractable problems. Creative methods and tools have evolved in response to "cutting the knot." Hear about the cutting-edge formal strategies, security verification strategies and system-testing of IOT in this verification session to help you "cut" your Gordian's Knot of the future.

53.1 Formal Verification: From Flops to Cones to Blocks to Systems (1:30)
Vigyan Singhal - *Oski Technology, Inc., Mountain View, CA*

53.2 Verifying Hardware Security Features to Deliver Secure Systems (2:00)
Mike Bartley - *Test and Verification Solutions, Bristol, United Kingdom*

53.3 System Testing using Transaction-Level Simulation of IoT (2:30)
Jakob Engblom - *Intel Corp., Stockholm, Sweden*

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54 DESIGN TRACK: OPTIMIZING MOBILE USER EXPERIENCE VIA ALL LAYERS OF THE SYSTEM STACK

Time: 1:30pm - 3:00pm || Room: Ballroom F || Event Type: Invited Presentations
Track: Design, IoT || Topic Area: Low-Power & Reliability, Physical Design

CHAIR:
Jian Li - *Huawei Technologies Co., Ltd., Austin, TX*

ORGANIZER:
Harry Chen - *MediaTek, Inc., Hsinchu, Taiwan*

From the smartphones of today to the highly connected and smart IoT world of tomorrow, wireless mobility and energy efficiency have risen to become essential and dominant requirements. To deliver products and services that offer fulfilling user experiences, ever deeper collaboration among ecosystem players is called for. This is occurring while the underlying semiconductor technology continues to advance and evolve in greater complexity from devices to packaging to systems. An open platform of capabilities across the system stack holds the potential to allow creation of optimized solutions in the most cost-effective and flexible manner.We propose a special session of three invited talks by ecosystem players to explore aspects of such a collaborative design environment with focus on energy efficiency.
The players come from different layers of the system stack.

54.1 TSMC solutions for low-power design enablement (1:30)
Guru Prasad - *Taiwan Semiconductor Manufacturing Co., Ltd., Austin, TX*
Charles Liu - *Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan*

54.2 Low-power mobile design realization (2:00)
Chino Lin - *MediaTek, Inc., San Jose, CA*
Eric Fang - *MediaTek, Inc., Hsinchu, Taiwan*

54.3 System Power Modeling: Which Way is Up? (2:30)
Ashley Crawford - *ARM Ltd., Cambridge, United Kingdom*

55 IP TRACK: WHY IP SUBSYSTEMS AND WHY NOW?

Time: 1:30pm - 3:00pm || Room: Ballroom G || Event Type: Embedded Tutorial
Track: IP, IP || Topic Area: General Interest, Business

CHAIR:
Warren Savage - *IPextreme, Campbell, CA*

ORGANIZER:
Richard Wawrzyniak - *Semico Research Corp., Phoenix, AZ*

The session will consider the following aspects of the emerging the IP Subsystem market.

- Drivers and market forces that have combined to prompt the creation of the IP Subsystem concept
- Evolution of the IP Subsystem market
- Benefits of IP Subsystems
- Cons of IP Subsystems
- IP Subsystem Vendor Landscape
- Categories of IP Subsystems
- Examples of IP Subsystems
- Impacts on complex SoC silicon and software design costs and design time
- Solving real world problems with IP Subsystems
- Where does the IP Subsystem concept go from here and how do we get there?

Attendees will walk away with an understanding of the underlying fundamentals driving the Subsystem market with tips on when and when not to use a Subsystem product.

SPEAKERS:
Richard Wawrzyniak - *Semico Research Corp., Phoenix, AZ*
Drew Wingard - *Sonics, Inc., Milpitas, CA*
Marco Brambilla - *Synapse Design, Santa Clara, CA*

56 CRUISING TO CLOSURE WHILE TRUMPING CONSTRAINTS!

Time: 3:30pm - 5:30pm || Room: 12AB || Event Type: Reviewed Presentations || Track: EDA
Topic Area: Physical Design

CHAIR:
Laleh Behjat - *Univ. of Calgary, AB, Canada*

CO-CHAIR:
Wen-Hao Liu - *Cadence Design Systems, Inc., Austin, TX*

From floorplanning to routing, traditional physical design methodologies are being challenged with increasingly complex and diverse constraints brought about by the constant drum of feature scaling. This session focuses on digital and analog design closure in the nanometer regime. The session starts with a new floorplanning representation for analog layout designs, and then moves to timing-driven placement via flip-flop and clock buffer movement. Clock power for high-performance designs is then minimized via flip-flop clustering and placement. This is followed by legalization and detailed placement for advanced nodes handling multi-row height cells and minimum implant area constraints. The session concludes with a layer assignment algorithm for timing optimization.

*** Indicates Best Paper Candidate**

56.1 QB-Trees: Towards An Optimal Topological Representation and Its Applications to Analog Layout Designs (3:30)
I-Peng Wu, Hung-Chih Ou, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

56.2 Timing-Driven Cell Placement Optimization for Early Slack Histogram Compression (3:45)
Chau-Chin Huang, Yen-Chun Liu, Yu-Sheng Lu, Yun-Chih Kuo, Yao-Wen Chang, Sy-Yen Kuo - *National Taiwan Univ., Taipei, Taiwan*

56.3 Flip-flop Clustering by Weighted K-means Algorithm (4:00)
Gang Wu - *Iowa State Univ., Ames, IA*
Yue Xu - *Oracle Corp., Santa Clara, CA*
Dean Wu - *RedMart, Singapore, Singapore*
Manoj Ragupathy, Yu-yen Mo - *Oracle Corp., Santa Clara, CA*
Chris Chu - *Iowa State Univ., Ames, IA*

56.4 Legalization Algorithm for Multiple-Row Height Standard Cell Design (4:15)
Wing-Kai Chow, Chak-Wa Pui, Evangeline F.Y. Young - *Chinese Univ. of Hong Kong, Hong Kong*

56.5 Minimum-Implant-Area-Aware Detailed Placement with Spacing Constraints (4:30)
Kai-Han Tseng, **Yao-Wen Chang** - *National Taiwan Univ., Taipei, Taiwan*
Charles C. C. Liu - *Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan*

56.6 Incremental Layer Assignment for Critical Path Timing (4:45)
Derong Liu - *Univ. of Texas at Austin, TX*
Bei Yu - *Chinese Univ. of Hong Kong, Hong Kong*
Salim Chowdhury - *Oracle Corp., Austin, TX*
David Z. Pan - *Univ. of Texas at Austin, TX*

A Q&A poster session will immediately follow the presentations from 5:00pm to 5:30pm.

57 ATTACKS AND DEFENSES FOR SECURE SYSTEMS - THE ARMS RACE CONTINUES

Time: 3:30pm - 5:30pm || Room: 19AB || Event Type: Reviewed Presentations || Track: Security
Topic Area: Cyber-Physical Systems, Emerging Technologies, Circuit Design

CHAIR:
Jeyavijayan (JV) Rajendran - *Univ. of Texas at Dallas, TX*

CO-CHAIR:
Seetharam Narasimhan - *Intel Corp., Hillsboro, OR*

Globalization of the semiconductor supply chain introduces vulnerabilities in hardware designs such as hardware Trojans, IP piracy, and cloning. Concurrently, there has been a rise in the ingenuity of attackers to exploit them. This session is an assortment of attacks and defenses. The attacks include Trojan-infected power management units, reverse engineering and EM-based fault injection. The defenses range from high-level synthesis for protection against Trojans, automated vulnerability analysis of finite state machines, preventing reverse engineering in STT-CMOS designs, PLL-based countermeasures against fault injection, and remote device attestation.

57.1 Catching the Flu: Emerging threats from a Third Party Power Management Unit (3:30)
Rajesh JayashankaraShridevi, Chidhambaranathan Rajamanikkam, Sanghamitra Roy, Koushik Chakraborty - *Utah State Univ., Logan, UT*

57.2 Information Dispersion for Trojan Defense through High-Level Synthesis (3:45)
S. T. Choden Konigsmark, Deming Chen, Martin D.F. Wong - *Univ. of Illinois at Urbana-Champaign, IL*

57.3 STT-CMOS Hybrid Designs for Reverse-engineering (4:00) Prevention
Theodore Winograd - *George Mason Univ. & Booz Allen Hamilton, Inc., Fairfax, VA*
Hassan Salmani - *Howard Univ., Washington, D.C.*
Hamid M. Mahmoodi - *San Francisco State Univ., San Franscisco, CA*
Kris Gaj, Houman Homayoun - *George Mason Univ., Fairfax, VA*

57.4 AVFSM: A Framework for Identifying and Mitigating Vulnerabilities in FSMs (4:15)
Adib Nahiyan - *Univ. of Florida, Gainesville, FL*
Kan Xiao - *Univ. of Connecticut, Storrs, CT*
Kun Yang - *Univ. of Florida, Gainesville, FL*
Yier Jin - *Univ. of Central Florida, Orlando, FL*
Domenic Forte, Mark Tehranipoor - *Univ. of Florida, Gainesville, FL*

57.5 PLL to the Rescue: A Novel EM Fault Countermeasure (4:30)
Noriyuki Miura - *Kobe Univ., Kobe, Japan*
Zakaria Najm - *Télécom ParisTech, Paris, France*
Wei He - *Nanyang Technological Univ., Singapore, Singapore*
Xuan Thuy Ngo - *Télécom ParisTech, Paris, France*
Shivam Bhasin - *Nanyang Technological Univ., Singapore, Singapore*
Jean-Luc Danger - *Télécom ParisTech, Paris, France*
Makoto Nagata - *Kobe Univ., Kobe, Japan*

57.6 Remote Attestation for Low-End Embedded Devices: the Prover's Perspective (4:45)
Ferdinand Brasser - *Technische Univ. Darmstadt, Germany*
Kasper B. Rasmussen - *Univ. of Oxford, United Kingdom*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*
Gene Tsudik - *Univ. of California, Irvine, CA*

A Q&A poster session will immediately follow the presentations from 5:00pm to 5:30pm.

58 ITCHING FOR INNOVATIVE TECHNOLOGY FOR CPS HARDWARE

Time: 3:30pm - 5:30pm || Room: 17AB || Event Type: Reviewed Presentations || Track: Design, IoT
Topic Area: Codesign & System Design, Cyber-Physical Systems, Emerging Technologies

CHAIR:
Houman Homayoun - *George Mason Univ., Fairfax, VA*

CO-CHAIR:
Fadi Kurdahi - *Univ. of California, Irvine, CA*

This session discusses hardware designs for CPS systems in terms of optimizing the memory hierarchy and compute capabilities. The first three papers investigate adaptations of the memory hierarchy using emerging technologies and controlling the path to memory. The second set of papers aims to improve compute efficiency, targeting mobile computer vision, correcting approximate adders, and approximate bitcoin mining.

*** Indicates Best Paper Candidate**

58.1 Enabling Sub-blocks Erase Management to Boost the Performance of 3D NAND Flash Memory* (3:30)
Tseng-Yi Chen, Yuan-Hao Chang - *Academia Sinica, Taipei, Taiwan*
Chien-Chung Ho - *National Taiwan Univ. & Academia Sinica, Taipei, Taiwan*
Shuo-Han Chen - *National Tsing Hua Univ., Hsinchu, Taiwan*

58.2 BLESS: A Simple and Efficient Scheme for Prolonging PCM Lifetime (3:45)
Marjan Asadinia, Majid Jalili, Hamid Sarbazi-Azad - *Sharif Univ. of Technology, Tehran, Iran*

58.3 A Model-Driven Approach to Warp/Thread-Block Level GPU Cache Bypassing (4:00)
Hongwen Dai - *North Carolina State Univ., Raleigh, NC*
Saurabh Gupta - *Oak Ridge National Laboratory, Oak Ridge, TN*
Chao Li - *North Carolina State Univ., Raleigh, NC*
Christos Kartsaklis - *Oak Ridge National Laboratory, Oak Ridge, TN*
Mike Mantor - *Advanced Micro Devices, Inc., Orlando, FL*
Huiyang Zhou - *North Carolina State Univ., Raleigh, NC*

58.4 A Real-time Energy-Efficient Superpixel Hardware Accelerator for Mobile Computer Vision Applications (4:15)
Injoon Hong - *KAIST, Daejeon, Republic of Korea*
Jason Clemons - *NVIDIA Corp., Austin, TX*
Iuri Frosio, Rangharajan Venkatesan - *NVIDIA Corp., Santa Clara, CA*
Brucek Khailany, Stephen Keckler - *NVIDIA Corp., Austin, TX*

58.5 An Area-Efficient Consolidated Configurable Error Correction for Approximate Hardware Accelerators (4:30)
Sana Mazahir, Osman Hasan - *National Univ. of Sciences and Technology, Islamabad, Pakistan*
Rehan Hafiz - *Information Technology Univ., Lahore, Pakistan*
Muhammad Shafique, Jög Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

58.6 Approximate Bitcoin Mining (4:45)
Matthew T. Vilim, Henry Duwe, Rakesh Kumar - *Univ. of Illinois at Urbana-Champaign, IL*

A Q&A poster session will immediately follow the presentations from 5:00pm to 5:30pm.

59 HOW DO WE MAKE IP REUSE WORK?

Time: 3:30pm - 4:30pm || Room: 18AB || Event Type: Panel || Track: IP
Topic Area: General Interest

MODERATOR:
Brian Fuller - *ARM, Inc., San Jose, CA*

Looking through the crystal ball a decade ago, managers and engineers alike predicted that with the ever-increasing complexity in semiconductor designs, IP would rule the design world. Everyone got sold on the "Plug-n-play" concept of using IPs to create SoCs. From an IP provider's standpoint, design companies rushed to create IPs with high hopes, only to realize that the future was not as rosy as predicted. The Darwinian theory reigned supreme and IP providers fell by the wayside with only a handful of them, emphasizing quality and support, surviving.

At the other end of the spectrum, semiconductor companies have struggled to create and reuse IPs within their own companies. Now, with the growth in analog SoCs, many of the existing providers -- as well as some new ones -- started to create analog IP. However, analog IP design is like black magic: loved by many but known to only a few. Good analog designers are hard to come by, and the need to create test chips for different process technologies, as well as expense, has dented the growth of the analog IP industry. EDA providers have approached IP reuse from a different angle and tried to develop tools that could help IP integration or quality validation. But the challenge has been selling the paradigm shift of using EDA tools to hook up or test IPs as opposed to using their own tools and scripts.

From an IP reuse standpoint, a combination of factors has made reuse an arduous journey. Tight schedules have constrained semiconductor companies from creating as much reusable IP as they would have liked. Keeping track of the various IPs created at the different business units and locations has been equally challenging. In addition, new languages such IP-XACT (IEEE 1685) were developed by a consortium of semiconductor companies, but failed to make major headway among the designer community (although IP providers have started using this as a means for distributing IPs). This panel aims to see whether we oversold IP reuse.

Representatives from the design, provider and semiconductor communities will discuss what ails the IP industry and what can be done to improve IP reuse for analog and digital design. Will emerging technologies such as 3D stacking help? Will an IP management system that lets designers find the right existing IP and track its previous success help?

PANELISTS:
Lisa Minwell - *eSilicon Corp., Austin TX*
Rwik Sengupta - *Samsung Semiconductor, Inc., Austin, TX*
Ranit Adhikary - *ClioSoft, Inc., Fremont, CA*
John Koeter - *Synopsys, Inc., Austin, TX*

60 DESIGN AUTOMATION RESEARCH: FINDING FUNDING FOR THE FUTURE

Time: 4:30pm - 5:30pm || Room: 18AB || Event Type: Panel || Track: EDA, Embedded Systems
Topic Area: General Interest

MODERATOR:
Rob Rutenbar - *Univ. of Illinois at Urbana-Champaign, IL*

ORGANIZER:
Rob Aitken - *ARM, Inc., San Jose, CA*

Various venues at DAC, in ACM forums, and elsewhere have lamented reduced funding for university research in design automation, and have suggested several avenues for the "rebirth" and expansion of this work into new areas.

But what do the funding agencies say about this? Representatives of industry and government will discuss the actual state of support, make suggestions for promising areas of research, and answer questions from the audience about the future in this area.

PANELISTS:
Sankar Basu - *National Science Foundation, Arlington, VA*
William Joyner - *Semiconductor Research Corp., Durham, NC*
Linton Salmon - *Defense Advanced Research Projects Agency, Arlington, VA*
Rich Goldman - *Silicon Catalyst, Silicon Valley, CA*

61 CROSS-LAYER APPROXIMATE COMPUTING: CHALLENGES AND SOLUTIONS

Time: 3:30pm - 5:30pm || Room: 18CD || Event Type: Invited Presentations
Track: Embedded Systems, EDA || Topic Area: Codesign & System Design, Low-Power & Reliability

CHAIRS:
Sybille Hellebrand - *Univ. of Paderborn, Germany*
Umit Ogras - *Arizona State Univ., Tempe, AZ*

ORGANIZERS:
Muhammad Shafique - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

The goal of this special session is on exposing the Approximate Computing challenges across various layers of the hardware-software stacks and enabling cross-layer approximate computing, along with an overview of the early research efforts. This special session highlights the new challenges and opportunities available at multiple abstraction level (i.e. layers between circuits and applications) and motivates the need to bridge this gap through cross-layer design and optimization practices.

The key questions that will be discussed are:
1) Where to apply approximate computing? Computation, communication, and/or data approximations!
2) Interplay of different layers in the hardware and software stacks: More at the application layer where approximations are acceptable, if yes, what kind of programming language and compiler support are required? More at the circuit and architecture layers where a high potential of savings for less effort is available.
3) Will working at one level be inherently limiting?

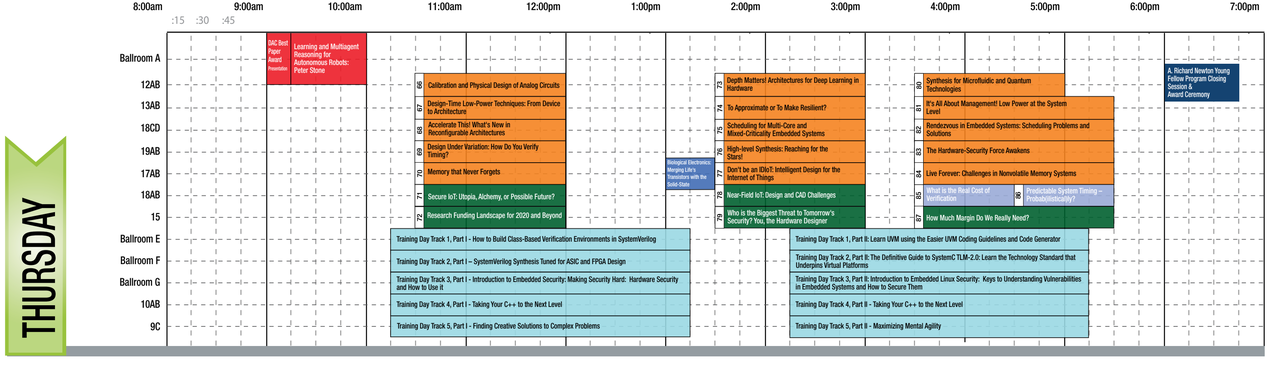
61.1 Cross-Layer Approximations for Neuromorphic Computing: From Devices to Circuits and Systems (3:30)
Priyadarshini Panda, Abhronil Sengupta, Syed Shakib Sarwar, Gopalkrishnan Srinivasan, Swagath Venkataramani, Anand Raghunathan, **Kaushik Roy** - *Purdue Univ., West Lafayette, IN*

61.2 Cross-Layer Approximate Computing: From Logic to Architectures (4:00)
Muhammad Shafique - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Rehan Hafiz - *Information Technology Univ., Lahore, Pakistan*
Semeen Rehman - *Technische Univ. Dresden, Germany*
Walaa El-Harouni , Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

61.3 Approximate Computing with Partially Unreliable Dynamic Random Access Memory: Approximate DRAM (4:30)
Matthias Jung, Deepak M. Mathew, Christian Weis, **Norbert Wehn** - *Univ. of Kaiserslautern, Germany*

61.4 Programming Uncertain Things (5:00)
Todd Mytkowicz - *Microsoft Research, Redmond, WA*

THURSDAY SCHEDULE

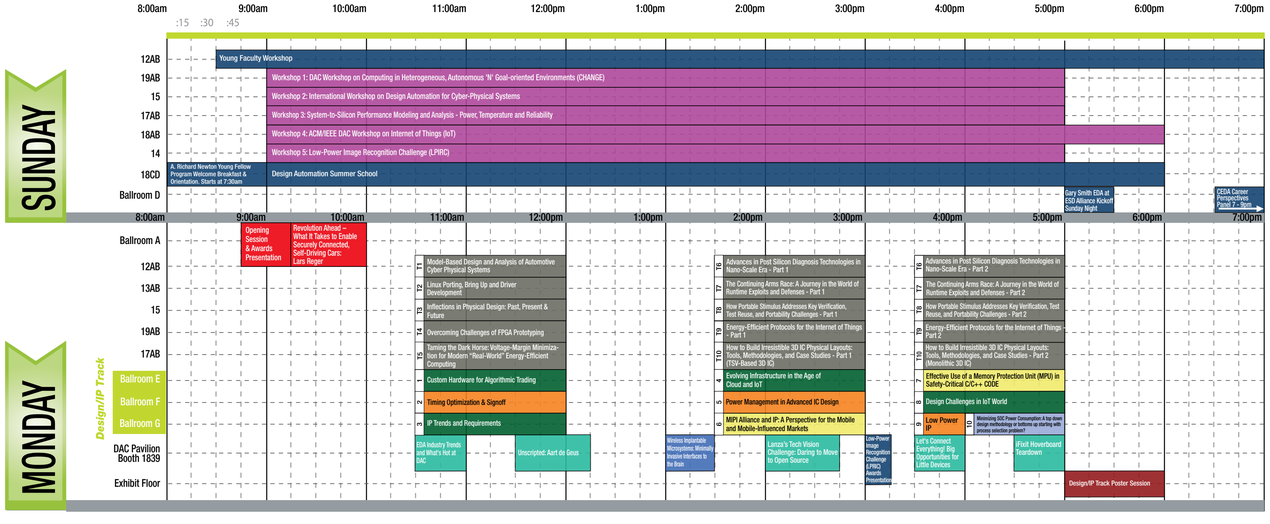


RECEPTION
Thursday, June 9 | 5:30 - 6:30pm | 4th Floor Foyer

EVENT TYPES LEGEND

- Keynotes
- SKY Talks
- Reviewed Presentations
- Invited Presentations
- Panels
- DAC Pavilion
- Monday Tutorials
- Embedded Tutorials
- Workshops
- Thursday is Training Day
- Poster Sessions
- Additional Meetings

SUNDAY/MONDAY SCHEDULE



WELCOME RECEPTION
Sunday, June 5 | 5:30 - 7:00pm | 4th Floor Foyer

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RECEPTION
Monday, June 6 | 6:00 - 7:00pm | Trinity St. Foyer

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DAC SILICON/TECHNOLOGY ART SHOW
Monday, June 6 | 6:00 - 7:00pm | Trinity St. Foyer

EVENT TYPES LEGEND

- Keynotes
- SKY Talks
- Reviewed Presentations
- Invited Presentations
- Panels
- DAC Pavilion
- Monday Tutorials
- Embedded Tutorials
- Workshops
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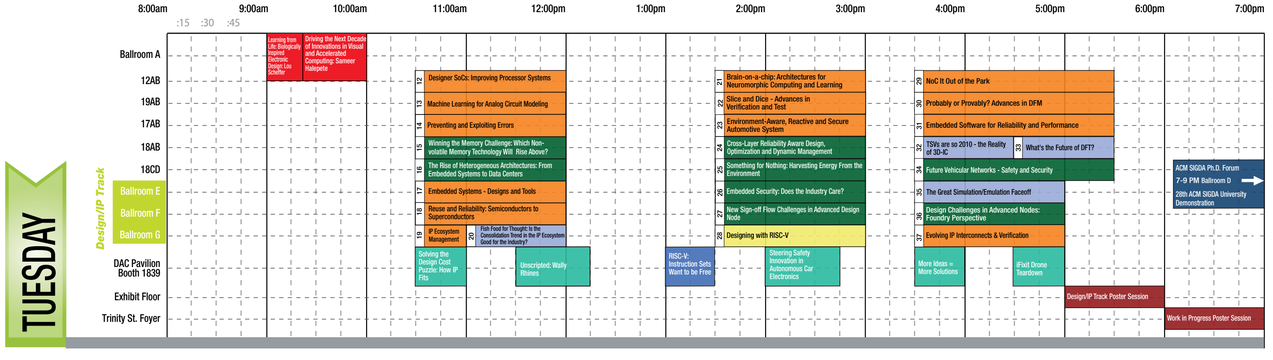
TUESDAY SCHEDULE



RECEPTION
Tuesday, June 7 | 6:00 - 7:00pm | Trinity St. Foyer

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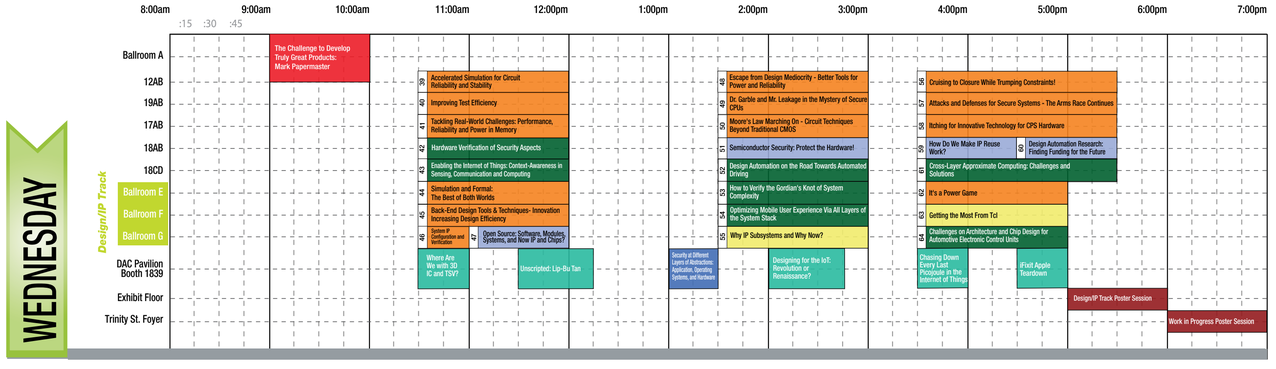
EVENT TYPES LEGEND

- Keynotes
- SKY Talks
- Reviewed Presentations
- Invited Presentations
- Panels
- DAC Pavilion
- Monday Tutorials
- Embedded Tutorials
- Workshops
- Thursday is Training Day
- Poster Sessions
- Additional Meetings

WEDNESDAY SCHEDULE



RECEPTION
Wednesday, June 8 | 6:00 - 7:00pm | Trinity St. Foyer

Thank You to Our Sponsor:

EVENT TYPES LEGEND

- Keynotes
- SKY Talks
- Reviewed Presentations
- Invited Presentations
- Panels
- DAC Pavilion
- Monday Tutorials
- Embedded Tutorials
- Workshops
- Thursday is Training Day
- Poster Sessions
- Additional Meetings

62 DESIGN TRACK: IT'S A POWER GAME

Time: 3:30pm - 5:00pm || Room: Ballroom E || Event Type: Reviewed Presentations
Track: Design, Design || Topic Area: Low-Power & Reliability, System Architectures & SoC, Codesign & System Design

CHAIR:
John Redmond - *Broadcom Corp., San Diego, CA*

Power is the name of the game. Finding every last micro-watt, even nano-watt savings is what matters to chip designers today. Technology of the future is driving chip designs today towards longer lasting devices that can do more with less. Learn about the latest power saving techniques and power verification that will make your device "power"-full!

62.1 Putting On the Dynamic Power Glasses: A FinFET-Aware Approach for Early Realistic Block Activity Analysis and Exploration (3:30)
Ioannis Savvidis, Björn Fjellborg - *Ericsson, Stockholm, Sweden*

62.2 AP Power - Performance Optimization with System Level Thermal/Power Analysis (3:45)
Wook Kim - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Eunju Hwang - *Samsung Electronics Co., Ltd., Hwasung, Republic of Korea*
Joohee Choung - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

62.3 Successive evolution: Tips and tricks for UPF based Low Power verification (4:00)
Deepmala Sachan, Thameem Syed S. - *Intel Corp., Bangalore, India*

62.4 Efficient Techniques for Per Clock Gating Domain Contributor based Power Abstraction of IP Blocks for Hierarchical Power Analysis (4:15)
Arun Joseph - *IBM Systems and Technology Group, Bangalore, India*
Nagu Dhanwada - *IBM Corp., Poughkeepsie, NY*
Spandana Rachamalla - *IBM Corp., Bangalore, India*
William Dungan - *IBM Corp., Poughkeepsie, NY*
Ricardo Nigaglioni - *IBM Systems and Technology Group, Austin, TX*

62.5 Boosting Power Verification by leveraging functional regression (4:30)
Kuo-Kai Hsieh - *Univ. of California, Santa Barbara, CA*
Wen Chen, Monica Farkash - *NXP Semiconductors, Austin, TX*

62.6 Efficient Generation of Power Optimized RTL using Incremental Modification of Design CDFG (4:45)
Manish Kumar - *Mentor Graphics (India) Pvt. Ltd., Noida, India*
Abhishek Bansal, Mamta Asija, Puneet K. Gour - *Mentor Graphics Corp., Noida, India*
Jianfeng Liu - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Abhishek Ranjan - *Mentor Graphics (India) Pvt. Ltd., Noida, India*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*
Kyungtae Do, Mi-Suk Hong - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

Q&A Poster Session
Wednesday, June 8, 5:00 - 6:00pm - Exhibit Floor

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63 DESIGN TRACK: GETTING THE MOST FROM TCL

Time: 3:30pm - 5:00pm || Room: Ballroom F || Event Type: Embedded Tutorial || Track: EDA
Topic Area: General Interest

Tcl has been the language of design-automation since it's inception in the 1980s. Tcl's dominance is due in part to the ease of extending the language by exposing existing C/object code and the availability of Tk for graphics extension. As a language, it has relatively few firm syntax rules and can be described as a nested string processor. That minimal syntax has led many EDA engineers to learn just-enough of the language for the job at hand. That minimized knowledge unfortunately leads users to develop coding patterns that are not robust or even dangerous in large systems. The tutorial will give a firm grounding to EDA users to develop code that works all of the time instead of most of the time. It will discuss Tcl features that make coding in Tcl more productive and will describe patterns to build complex EDA flows and systems in Tcl.

SPEAKERS:
Brian Wilson - *Cadence Design Systems, Inc., Austin, TX*
Mark Brown - *Huawei Technologies Co., Ltd., Dallas, TX*

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64

DESIGN TRACK: CHALLENGES ON ARCHITECTURE AND CHIP DESIGN FOR AUTOMOTIVE ELECTRONIC CONTROL UNITS

Time: 3:30pm - 5:00pm || Room: Ballroom G || Event Type: Invited Presentations
Track: Automotive, Design || Topic Area: System Architectures & SoC

CHAIR:
Michael Huebner - *Ruhr Univ. Bochum, Germany*

ORGANIZERS:
Michael Huebner - *Ruhr Univ. Bochum, Germany*
Dirk Ziegenbein - *Robert Bosch GmbH, Renningen, Germany*

Next generation of electronic control units (ECU) in cars need a next generation of silicon devices for analog, digital as well for mixed signal functionality. The increasing complexity of ECUs leads e.g. to a shift towards multicore processors which are able to handle the high computational requirements of advanced driver assistant systems. Also a higher integration of systems into System-on-Chip (SoC) devices, where analog as well as digital interfaces, partly with a very high throughput for camera based system are on one silicon die, requires high end EDA tools in a broad range. This means tools for system level design, mixed signal chip design, formal verification and finally testing needs to be selected. In this special session the silicon providers as well as developers present recent techniques for next generation automotive chip design. The special session is addressed to hardware and system engineers as well as to researchers.

64.1 Fast and Furious: Keeping Pace with the Trends in Automotive Architecture (3:30)
Jason Jones - *Texas Instruments, Inc., Houston, TX*

64.2 New ADAS Silicon Architectures Drive a Quantum Leap in Platform Efficiency, Intelligence and Flexibility (4:00)
Chris Rowen - *Cadence Design Systems, Inc., San Jose, CA*

64.3 SoC Architectures for Automotive and Functional Safety (4:30)
Balatripura Chavali - *Intel Corp., Austin, TX*

Thank You to Our Sponsor: Mentor Graphics

DESIGN/IP TRACK POSTER SESSION

Time: 5:00pm - 6:00pm || Room: Exhibit Floor || Event Type: Poster Session || Track: Design, IP
Topic Area: General Interest

During the poster presentation, you will interact directly with poster presenters in a small group setting.

As the limited time available in the Design/IP Track session program was exceeded by the quantity of great submitted content, we present the following posters in the Design/IP Track Poster Session held Wednesday, June 8 from 5:00 to 6:00pm on the Exhibit Floor.

Thank You to Our Sponsors:

Mentor Graphics ChipEstimate.com

65.1 Expediting standard cell development using on-the-fly DRC
Atul Bhargava, Shayamli Choudhary - *STMicroelectronics, Greater Noida, India*
Srinivas Velivala - *Mentor Graphics Corp., Wilsonville, OR*

65.2 FX-14 Design Methodology Implementation
Michael D. Amundson - *GLOBALFOUNDRIES, Oronoco, MN*

65.3 Reduction of supply noise and timing Jitter with Power delivery network optimization in DDR3 based system
Pratik Damle, Rakesh K. Malik, Shiv Om Sharma - *STMicroelectronics, Greater Noida, India*
Abhishek Nigam - *STMicroelectronics & HCL Technologies, Greater Noida, India*
Akhilesh Chandra Mishra - *STMicroelectronics, Greater Noida, India*

65.4 Chip IR-drop optimism using lumped or pin grouped package models
Marc DeWilde - *Texas Instruments, Inc., Plano, TX*
Jeff Linn - *Apache Design, Inc., A Subsidiary of ANSYS, Inc., Austin, TX*

65.5 Perforance Optimization without Area and Power Penalties in Auto P&R Flow
Wootae Kim - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Hyung-Ock Kim, Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*

65.7 A Methodology to Design Early and Efficient Power-Distribution-Network for Power-Gated Designs
Abhishek Mittal - *Broadcom Corp., Banagalore, India*
Anusha Gummana, Dileesh Jostin - *ANSYS, Inc., Bangalore, India*

65.9 FinFET Episode II Unveil: Is 16-to-10nm the revolution or evolution?
Andy Chao, **Shawn S. Hung** - *ARM Ltd., Hsinchu City, Taiwan*

65.10 Power Grid Sign-Off with timing Perspective and per instance timing derating feedback to ease STA signoff
John Fellbaum - *Hewlett-Packard Co., Houston, TX*
Kaushal Kishore - *ANSYS, Inc., Austin, TX*

DESIGN/IP TRACK POSTER SESSION

65.11 An Effectual Approach of Timing Constraints Promotion and Demotion
Prakul Bhagat, Akhilesh Chandra, Venus Kothari, Renuka Deshpande, Ankur Kaushik, Himanshu Bhatnagar, **Aditi Sharma** - *STMicroelectronics, Greater Noida, India*

65.12 Area-efficient built-in memory self-repair architecture for heterogeneous cores with embedded BIST datapath
Devanathan VR, **Sumant Kale**, Eric Von Dohlen - *Texas Instruments, Inc., Dallas, TX*

65.14 Enhancements in Full-Custom Flow to Mitigate Post-Layout Challenges in Advanced Technology Nodes
Radhika Gupta, Atul Bhargava - *STMicroelectronics, Greater Noida, India*
Francois Lemery - *STMicroelectronics, Crolles, France*
Rakesh Shenoy - *Synopsys India Pvt. Ltd., Noida, India*

65.15 How Substrate Noise Analysis Root Causing Chip Failure due to Coupling Effect
Kwangseok Choi - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Youngsoo Lee - *ANSYS, Inc., Santa Clara, CA*
Byunghyun Lee - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

65.16 RESTful API for Microprocessor Timing Data
Jose A. Paredes, **Trevor H. Green** - *IBM Corp., Austin, TX*

65.17 Early and Sign-off Stage Analysis of Power and Thermal Integrity of Large Vertically Stacked 3D-IC
Koichi Yoshimi, Hironori Kawaminami - *Fujitsu VLSI Ltd., Tokyo, Japan*
Norman Chang - *ANSYS, Inc., San Jose, CA*

65.18 Chip Area Optimization Using Polygonal Standard Cell
JinTae Kim - *Samsung Electronics Co., Ltd. & Samsung Semiconductor, Inc., Hwaseong-Si, Republic of Korea*
Jaewan Choi, Sangwoo Han - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Tae Joong Song - *Samsung Electronics Co., Ltd., Seongnam-Si, Republic of Korea*
Sungwee Cho - *Samsung Electronics Co., Ltd., Hwaseong-Si, Republic of Korea*

65.19 Early and Efficient Approach to Model Power & IR analysis for Multimillion SOC using RTL VCD
Vaishali V. Huilgol, Shashank Bhonge, Jayanth Bandaru - *Xilinx Inc., Hyderabad, India*

65.20 Enabling Efficient Design Planning
Meng-Fan Wu, Chih-Tsung Yao, Koan Huang - *MediaTek, Inc., Hsinchu, Taiwan*
Chino Lin - *MediaTek, Inc., San Jose, CA*

65.22 Multi-Voltage Domain Timing Methodology for Microprocessor Designs
Eric Foreman - *IBM Systems and Technology Group, Essex Jct., VT*
Nathan Buck - *IBM Corp., Underhill, VT*
Stephen Shuma - *IBM Corp., Essex Jct., VT*
Jeffrey G. Hemmett - *IBM Systems and Technology Group, Essex Junction, VT*
Debjit Sinha - *IBM Corp., Poughkeepsie, NY*

65.29 DFx testing on emulation
Aviv Barkai, Noy Nakash - *Intel Corp., Haifa, Israel*

65.30 Performance Estimation and System Analysis in systems with ARM Cores
Robert Kaye - *ARM Ltd., Cambridge, United Kingdom*
Jason Andrews - *ARM, Inc., Ham Lake, MN*

65.31 Requirements driven Verification
Michael Bartley - *Test and Verification Solutions, Bristol, United Kingdom*

65.32 Advanced on-chip data protection for automotive functional safety and storage reliability
Kurt Shuler, **Dee Lin** - *Arteris, Inc., Campbell, CA*

65.45 Hierarchical IP Design in SoCs
William E. Orme - *ARM Ltd., Cambridge, United Kingdom*
David Murray - *ARM Ltd. & ARM, Inc., Galway, Ireland*

65.46 Verilog modelling of transistor and R,L,C components for very fast digital simulations of mixed signal IPs
Santosh Nene, Babu Ramki S., Shovan Maity - *Intel Corp., Bangalore, India*

WORK-IN-PROGRESS POSTER SESSION

Time: 6:00pm - 7:00pm || Room: Trinity St. Foyer || Event Type: Poster Session || Track: EDA
Topic Area: General Interest

The DAC Work-in-Progress (WIP) poster session aims to provide authors an opportunity to network with peer feedback on current work and preliminary results. Join the presenters in the Foyer for their presentations.

101.1 KVFTL: Optimization of Storage Space Utilization for Key-Value-Specific Flash Storage Devices
Yen-Ting Chen - *National Tsing Hua Univ., New Taipei, Taiwan*
Ming-Chang Yang - *Academia Sinica and National Taiwan Univ., Taipei, Taiwan*
Yuan-Hao Chang - *Academia Sinica, Taipei, Taiwan*
Tseng-Yi Chen - *Academia Sinica, New Taipei, Taiwan*
Hsin-Wen Wei - *Tamkang Univ., Taipei, Taiwan*
Wei-Kuan Shih - *National Tsing Hua Univ., Hsinchu, Taiwan*

101.2 An Incremental Timing-Driven Placement Flow Considering Routability
Jucemar L. Monteiro - *Univ. Federal do Rio Grande do Sul & Univ. of Calgary, Porto Algre, Brazil*
Nima Karimpour Darav - *Univ. of Calgary, AB, Canada*
Guilherme Flach, Mateus Fogaça, Ricardo Reis - *Univ. Federal do Rio Grande do Sul, Porto Algre, Brazil*
Andrew Kennings - *Univ. of Waterloo, ON, Canada*
Marcelo Johann - *Univ. Federal do Rio Grande do Sul, Porto Algre, Brazil*
Laleh Behjat - *Univ. of Calgary, AB, Canada*

101.3 System Verilog Assertions Synthesis Based Compiler
Khaled Salah - *Mentor Graphics Corp., Cairo, Egypt*
Ahmed Y. Fouad, Omar Ibrahem, Omar Amin, Youssef Ramzy - *Alexandria Univ., Alexandria, Egypt*
Mohamed AbdelSalam - *Mentor Graphics Corp., Cairo, Egypt*

101.4 End of the Life Guard-band for SRAM memories : Reliability analysis and characterization of Memory products for Aging tolerant System-On-Chip timing closure
Akash B S, Abhairaj Singh, Anand Shukla, Piyush Jain, Shruti Aggarwal - *ARM Ltd., Noida, India*

101.5 An Optimized, Dynamic and Generic UVM Architecture for Flash Memory Controllers
Sameh El-Ashry - *Ain Shams Univ., Alexandria, Egypt*
Ahmed El-Yamany - *Alexandria Univ., Alexandria, Egypt*
Khaled Salah - *Mentor Graphics Corp., Cairo, Egypt*

101.6 Correlation Power Analysis Attack on PIC Based AES-128 Implementation without Triggering Signal: Leveraging Elastic Alignment
Oluwadara Adegbite, Syed Rafay Hasan - *Tennessee Technological Univ., Cookeville, TN*

101.7 Analysis and Verification of Hard Tie-off Signals in SoC
Prokash Ghosh - *NXP Semiconductors, Noida, India*

101.8 Automatic Assertions to Coverage Conversion Using A Novel Tool
Sameh El-Ashry - *Ain Shams Univ., Alexandria, Egypt*
Hatem El-Kharashy, Abdel-Rahman Gaber, Ahmed El-Yamany - *Alexandria Univ., Alexandria, Egypt*
Khaled Salah - *Mentor Graphics Corp., Cairo, Egypt*

101.9 CircuitsByCode: Programmable Schematics to Simplify PCB Design
Shengye Wang, Chris Taylor, Devon Merrill, Steven Swanson - *Univ. of California at San Diego, La Jolla, CA*

101.10 Towards Tighter Bounds for Coupling-Aware Timing Analysis
Jack S.-Y. Lin, Ryan H.-M. Huang, **Louis Y.-Z. Lin**, Charles H.-P. Wen - *National Chiao Tung Univ., Hsinchu, Taiwan*

101.11 Associative Memory with Online Learning for Approximate Computing
Mohsen Imani, Yeseong Kim - *Univ. of California at San Diego, La Jolla, CA*
Abbas Rahimi - *Univ. of California, Berkeley, CA*
Tajana S. Rosing - *Univ. of California at San Diego, La Jolla, CA*

101.12 Parametric Exploration for Energy Management Strategy Choice in 28nm UTBB FDSOI Technology
Jorge Rodas, **Diego Puschini** - *CEA-LETI Minatec, Grenoble, France*
Suzanne Lesecq - *CEA-LETI Minatec & Univ. Grenoble Alpes, Grenoble, France*

101.13 MaxPB : Accelerating PCM write by maximizing the power budget utilization
Zheng Li - *Huazhong Univ. of Science & Technology & Wuhan National Laboratory for Optoelectronics, Wuhan, China*
Fang Wang, Dan Feng, Yu Hua, Jingning Liu, Wei Tong - *Huazhong Univ. of Science & Technology, Wuhan, China*

101.14 Dynamic Power Optimization based on Formal Property Checking of Operations
Shrinidhi Udupi - *Technische Univ. Kaiserslautern, Germany*
Joakim Urdahl, Dominik Stoffel, Wolfgang Kunz - *Univ. of Kaiserslautern, Germany*

101.15 A Secure Network Architecture for the Internet of Things Based on Local Authorization Entities
Hokeun Kim, Armin Wasicek, Benjamin Mehne, Edward Lee - *Univ. of California, Berkeley, CA*

101.16 Exploiting bipartite graph matching for fast local clock network optimization during incremental timing-driven placement
Renan Netto, Vinicius S. Livramento, Chrystian S. Guth, Luiz C. V. dos Santos, **José Luís A. Güntzel** - *Federal Univ.of Santa Catarina, Brazil*

101.17 High-Performance Stream Cipher Using Physically Unclonable Functions for Big Data Security
Geng Zheng, **Yongqiang Lyu**, Qian Fang, Dongsheng Wang - *Tsinghua Univ., Beijing, China*
Gang Qu - *Univ. of Maryland, College Park, MD*

101.18 Security of Neuromorphic Computing: Thwarting Learning Attacks Using Memristor's Obsolescence Effect
Chaofei Yang, Beiye Liu - *Univ. of Pittsburgh, PA*
Wujie Wen - *Florida International Univ., Miami, FL*
Mark Barnell, Qing Wu - *Air Force Research Lab, Rome, NY*
Hai Li, **Yiran Chen** - *Univ. of Pittsburgh, PA*
Jeyavijayan Rajendran - *Univ. of Texas at Dallas, TX*

101.19 Novel Spiking Temporal Encoder for Brain-inspired Computing Systems
Chenyuan Zhao, Yang Yi - *Univ. of Kansas, Lawrence, KS*

WORK-IN-PROGRESS POSTER SESSION

101.20 A Novel Energy Harvesting Methodology using STTRAM
Rekha Govindaraj, Jae-Won Jang, Swaroop Ghosh, Nitin Rathi - *Univ. of South Florida, Tampa, FL*
Srikant Srinivasan - *Iowa State Univ., Ames, IA*

101.21 Optimizing Energy Efficiency with Multi-Mode Block inLast-Level Cache
Gregory K. Lee, Yuho Jin - *New Mexico State Univ., Las Cruces, NM*

101.22 Energy Optimization on MPSoC with Convex Framework
Erwan Nogues, Maxime Pelcat, **Daniel Menard** - *Institut National des Sciences Appliquées de Rennes, France*

101.23 An Accurate and Efficient Method to Calculate the Error Statistics of Carry Speculative Approximate Adders
You Li, Xiangxuan Ge, **Weikang Qian** - *Shanghai Jiao Tong Univ., Shanghai, China*

101.24 Towards Formal Autopilot Control Under Perception Uncertainty
Susmit Jha - *United Technologies Research Center, Emeryville, CA*
Vasumathi Raman - *United Technologies Research Center, Berkeley, CA*

101.25 Power Efficient Hierarchical SEC-DAEC-DEC code for Reliable Memory
Yonghae Kim - *Sungkyunkwan Univ., Gyeonggi-do, Republic of Korea*
Joon-Sung Yang - *Sungkyunkwan Univ., Suwon, Republic of Korea*

101.26 Towards a practical specification of quantum circuits
Alexandru Paler - *Univ. Transilvania, Brasov, Romania*
Simon J. Devitt - *RIKEN Center for Emergent Matter Science, Saitama, Japan*

101.27 Hardware Trojans Detection based on Steady State Learning
Kento Hasegawa - *Waseda Univ., Shinjuku, Japan*
Masao Yanagisawa, Nozomu Togawa, **Masaru Oya** - *Waseda Univ., Tokyo, Japan*

101.28 COPAL: Connectivity Preserving Algorithm for Network-On-Chip Power-Gating
Pengju Ren - *Xi'an Jiaotong Univ., Xi'an, China*
Michel A. Kinsy - *Univ. of Oregon, Eugene, OR*
Chenxi Yang - *Xi'an Jiaotong Univ., Xi'an, China*
Sena A. Koehnen, Shreeya Khadka, Brian J. Gravelle - *Univ. of Oregon, Eugene, OR*
Nanning Zheng - *Xi'an Jiaotong Univ., Xi'an, China*

101.29 A Novel ECO Algorithm For Sequential Clock Gating based Low Power Design Flow
Mahima Jain -*Mentor Graphics Corp., Mentor Graphics (India) Pvt. Ltd. Noida, India*
Mohit Kumar, Nikhil Tripathi, Abhishek Ranjan, Amit Jain, Saumik Sarkar - *Mentor Graphics Corp., Noida, India*
Jianfeng Liu, Mi-Suk Hong, Kyungtae Do - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*
SungHo Park - *Samsung Electronics Co., Ltd., Hwasong-Si, Republic of Korea*

101.30 Data integrity of STTRAM-Vulnerabilities, Attack Models and Prevention
Jae-Won Jang, Swaroop Ghosh - *Univ. of South Florida, Tampa, FL*

101.31 SAT-Based Time Borrowing against Aging-Induced Timing Errors
Jhao-Yang Huang, Chang-Lin Tsai, **Kai-Chiang Wu** - *National Chiao Tung Univ., Hsinchu, Taiwan*

101.32 Simultaneous Discrete Finite Automata for Wildcard Pattern Matching by Separated nvTCAM Search Engines
Hsiang-Jen Tsai, Chien-Chih Chen, Keng-Hao Yang - *National Chiao Tung Univ., Hsinchu, Taiwan*
Tay-Jyi Lin - *National Chung Cheng Univ., Chiayi, Taiwan*
Yen-Ning Chiang, Wei-Cheng Zhao, Meng-Fan Chang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Tien-Fu Chen - *National Chiao Tung Univ., Hsinchu, Taiwan*

101.33 Challenging On-Chip SRAM Security with Boot-State Statistics
Joseph E. McMahan, Weilong Cui, Liang Xia - *Univ. of California, Santa Barbara, CA*
Jeff Heckey - *Avago Technologies, Colorado Springs, CO*
Fred Chong - *Univ. of Chicago, IL*
Timothy Sherwood - *Univ. of California, Santa Barbara, CA*

101.34 Built-In Self-Test/Repair Methodology for Multi-Band RF-Interconnected TSV 3D Integrations
Shu-Feng Cheng, Po-Tsang Huang, Li-Chun Wang - *National Chiao Tung Univ., Hsinchu, Taiwan*
Mau-Chung F. Chang - *Univ. of California, Los Angeles, CA*

101.35 Post-Silicon Validation Methodology for the Address Translation Mechanisms of Modern Microprocessors
George Papadimitriou, Athanasios Chatzidimitriou, Dimitris Gizopoulos - *Univ. of Athens, Greece*
Ronny Morad - *IBM Research - Haifa, Israel*

101.36 Directly Coupled S-NDR Oscillator Networks for Image Segmentation
Yunus E. Kesim, Abhishek Anil Sharma, James A. Bain, Jeffrey A. Weldon - *Carnegie Mellon Univ., Pittsburgh, PA*

101.37 A Low-Power Design for Brain-Inspired Hyperdimensional Computing
Abbas Rahimi, Pentti Kanerva, Jan M. Rabaey - *Univ. of California, Berkeley, CA*

101.38 STOCK: Stochastic Checkers for Faults in Approximate Applications
Neel T. Gala - *Indian Institute of Technology Madras, Chennai, India*
Swagath Venkataramani, Anand Raghunathan - *Purdue Univ., West Lafayette, IN*
Veezhinathan Kamakoti - *Indian Institute of Technology Madras, Chennai, India*

101.39 HW/SW Embedded System for Accelerating Diagnosis of Glaucoma From Eye Fundus Images
Paulo Cezar Dantas Junior - *Univ. Federal de Pernambuco, Recife, Brazil*
Andrea Sarmento - *Clinica Oftalmologica Zona Sul, Recife, Brazil*
Adriano Sarmento - *Univ. Federal de Pernambuco, Recife, Brazil*

101.40 Co-Optimization of TAM Bus Wires Routing and Test Scheduling for Core-Based SoC Designs
Jui-Hung Hung, Chun-Hua Cheng, **Shih-Hsu Huang**, Wei-Kai Cheng - *Chung Yuan Christian Univ., Taoyuan City, Taiwan*

101.41 An algorithm to identify cornerstones of digital circuits
Yanxiang Huang, Chunshu Li - *IMEC & Katholieke Univ. Leuven, Heverlee, Belgium*
Meng Li - *IMEC, Heverlee, Belgium*
Francky Catthoor - *IMEC & Katholieke Univ. Leuven, Leuven, Belgium*
Liesbet Van der Perre, Wim Dehaene - *Katholieke Univ. Leuven, Belgium*

101.42 Improving Performance and Energy Efficiency of STT-MRAM-Based Handheld Platforms Under Read Disturbance
Hao Yan - *Univ. of Texas at San Antonio, TX*
Lei Jiang - *Advanced Micro Devices, Inc., Austin, TX*
Lide Duan - *Univ. of Texas at San Antonio, TX*

WORK-IN-PROGRESS POSTER SESSION

101.43 CNFET-Based High Throughput Register File Architecture
Li Jiang, Tianjian Li, Naifeng Jing - *Shanghai Jiao Tong Univ., Shanghai, China*
Nam Sung Kim - *Univ. of Illinois at Urbana-Champaign, IL*
Xiaoyao Liang, Tianjian Li - *Shanghai Jiao Tong Univ., Shanghai, China*

101.44 A New Datapath Bit Slicing Algorithm for Modern Circuit Placement
Chau-Chin Huang, Hsin-Ying Lee, Bo-Qiao Lin, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*
Jun-Zhi Yang, Kuo-Sheng Wu - *MediaTek, Inc., Hsinchu, Taiwan*

101.45 Reliable Many-Core System-on-Chip Design using K-Node Fault Tolerant Graphs
Zheng Wang - *Nanyang Technological Univ., Singapore, Singapore*
Alessandro Littarru - *Univ. of Cagliari & RWTH Aachen Univ., Italy*
Emmanuel I. Ugwu - *Aachen Univ. of Technology, Aachen, Germany*
Shazia Kanwal - *Sirindhorn International Thai-German Graduate School of Engineering, Bangkok, Thailand*
Anupam Chattopadhyay - *Nanyang Technological Univ., Singapore, Singapore*

101.46 Encasing Block Ciphers to Foil Key Recovery Attempts via Side Channel
Giovanni Agosta, **Alessandro Barenghi**, Michele Scandale, Gerardo Pelosi - *Politecnico di Milano, Italy*

101.47 A Data-Driven Compressive Sensing Framework for Long-Term Health Monitoring
Kai Xu, Yixing Li - *Arizona State Univ., Tempe, AZ*
Yuhao Wang - *Nanyang Technological Univ., Singapore, Singapore*
Fengbo Ren - *Arizona State Univ., Tempe, AZ*

101.48 System-Level Energy Optimization For Dark Silicon Manycore Microprocessor Considering both Hard and Soft Errors
Taeyoung Kim, Xin Huang - *Univ. of California, Riverside, CA*
Hai-Bao Chen - *Shanghai Jiao Tong Univ., Shanghai, China*
Zeyu Sun, Nazmus Saquib - *Univ. of California, Riverside, CA*
Valeriy Sukharev - *Mentor Graphics Corp., Fremont, CA*
Sheldon X.-D. Tan - *Univ. of California, Riverside, CA*

101.49 INsight: A Neuromorphic Computing System for Evaluation of Deep Neural Networks
Jaeyong Chung, Taehwan Shin, Yongshin Kang - *Incheon National Univ., Incheon, Republic of Korea*

101.50 Model Free Adaptive Data Prefetching using Hypothesis Tests
Lionel Vincent - *PERSYVAL-lab & Univ. Grenoble Alpes, France*
Stéphane Mancini - *TIMA Lab, CNRS/Grenoble INP/UJF, Grenoble, France*
Suzanne Lesecq - *CEA-LETI Minatec & Univ. Grenoble Alpes, Grenoble, France*
Henri-Pierre Charles - *CEA-LIST & Univ. Grenoble Alpes, Grenoble, France*

101.51 Bard: A Unified Framework for Managing Soft Timing and Power Constraints
Connor Imes, Henry C. Hoffmann - *Univ. of Chicago, IL*

101.52 Energy-Aware Multi-Variant Networked Wearable System Design: A Derivative-Free Optimization
Ramin Fallahzadeh, Ramyar Saeedi, Hassan Ghasemzadeh - *Washington State Univ., Pullman, WA*

101.53 On the Analysis of the Confidence on WCET Estimates for Software Randomization Caches
Pedro Benedicte, Leonidas Kosmidis - *Barcelona Supercomputing Center & Univ. Politècnica de Catalunya, Barcelona, Spain*
Eduardo Quinones, Jaume Abella, Francisco J. Cazorla - *Barcelona Supercomputing Center, Barcelona, Spain*

101.54 Selective Abstraction and Stochastic Methods for Scalable Power Modelling of Heterogeneous Systems
Ashur Rafiev, **Fei Xia**, Alexei Iliasov, Rem Gensh, Ali Aalsaud, Alexander Romanovsky, Alex Yakovlev - *Newcastle Univ., Newcastle upon Tyne, United Kingdom*

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THURSDAY, JUNE 9

DAC BEST PAPER AWARD PRESENTATION

Time: 9:00am - 9:10am || Room: Ballroom A

DAC will present the research Best Paper Award as well as the Design/IP Track Best Presentation Awards.

KEYNOTE: LEARNING AND MULTIAGENT REASONING FOR AUTONOMOUS ROBOTS

Peter Stone - *Univ. of Texas at Austin, TX*

Time: 9:10am - 10:00am || Room: Ballroom A || Track: IoT, Embedded Systems
Topic Area: Cyber-Physical Systems, General Interest

Over the past half-century, we have transitioned from a world with just a handful of mainframe computers owned by large corporations, to a world in which private individuals have multiple computers in their homes, in their cars, in their pockets, and even on their bodies. This transition was enabled by computer science research in multiple areas such as systems, networking, programming languages, human computer interaction, and artificial intelligence.

We are now in the midst of a similar transition in the area of robotics. Today, most robots are still found in controlled, industrial settings. However, robots are starting to emerge in the consumer market, and we are rapidly transitioning towards a time when private individuals will have useful robots in their homes, cars, and workplaces. For robots to operate robustly in such dynamic, uncertain environments, we are still in need of multidisciplinary research advances in many areas such as computer vision, tactile sensing, compliant motion, manipulation, locomotion, high-level decision-making, and many others.

This talk will focus on two essential capabilities for robust autonomous intelligent robots, namely online learning from experience, and the ability to interact with other robots and with people. Examples of theoretically grounded research in these areas will be highlighted, as well as concrete applications in domains including robot soccer and autonomous driving!

Biography: Dr. Peter Stone is the David Bruton, Jr. Centennial Professor of Computer Science at the University of Texas at Austin. In 2013 he was awarded the University of Texas System Regents' Outstanding Teaching Award and in 2014 he was inducted into the UT Austin Academy of Distinguished Teachers, earning him the title of University Distinguished Teaching Professor. Professor Stone's research interests in Artificial Intelligence include machine learning (especially reinforcement learning), multiagent systems, robotics, and e-commerce. Professor Stone received his Ph.D in Computer Science in 1998 from Carnegie Mellon University. From 1999 to 2002 he was a Senior Technical Staff Member in the Artificial Intelligence Principles Research Department at AT&T Labs - Research. He is an Alfred P. Sloan Research Fellow, Guggenheim Fellow, AAAI Fellow, Fulbright Scholar, and 2004 ONR Young Investigator. In 2003, he won an NSF CAREER award for his proposed long term research on learning agents in dynamic, collaborative, and adversarial multiagent environments, and in 2007 he received the prestigious IJCAI Computers and Thought Award, given biannually to the top AI researcher under the age of 35.

66 CALIBRATION AND PHYSICAL DESIGN OF ANALOG CIRCUITS

Time: 10:30am - 12:00pm || Room: 12AB || Event Type: Reviewed Presentations
Track: EDA, Design || Topic Area: Physical Design, Circuit Design, Lithography & DFM

CHAIR:
Peter Feldmann - *D. E. Shaw Research, New York, NY*

CO-CHAIR:
Jaeha Kim - *Seoul National Univ., Seoul, Republic of Korea*

Device mismatch and process variations are critical issues in analog and RF design. This session begins with novel results in automated layout generation and capacitor placement, followed by the design of SAR ADC with self-learning techniques, and concludes with a statistical selection method for design calibration.

66.1 Novel CMOS RFIC Layout Generation with Concurrent Device Placement and Fixed-Length Microstrip Routing (10:30)
Tsun-Ming Tseng, Bing Li - *Technische Univ. München, Germany*
Ching-Feng Yeh, Hsiang-Chieh Jhan, Zuo-Min Tsai, Mark Po-Hung Lin - *National Chung Cheng Univ., Chiayi, Taiwan*
Ulf Schlichtmann - *Technische Univ. München, Germany*

66.2 Procedural Capacitor Placement in Differential Charge-Scaling Converters by Nonlinearity Analysis (10:45)
Florin Burcea, Husni Habal, Helmut Graeb - *Technische Univ. München, Germany*

66.3 A Novel Time and Voltage Based SAR ADC Design with Self-Learning Technique (11:00)
Abhilash Karnatakam Nagabhushana, Haibo Wang - *Southern Illinois Univ. Carbondale, IL*

66.4 Extended Statistical Element Selection: A Calibration Method for High Resolution in Analog/RF Designs (11:15)
Renzhi Liu - *Carnegie Mellon Univ. & Intel Corp, Pittsburgh, PA*
Jeffrey A. Weldon, Larry Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

A Q&A poster session will immediately follow the presentations from 11:30am to 12:00pm.

67 DESIGN-TIME LOW-POWER TECHNIQUES: FROM DEVICE TO ARCHITECTURE

Time: 10:30am - 12:00pm || Room: 13AB || Event Type: Reviewed Presentations
Track: EDA, Design || Topic Area: Low-Power & Reliability, Circuit Design, System Architectures & SoC

CHAIR:
Martin Lukasiewycz - *Bosch Research, Munich, Germany*

CO-CHAIR:
Phillip Stanley-Marbell - *Massachusetts Institute of Technology, Cambridge, MA*

Improving energy efficiency requires considerations across different layers, from device to circuit and architecture. The first two papers in this session describe a low-power divider and a JPEG encoder under the approximate computing paradigm. The third paper presents a joint architecture/circuit optimization for FinFET-based SRAM. Last, a new circuit design technique, asynchronous race, is introduced to greatly improve the power efficiency of dynamic programming computation.

67.1 A Low-Power Dynamic Divider for Approximate Applications (10:30)
Soheil Hashemi, R. Iris Bahar, Sherief Reda - *Brown Univ., Providence, RI*

67.2 Optimal Design of JPEG Hardware under the Approximate Computing Paradigm (10:45)
Farhana Sharmin Snigdha, Deepashree Sengupta - *Univ. of Minnesota, Twin Cities, Minneapolis, MN*
Jiang Hu - *Texas A&M Univ., College Station, TX*
Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

67.3 Minimizing the Energy-Delay Product of SRAM Arrays using a Device-Circuit-Architecture Co-Optimization Framework (11:00)
Alireza Shafaei, Hassan Afzali-Kusha, Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

67.4 Energy Efficient Computation with Asynchronous Races (11:15)
Advait Madhavan, Timothy Sherwood, Dmitri Strukov - *Univ. of California, Santa Barbara, CA*

A Q&A poster session will immediately follow the presentations from 11:30am to 12:00pm.

68 ACCELERATE THIS! WHAT'S NEW IN RECONFIGURABLE ARCHITECTURES

Time: 10:30am - 12:00pm || Room: 18CD || Event Type: Reviewed Presentations
Track: EDA || Topic Area: System Architectures & SoC

CHAIR:
Mohit Tiwari - *Univ. of Texas at Austin, TX*

CO-CHAIR:
Chia-Lin Yang - *National Taiwan Univ., Taipei, Taiwan*

Reconfigurable architectures are emerging to address the performance, power and reliability concerns of modern systems. The first paper performs experimental evaluation of the communication bandwidth and latency of two CPU-FPGA platforms. The second paper presents a framework to automatically generate RTL implementations of neural network accelerators. The third paper presents Ta heterogeneous database accelerator MPSoC that yields significant power efficiency improvements compared to high-end CPU and GPU-based systems. The final paper improves the reliability of FPGA-based reconfigurable architectures by performing kernel-specific transient fault vulnerability reduction.

68.1 A Quantitative Analysis on Microarchitectures of Modern CPU-FPGA Platforms (10:30)
Young-kyu Choi, Jason Cong, Zhenman Fang, Yuchen Hao, Glenn Reinman, **Peng Wei** - *Univ. of California, Los Angeles, CA*

68.2 DeepBurning: Automatic Generation of FPGA-based Learning Accelerators for the Neural Network Family (10:45)
Ying Wang - *Chinese Academy of Sciences & Institute of Computing Technology, Beijing, China*
Jie Xu, Yinhe Han, Huawei Li - *Institute of Computing Technology & Chinese Academy of Sciences & Univ. of Chinese Academy of Sciences, Beijing, China*
Xiaowei Li - *Chinese Academy of Sciences & Institute of Computing Technology, Beijing, China*

68.3 Resource Budgeting for Reliability in Reconfigurable Architectures (11:00)
Hongyan Zhang, Lars Bauer, Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

68.4 An MPSoC for Energy-Efficient Database Query Processing (11:15)
Sebastian Haas, Oliver Arnold, Benedikt Nöthen, Tobias Seifert, Friedrich Pauls, Mattis Hasler, Yong Chen, Hermann Hensel, Sadia Moriam, Emil Matúš, Stefan Scholze, Georg Ellguth, Andreas Dixius, Sebastian Höppner, Stefan Schiefer, Stephan Hartmann, Stephan Henker, Thomas Hocker, Jörg Schreiter - *Technische Univ. Dresden, Germany*
Holger Eisenreich - *RacylCs GmbH, Dresden, Germany*
Jens-Uwe Schlüßler, Dennis Walter, Christian Mayr, René Schüffny, Gerhard P. Fettweis - *Technische Univ. Dresden, Germany*

A Q&A poster session will immediately follow the presentations from 11:30am to 12:00pm.

69 DESIGN UNDER VARIATION: HOW DO YOU VERIFY TIMING?

Time: 10:30am - 12:00pm || Room: 19AB || Event Type: Reviewed Presentations
Track: EDA || Topic Area: Modeling, Simulation & Timing

CHAIR:
Hung-Ming Chen - *National Chiao Tung Univ., Hsinchu, Taiwan*

CO-CHAIR:
Yasuhiro Takashima - *Univ. of Kitakyushu, Japan*

The accuracy and efficiency of timing analysis in the presence of variation is critical for VLSI design. This session presents the state of the art on this topic, beginning with integrating various techniques into statistical analysis, including current source models, path tracing methods and smart sampling at the transistor level, and concluding with a distributed timing analysis framework for large scale designs.

69.1 Practical Statistical Static Timing Analysis with Current Source Models (10:30)
Debjit Sinha - *IBM Corp., Poughkeepsie, NY*
Vladimir Zolotov - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Sheshashayee K. Raghunathan - *IBM Corp., Bangalore, India*
Michael H. Wood - *IBM Systems and Technology Group, Poughkeepsie, NY*
Kerim Kalafala - *IBM Corp., Poughkeepsie, NY*

69.2 Statistical Path Tracing in Timing Graphs (10:45)
Vasant B. Rao, Debjit Sinha - *IBM Corp., Poughkeepsie, NY*
Nitin Srimal, Prabhat K. Maurya - *IBM Corp., Bangalore, India*

69.3 Efficient Transistor-level Timing Yield Estimation via Line Sampling (11:00)
Hiromitsu Awano, Takashi Sato - *Kyoto Univ., Kyoto, Japan*

69.4 A Distributed Timing Analysis Framework for Large Designs (11:15)
Tsung-Wei Huang, Martin D.F. Wong - *Univ. of Illinois at Urbana-Champaign, IL*
Debjit Sinha, Kerim Kalafala, Natesan Venkateswaran - *IBM Corp., Poughkeepsie, NY*

A Q&A poster session will immediately follow the presentations from 11:30am to 12:00pm.

70 MEMORY THAT NEVER FORGETS

Time: 10:30am - 12:00pm || Room: 17AB || Event Type: Reviewed Presentations
Track: EDA, Design || Topic Area: Emerging Technologies, System Architectures & SoC

CHAIR:
Jishen Zhao - *Univ. of California, Santa Cruz, CA*

CO-CHAIR:
Dimin Niu - *Samsung Semiconductor, Inc., Santa Clara, CA*

Emerging non-volatile memory technologies enable new opportunities for architecture designs and novel applications. The first paper introduces a novel programmable logic-in-memory design (PLiM) using majority-inverter graphs with the ReRAM technology. The second paper describes memory design with Ferroelectric FETs. The third paper proposes a new register file design with STT-RAM for GPGPU, with techniques to reduce write overheads for minimizing energy. The last paper addresses the read reliability and write power concerns in STT-RAM with pseudo-differential sensing schemes.

70.1 An MIG-based Compiler for Programmable Logic-in-Memory Architectures (10:30)
Mathias Soeken - *École Polytechnique Fédérale de Lausanne, Switzerland*
Saeideh Shirinzadeh - *Univ. of Bremen, Germany*
Pierre-Emmanuel Gaillardon - *Univ. of Utah, Salt Lake City, UT*
Luca Amaru - *École Polytechnique Fédérale de Lausanne, Switzerland*
Rolf Drechsler - *Univ. of Bremen & DFKI GmbH, Germany*
Giovanni De Micheli - *École Polytechnique Fédérale de Lausanne, Switzerland*

70.2 Nonvolatile Memory Design Based on Ferroelectric FETs (10:45)
Sumitha George, Kaisheng Ma - *Pennsylvania State Univ., State College, PA*
Ahmedullah Aziz - *Pennsylvania State Univ., University Park, PA*
Xueqing Li - *Pennsylvania State Univ., State College, PA*
John Sampson - *Pennsylvania State Univ., University Park, PA*
Asif Khan, Sayeef Salahuddin - *Univ. of California, Berkeley, CA*
Meng-Fan Chang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Suman Datta, Sumeet K. Gupta, Vijaykrishnan Narayanan - *Pennsylvania State Univ., University Park, PA*

70.3 Architecting Energy-efficient STT-RAM based Register File for GPGPUs via Delta Compression (11:00)
Hang Zhang, Xuhao Chen - *National Univ. of Defense Technology, Changsha, China*
Nong Xiao - *National Univ. of Defense Technology & Sun Yat-sen Univ., Changsha, China*
Fang Liu - *National Univ. of Defense Technology, Changsha, China*

70.4 PDS: Pseudo-Differential Sensing Scheme for STT-MRAM (11:15)
Wang Kang, Tingting Pang, Bi Wu, Weifeng Lv, Youguang Zhang - *Beihang Univ., Beijing, China*
Guangyu Sun - *Peking Univ., Beijing, China*
Weisheng Zhao - *Beihang Univ. & Univ. Paris-Sud, Beijing, China*

A Q&A poster session will immediately follow the presentations from 11:30am to 12:00pm.

71 SECURE IOT: UTOPIA, ALCHEMY, OR POSSIBLE FUTURE?

Time: 10:30am - 12:00pm || Room: 18AB || Event Type: Invited Presentations
Track: Security, IoT || Topic Area: Cyber-Physical Systems, System Architectures & SoC, General Interest

CHAIRS:
Anand Rajan - *Intel Corp., Portland, OR*
Saverio Fazzari - *Booz Allen Hamilton, Inc., Clarksville, MD*

ORGANIZERS:
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*
Yier Jin - *Univ. of Central Florida, Orlando, FL*

The Internet of Things (IoT) has become a popular concept in both industry and academic settings, bringing along the vision of a bright future where all “unconnected” things become “connected.” Whereas such a tightly connected world brings about many benefits to our civilization, it comes at the cost of privacy and security. The internet revolution has already showed us once that leaving security as an afterthought has devastating consequences. Repeating the same mistake with IoT would destroy the utopic future we are aiming for.

In this special session IoT architects from academia and industry discuss their views on how to properly secure IoT from the start, addressing challenges of secure communication from the single IoT device, to groups of devices, to the backbone network.

71.1 Things, Trouble, Trust: On Building Trust in IoT Systems (10:30)
Tigist Abera - *Technische Univ. Darmstadt, Germany*
N Asokan - *Aalto Univ., Espoo, Finland*
Lucas Davi - *Technische Univ. Darmstadt, Germany*
Farinaz Koushanfar - *Univ. of California at San Diego, La Jolla, CA*
Andrew Raverd - *Aalto Univ., Espoo, Finland*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*
Gene Tsudik - *Univ. of California, Irvine, CA*

71.2 Exploring risk and mapping the Internet of Things with Autonomous Drones (11:00)
Paul Jauregui - *Praetorian, Austin, TX*

71.3 Can IoT be Secured: Emerging Challenges in Connecting the Unconnected (11:30)
Nancy Cam-Winget - *Cisco Systems, Inc., San Jose, CA*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*
Yier Jin - *Univ. of Central Florida, Orlando, FL*

72 RESEARCH FUNDING LANDSCAPE FOR 2020 AND BEYOND

Time: 10:30am - 12:00pm || Room: 15 || Event Type: Invited Presentations
Track: EDA, Embedded Systems || Topic Area: General Interest

CHAIR:
William Joyner - *Semiconductor Research Corp., Durham, NC*

ORGANIZER:
Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

Do you wonder what the critical research areas relating to hardware design and EDA will be in 10 years? In this session, agency directors from NSF, DARPA and NIH will discuss their vision on upcoming research problems for the next decade and what is the related funding landscape they foresee.

72.1 DARPA View (10:30)
William Chappell - *Defense Advanced Research Projects Agency, Arlington, VA*

72.2 Looking forward: Outlines of an NSCI, Architecture and Systems Research Agenda (11:00)
James Kurose - *National Science Foundation, Arlington, VA*

72.3 NIH, High Performance Computing and Biomedical Sciences (11:30)
Susan Gregurick - *National Institutes of Health - NIGMS, Bethesda, MD*

SKY TALK: BIOLOGICAL ELECTRONICS: MERGING LIFE'S TRANSISTORS WITH THE SOLID-STATE

Time: 1:00pm - 1:30pm || Room: 17AB || Event Type: SKY Talk || Track: Design, EDA
Topic Area: Emerging Technologies

ORGANIZER:
Rob Aitken - *ARM, Inc., San Jose, CA*

Silicon integrated circuits based on CMOS technology form the basis for complex electronic systems with more than 10 billion transistors in a single chip. As the scaling of solid-state devices through Moore's Law reaches an end and there is a search to expand the capabilities of CMOS technology to new applications through the addition of new materials ("more than Moore"), biological components represent a largely untapped opportunity. Living systems have lipid bilayer membranes, which act as capacitors, storing charge as ionic gradients across these membranes. Proteins that permeate these membranes (transmembrane proteins) are versatile biological electronic devices, controlling ion flow through the membrane. These proteins can harvest energy from the environment (and store this energy as electrochemical potentials) and can sense the environment (other molecules, temperature, pH, voltage, mechanical forces) and signal this by opening or closing the ion channel through the membrane.

As a first foray into this exciting new area of exploration, we powered an integrated circuit using adenosine triphosphate (ATP), the energy currency of living systems, by integrating with a CMOS circuit an artificial cell membrane containing ATPase pumps that hydrolyze ATP and pump ions, producing a transmembrane potential that can power the solid-state integrated circuit. Despite these primitive first steps, this co-integration of CMOS and transmembrane proteins has the potential for impact a large number of applications: molecular diagnostics and drug discovery by providing new nanoscale sophistication to electrophysiological interfaces; new sensing systems for smell and taste; and the ability to detect and treat disease with real-time feedback through autonomous hybrid systems that could be symbiotic probes in living organisms. There may also be possibility to exploit the mechanical nature of ion channels and the ultra-low-voltage operation that they support to create hybrid ultra-low-power biological co-processors to augment CMOS in signal processing and computational applications.

SPEAKER:
Kenneth Shepard - *Columbia Univ., New York, NY*

73 DEPTH MATTERS! ARCHITECTURES FOR DEEP LEARNING IN HARDWARE

Time: 1:30pm - 3:00pm || Room: 12AB || Event Type: Reviewed Presentations
Track: EDA || Topic Area: Emerging Technologies

CHAIR:
Rangharajan Venkatesan - *NVIDIA Corp, Santa Clara, CA*

CO-CHAIR:
Jae-sun Seo - *Arizona State Univ., Phoenix, AZ*

Deep learning networks have recently emerged as one of the most promising approaches to machine learning, and are advancing the field at a rapid pace. How can these networks be implemented in hardware? The papers in the session answer this question using novel approaches and emerging device technologies.

73.1 C-Brain:A deep learning accelerator that tames the diversity of CNNs through adaptive data-level parallelization (1:30)
Lili Song, Ying Wang, Yinhe Han, Xin Zhao, Bosheng Liu, Xiaowei Li - *Chinese Academy of Sciences & Institute of Computing Technology, Beijing, China*

73.2 Dynamic Energy-Accuracy Trade-off Using Stochastic Computing in Deep Neural Networks (1:45)
Kyounghoon Kim - *Samsung Electronics Co., Ltd. & Seoul National Univ., Seoul, Republic of Korea*
Jungki Kim, **Joonsang Yu**, Jungwoo Seo - *Seoul National Univ., Seoul, Republic of Korea*
Jongeun Lee - *Ulsan National Institute of Science and Technology (UNIST), Ulsan, Republic of Korea*
Kiyoung Choi - *Seoul National Univ., Seoul, Republic of Korea*

73.3 Switched by Input: Power Efficient Structure for RRAM-based Convolutional Neural Network (2:00)
Lixue Xia, Tianqi Tang, Wenqin Huangfu, Ming Cheng, Xiling Yin, Boxun Li, Yu Wang, Huazhong Yang - *Tsinghua Univ., Beijing, China*

73.4 Simplifying Deep Neural Networks for Neuromorphic Architectures (2:15)
Jaeyong Chung, Taehwan Shin - *Incheon National Univ., Incheon, Republic of Korea*

A Q&A poster session will immediately follow the presentations from 2:30pm to 3:00pm.

74 TO APPROXIMATE OR TO MAKE RESILIENT?

Time: 1:30pm - 3:00pm || Room: 13AB || Event Type: Reviewed Presentations
Track: EDA, Design || Topic Area: Logic & High-Level Synthesis, Low-Power & Reliability

CHAIR:
Michael Orshansky - *Univ. of Texas at Austin, TX*

CO-CHAIR:
Sunil Khatri - *Texas A&M Univ., College Station, TX*

Approximate computing is an emerging design approach that exploits the intrinsic error resilience of many applications to improve power efficiency. This session has papers that address approximate computing at various levels - the design of approximate adders, synthesis of approximate circuits, and verification of approximate sequential circuits. The session concludes with a paper that discusses improving timing error resilience at the circuit level.

74.1 A Low-power Carry Cut-Back Approximate Adder with Fixed-point Implementation and Floating-point Precision (1:30)
Vincent Camus, Jeremy Schlachter, Christian C. Enz - *École Polytechnique Fédérale de Lausanne, Switzerland*

74.2 An Efficient Method for Multi-level Approximate Logic Synthesis under Error Rate Constraint (1:45)
Yi Wu, **Weikang Qian** - *Shanghai Jiao Tong Univ., Shanghai, China*

74.3 Precise Error Determination of Approximated Components in Sequential Circuits With Model Checking (2:00)
Arun Chandrasekharan - *Univ. of Bremen, Germany*
Mathias Soeken - *École Polytechnique Fédérale de Lausanne, Switzerland*
Daniel Grosse, Rolf Drechsler - *Univ. of Bremen & DFKI GmbH, Germany*

74.4 Area Optimization of Resilient Designs Guided by a Mixed Integer Geometric Program (2:15)
Hsin-Ho Huang, Huimei Cheng - *Univ. of Southern California, Los Angeles, CA*
Chris Chu - *Iowa State Univ., Ames, IA*
Peter A. Beerel - *Univ. of Southern California, Los Angeles, CA*

A Q&A poster session will immediately follow the presentations from 2:30pm to 3:00pm.

75 SCHEDULING FOR MULTI-CORE AND MIXED-CRITICALITY EMBEDDED SYSTEMS

Time: 1:30pm - 3:00pm || Room: 18CD || Event Type: Reviewed Presentations
Track: Embedded Systems || Topic Area: System Software, Cyber-Physical Systems

CHAIR:
Riccardo Bettati - *Texas A&M Univ., College Station, TX*

CO-CHAIR:
Nan Guan - *Hong Kong Polytechnic Univ., Hong Kong, Hong Kong*

The recent introduction of multi-core and mixed-criticality systems has resulted in the need for new scheduling algorithms capable of handling these systems. The first paper generalizes harmonicity to real-time tasks with deadlines shorter than periods, and applies it to workload partitioning on multi-cores. The second paper proposes a probabilistic framework for design and analysis of real-time mixed-criticality systems. The third paper introduces a distributed scheduler for many-core systems based on cooperative game theory to reduce inter-core processing overheads. The last paper derives utilization bounds for partitioned rate-monotonic multiprocessor scheduling of multi-mode real-time task systems.

75.1 On Harmonic Fixed-Priority Scheduling of Periodic Real-Time Tasks with Constrained Deadlines (1:30)
Tianyi Wang, Qiushi Han, Shi Sha, Wujie Wen, **Gang Quan**
- *Florida International Univ., Miami, FL*
Meikang Qiu - *Pace Univ., New York, NY*

75.2 A Probabilistic Scheduling Framework for Mixed-Criticality Systems (1:45)
Alejandro Masrur - *Technical Univ. of Chemnitz, Germany*

75.3 Distributed Scheduling for Many-Cores Using Cooperative Game Theory (2:00)
Anuj Pathania - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Vanchinathan Venkataramani - *National Univ. of Singapore, Singapore*
Muhammad Shafique - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Tulika Mitra - *National Univ. of Singapore, Singapore*
Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

75.4 Utilization Bounds on Allocating Rate-Monotonic Scheduled Multi-Mode Tasks on Multiprocessor Systems (2:15)
Wen-Hung K. Huang, Jian-Jia Chen - *Technische Univ. Dortmund, Germany*

A Q&A poster session will immediately follow the presentations from 2:30pm to 3:00pm.

76 HIGH-LEVEL SYNTHESIS: REACHING FOR THE STARS!

Time: 1:30pm - 3:00pm || Room: 19AB || Event Type: Reviewed Presentations || Track: EDA, IP
Topic Area: Logic & High-Level Synthesis, Low-Power & Reliability

CHAIR:
Andres Takach - *Mentor Graphics Corp., Wilsonville, OR*

CO-CHAIR:
Takashi Sato - *Kyoto Univ., Kyoto, Japan*

This session features papers on enhancing HLS technology, beyond its fundamentals. Papers describe techniques that help in selecting promising micro-architecture directives to get the best circuit; building IP libraries for data structures to enable broader deployment, and using HLS to improving circuit reliability.

76.1 DAG-Aware Logic Synthesis of Datapaths (1:30)
Cunxi Yu - *Univ. of Massachusetts, Amherst, MA*
Mihir Choudhury - *IBM T.J. Watson Research Center, New York, NY*
Andrew Sullivan - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Maciej Ciesielski - *Univ. of Massachusetts, Amherst, MA*

76.2 Lin-Analyzer: A High-level Performance Analysis Tool for FPGA-based Accelerators (1:45)
Guanwen Zhong, Alok Prakash - *National Univ. of Singapore, Singapore*
Yun Liang - *Peking Univ., Beijing, China*
Tulika Mitra - *National Univ. of Singapore, Singapore*
Smail Niar - *Univ. of Valenciennes, France*

76.3 Improving High-Level Synthesis with Decoupled Data Structure Optimization (2:00)
Ritchie Zhao, Gai Liu, Shreesha Srinath, Christopher Batten, Zhiru Zhang - *Cornell Univ., Ithaca, NY*

76.4 StitchUp: Automatic Control Flow Protection for High Level Synthesis Circuits (2:15)
Shane T. Fleming, David Thomas - *Imperial College London, United Kingdom*

A Q&A poster session will immediately follow the presentations from 2:30pm to 3:00pm.

77 DON'T BE AN IDIoT: INTELLIGENT DESIGN FOR THE INTERNET OF THINGS

Time: 1:30pm - 3:00pm || Room: 17AB || Event Type: Reviewed Presentations
Track: IoT, Design || Topic Area: Cyber-Physical Systems, Codesign & System Design

CHAIR:
Avesta Sasan - *George Mason Univ., Fairfax, VA*

CO-CHAIR:
Yongpan Liu - *Tsinghua Univ., Beijing, China*

The heterogeneous and distributed nature of IoT requires novel design techniques. This session presents emerging approaches to reduce the effort in designing distributed and dynamic sensing systems, ranging from automatic learning and auto-generation to semantics-aware design and statistical sampling.

77.1 Plug-n-Learn: Automatic Learning of Computational Algorithms in Human-Centered Internet-of-Things Applications (1:30)
Seyed Ali Rokni, Hassan Ghasemzadeh - *Washington State Univ., Pullman, WA*

77.2 A Semantics-Aware Design for Mounting Remote Sensors on Mobile Systems (1:45)
Yu-Wen Jong - *National Taiwan Univ., Taipei, Taiwan*
Pi-Cheng Hsiu - *Academia Sinica, Taipei, Taiwan*
Sheng-Wei Cheng - *National Taiwan Univ., Taipei, Taiwan*
Tei-Wei Kuo - *Academia Sinica & National Taiwan Univ., Taipei, Taiwan*

77.3 Re-target-able software power management framework using SoC data auto-generation (2:00)
Piyali Goswami, Sushaanth Srirangapathi - *Texas Instruments India Pvt. Ltd., Bangalore, India*
Chetan Matad - *PathPartner Technology Pvt. Ltd. & Texas Instruments India Pvt. Ltd., Bangalore, India*
Stanley Liu - *Texas Instruments, Inc., Dallas, TX*

77.4 Efficient Design Space Exploration via Statistical Sampling and AdaBoost Learning (2:15)
Dandan Li, Shuzhen Yao - *Beihang Univ., Beijing, China*
Yu-Hang Liu - *Illinois Institute of Technology, Chicago, IL*
Senzhang Wang - *Beihang Univ., Beijing, China*
Xian-He Sun - *Illinois Institute of Technology, Chicago, IL*

A Q&A poster session will immediately follow the presentations from 2:30pm to 3:00pm.

78 NEAR-FIELD IOT: DESIGN AND CAD CHALLENGES

Time: 1:30pm - 3:00pm || Room: 18AB || Event Type: Invited Presentations || Track: IoT, EDA
Topic Area: Circuit Design, Emerging Technologies, Physical Design

CHAIRS:
Eric Keiter - *Sandia National Laboratories, Albuquerque, NM*
Peng Li - *Texas A&M Univ., College Station, TX*

ORGANIZER:
Ibrahim Elfadel - *Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates*

Near-field IoT solutions comprise devices and applications that leverage high-frequency data sensing for near-field imaging, sensing, and communication. They use the untapped and unregulated spectrum between 200GHz and 1000GHz – the Terahertz range.

Such applications include medical, safety and security imaging; non-destructive testing; gas, explosive, and water detection; and food inspection. In the pharmaceutical industry, target applications are lab-on-chip systems, protection against medication tampering, and drug distinction.

In this special session we will bring experts from academia and industry to present the challenges that design engineers and CAD developers will be facing to extend the reach of the Internet of Things to such near-range, high-frequency applications. The three presentations of this session will cover many examples of near-field IoT applications, several design examples, and discuss the landscape of CAD methodologies and tools in this emerging research area.

78.1 Ultra Low Power Integrated Transceivers for Near-Field IoT (1:30)
Mihai Sanduleanu, Ibrahim (Abe) Elfadel - *Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates*

78.2 Integrated Millimeter-Wave/Terahertz Sensor Systems for Near-Field IoT (2:00)
Payam Heydari - *Univ. of California, Irvine, CA*

78.3 Near-Field IoT: Is CAD Ready? (2:30)
Sharad Kapur - *Integrand Software, Inc., Berkeley Heights, NJ*

79 WHO IS THE BIGGEST THREAT TO TOMORROW'S SECURITY? YOU, THE HARDWARE DESIGNER

Time: 1:30pm - 3:00pm || Room: 15 || Event Type: Invited Presentations || Track: Security, Design
Topic Area: Circuit Design, System Architectures & SoC, System Software

CHAIR:
Michael Chen - *Mentor Graphics Corp., Wilsonville, OR*

ORGANIZER:
Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

More and more security attacks today are perpetrated by exploiting the hardware: side-channel attacks leak secret keys to the outside world, weak random number generators render cryptography ineffective, fault-based attacks can compromise authentication, etc. Moreover, many of the tenets of efficient design are in tension with guaranteeing security. For instance, classic secure hardware does not allow to optimize common execution patterns, share resources or provide deep introspection.

In this session, speakers will educate the attendees on potential pitfalls and demonstrate technologies that effectively provide security without compromising a design's efficiency qualities, e.g., performance and power.

79.1 Protecting Security Primitives from Manufacturing Attacks (1:30)
Wayne Burleson - *Univ. of Massachusetts & Advanced Micro Devices, Inc., Amherst, MA*

79.2 The Row Hammer Problem and Other Issues We May Face as Memory Becomes Denser (2:00)
Onur Mutlu - *Carnegie Mellon Univ., Pittsburgh, PA*

79.3 Side-Channel Free Architectures (2:30)
Mohit Tiwari - *Univ. of Texas at Austin, TX*

80 SYNTHESIS FOR MICROFLUIDIC AND QUANTUM TECHNOLOGIES

Time: 3:30pm - 5:00pm || Room: 12AB || Event Type: Reviewed Presentations
Track: EDA || Topic Area: Emerging Technologies

CHAIR:
Robert Wille - *Johannes Kepler Univ. of Linz, Austria*

CO-CHAIR:
Shih-Hsu Huang - *Chung Yuan Christian Univ., Taoyuan City, Taiwan*

Increasing complexity of microfluidic and reversible circuits requires design automation. This session addresses synthesis of micro-electrode-dot-array digital microfluidic biochips, continuous-flow microfluidic biochips, boolean satisfiability using quantum annealing and reversible circuits.

80.1 High-Level Synthesis for Micro-Electrode-Dot-Array Digital Microfluidic Biochips (3:30)
Zipeng Li - *Duke Univ., Durham, NC*
Kelvin Yi-Tse Lai, Po-Hsien Yu - *National Chiao Tung Univ., Hsinchu, Taiwan*
Tsung-Yi Ho - *National Tsing Hua Univ., Hsinchu, Taiwan*
Krishnendu Chakrabarty - *Duke Univ., Durham, NC*
Chen-Yi Lee - *National Chiao Tung Univ., Hsinchu, Taiwan*

80.2 Columba: Co-Layout Synthesis for Continuous-Flow Microfluidic Biochips (3:45)
Tsun-Ming Tseng, **Mengchu Li**, Bing Li - *Technische Univ. München, Germany*
Tsung-Yi Ho - *National Tsing Hua Univ., Hsinchu, Taiwan*
Ulf Schlichtmann - *Technische Univ. München, Germany*

80.3 A Quantum Annealing Approach for Boolean Satisfiability Problem (4:00)
Juexiao Su, Tianheng Tu - *Univ. of California, Los Angeles, CA*
Lei He - *Univ. of California, Los Angeles & Fudan State Key Lab for Application Specific Circuits and Systems, Los Angeles, CA*

80.4 Unlocking Efficiency and Scalability of Reversible Logic Synthesis using Conventional Logic Synthesis (4:15)
Mathias Soeken - *École Polytechnique Fédérale de Lausanne, Switzerland*
Anupam Chattopadhyay - *Nanyang Technological Univ., Singapore, Singapore*

A Q&A poster session will immediately follow the presentations from 4:30pm to 5:00pm.

81 IT'S ALL ABOUT MANAGEMENT! LOW POWER AT THE SYSTEM LEVEL

Time: 3:30pm - 5:30pm || Room: 13AB || Event Type: Reviewed Presentations
Track: EDA, Embedded Systems || Topic Area: System Architectures & SoC, Codesign & System Design, Low-Power & Reliability

CHAIR:
Yanzhi Wang - *Syracuse Univ., Syracuse, NY*

CO-CHAIR:
Muhammad Shafique - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

This session highlights the effects of power management techniques applied at the system level. The presentations describe hardware techniques including DVFS strategies, optimization of the efficiency of voltage regulators, energy harvesting and novel sprinting techniques for dark silicon, as well as software techniques for low power image encoding/decoding.

81.1 SwiftGPU: Fostering Energy Efficiency in a Near-Threshold GPU Through a Tactical Performance Boost (3:30)
Prabal Basu, Hu Chen, Shamik Saha, Koushik Chakraborty, Sanghamitra Roy - *Utah State Univ., Logan, UT*

81.2 VR-Scale: Runtime Dynamic Phase Scaling of Processor Voltage Regulators for Improving Power Efficiency (3:45)
Hadi Asghari-Moghaddam - *Univ. of Illinois at Urbana-Champaign, IL*
Hamid Reza Ghasemi - *Univ. of Wisconsin, Madison, WI*
Abhishek A. Sinkar - *Oracle Corp., Santa Clara, CA*
Indrani Paul - *Advanced Micro Devices, Inc., Austin, TX*
Nam Sung Kim - *Univ. of Illinois at Urbana-Champaign, IL*

81.3 Exploration of Associative Power Management with Instruction Governed Operation for Ultra-low Power Design (4:00)
Tianyu Jia, Yuanbo Fan, Russ Joseph, Jie Gu - *Northwestern Univ., Evanston, IL*

81.4 MORPh: Mobile OLED-friendly Recording and Playback System for Low Power Video Streaming (4:15)
Xiang Chen, Jiachen Mao, Jiafei Gao, Kent Nixon, Yiran Chen - *Univ. of Pittsburgh, PA*

81.5 HW/SW Co-design of Nonvolatile IO System in Energy Harvesting Sensor Nodes for Optimal Data Acquisition (4:30)
Zewei Li, Yongpan Liu, Daming Zhang, Zhangyuan Wang, Xin Shi, Wenyu Sun - *Tsinghua Univ., Beijing, China*
Chun Jason Xue - *City Univ. of Hong Kong, Hong Kong*
Jiwu Shu, Huazhong Yang - *Tsinghua Univ., Beijing, China*

81.6 Shift Sprinting: Fine-Grained Temperature-Aware NoC-based MCSoC Architecture in Dark Silicon Age (4:45)
Amin Rezaei, **Danella Zhao** - *Univ. of Louisiana at Lafayette, LA*
Masoud Daneshtalab - *Royal Institute of Technology, Kista, Sweden*
Hongyi Wu - *Univ. of Louisiana at Lafayette, LA*

A Q&A poster session will immediately follow the presentations from 5:00pm to 5:30pm.

82 RENDEZVOUS IN EMBEDDED SYSTEMS: SCHEDULING PROBLEMS AND SOLUTIONS

Time: 3:30pm - 5:30pm || Room: 18CD || Event Type: Reviewed Presentations
Track: Embedded Systems || Topic Area: System Architectures & SoC, Codesign & System Design, Low-Power & Reliability

CHAIR:
Kyoungwoo Lee - *Yonsei Univ., Seoul, Republic of Korea*

CO-CHAIR:
Dip Goswami - *Technische Univ. Eindhoven, Netherlands Antilles*

The design of emerging embedded systems requires scheduling to coordinate hardware and software components. System quality would degrade due to insufficient battery capacity, careless coarse-grained evaluations, or uncertainty resulting from shared components or incorrect predictions. The first paper of this session discusses how to cope with nonvolatile processors when the power switching overhead can be significant. The second paper presents SoCs with fine-grained DVFS capabilities. The next two papers provide analytical and scheduling solutions for shared hardware and software components in real-time embedded systems, followed by an optimal and fast approach to schedule cyclo-static dataflow (CSDF). The session concludes with a design space exploration method to account for prediction uncertainty.

82.1 Performance-Aware Task Scheduling for Energy Harvesting Nonvolatile Processors Considering Power Switching Overhead (3:30)
Hehe Li, Yongpan Liu - *Tsinghua Univ., Beijing, China*
Chenchen Fu, Chun Jason Xue - *City Univ. of Hong Kong, Hong Kong*
Donglai Xiang, Jinshan Yue, Jinyang Li, Daming Zhang - *Tsinghua Univ., Beijing, China*
Jingtong Hu - *Oklahoma State Univ., Stillwater, OK*
Huazhong Yang - *Tsinghua Univ., Beijing, China*

82.2 An FPGA-Based Infrastructure for Fine-Grained DVFS Analysis in High-Performance Embedded Systems (3:45)
Paolo Mantovani, Emilio G. Cota, Kevin Tien, Christian Pilato, Giuseppe Di Guglielmo, Ken Shepard, Luca P. Carloni - *Columbia Univ., New York, NY*

82.3 MIRROR: Symmetric Timing Analysis for Real-Time Tasks on Multicore Platforms with Shared Resources (4:00)
Wen-Hung Huang, Jian-Jia Chen - *Technische Univ. Dortmund, Germany*
Jan Reineke - *Saarland Univ., Saarbrücken, Germany*

82.4 Real-Time Co-Scheduling of Multiple Dataflow Graphs on Multi-Processor Systems (4:15)
Shin-haeng Kang, Duseok Kang - *Seoul National Univ., Seoul, Republic of Korea*
Hoeseok Yang - *Ajou Univ., Suwon, Republic of Korea*
Soonhoi Ha - *Seoul National Univ., Seoul, Republic of Korea*

82.5 Optimal and Fast Throughput Evaluation of CSDF (4:30)
Bruno Bodin - *Univ. of Edinburgh, Edinburgh, United Kingdom*
Alix Munier Kordon - *LIP6 Laboratory, CNRS, Univ. Pierre et Marie Curie, Paris, France*
Benoît Dupont de Dinechin - *Kalray Corp., Montbonnot-Saint-Martin, France*

82.6 An Expected Hypervolume Improvement Algorithm for Architectural Exploration of Embedded Processors (4:45)
Hongwei Wang - *Institute of Computing Technology & Chinese Academy of Sciences & Univ. of Chinese Academy of Sciences, Beijing, China*
Jinglin Shi, Ziyuan Zhu - *Institute of Computing Technology & Chinese Academy of Sciences, Beijing, China*

A Q&A poster session will immediately follow the presentations from 5:00pm to 5:30pm.

83 THE HARDWARE-SECURITY FORCE AWAKENS

Time: 3:30pm - 5:30pm || Room: 19AB || Event Type: Reviewed Presentations || Track: Security
Topic Area: System Architectures & SoC, Codesign & System Design

CHAIR:
Michail Maniatakos - *New York Univ., Abu Dhabi, United Arab Emirates*

CO-CHAIR:
Jeff Draper - *Univ. of Southern California, Los Angeles, CA*

Hardware security research has entered a new era where we are not just protecting the hardware platform. The papers in this session awaken the force inside the hardware to protect systems efficiently and effectively in multiple ways.

Encryption of data in non-volatile memory, split-manufacturing, design of public PUFs and cryptographic primitives, reusing design-for-debug infrastructure and optimizing microprocessors for control flow integrity.

83.1 Lattice-based Encryption Over Standard Lattices in Hardware (3:30)
James Howe, Ciara Moore, Máire O'Neill - *Queen's Univ. Belfast, United Kingdom*
Francesco Regazzoni - *ALaRI, Lugano, Switzerland*
Tim Guneysu - *Univ. of Bremen, Germany*
Kevin Beeden - *Thales, Reading, United Kingdom*

83.2 Strategy Without Tactics: Policy-Agnostic Hardware-Enhanced Control-Flow Integrity (3:45)
Dean Sullivan, Orlando Arias - *Univ. of Central Florida, Orlando, FL*
Lucas Davi - *Technische Univ. Darmstadt, Germany*
Per Larsen - *Univ. of California, Irvine, CA*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*
Yier Jin - *Univ. of Central Florida, Orlando, FL*

83.3 Practical Public PUF Enabled by Solving Max-Flow Problem on Chip (4:00)
Meng Li - *Univ. of Texas at Austin, TX*
Jin Miao - *Cadence Design Systems, Inc., San Jose, CA*
Kai Zhong, David Z. Pan - *Univ. of Texas at Austin, TX*

83.4 The Cat and Mouse in Split Manufacturing (4:15)
Yujie Wang - *Texas A&M Univ. & Nankai Univ., College Station, TX*
Pu Chen, Jiang Hu - *Texas A&M Univ., College Station, TX*
Jeyavijayan Rajendran - *Univ. of Texas at Dallas, TX*

83.5 SECRET: Smartly EnCRypted Energy EfficienT Non-Volatile Memories (4:30)
Shivam Swami, Joydeep Rakshit, Kartik Mohanram - *Univ. of Pittsburgh, PA*

83.6 Exploiting Design-for-Debug for Flexible SoC Security Architecture (4:45)
Abhishek Basak - *Case Western Reserve Univ., Cleveland, OH*
Swarup Bhunia - *Univ. of Florida, Gainesville, FL*
Sandip Ray - *Intel Corp., Hillsboro, OR*

A Q&A poster session will immediately follow the presentations from 5:00pm to 5:30pm.

84 LIVE FOREVER: CHALLENGES IN NONVOLATILE MEMORY SYSTEMS

Time: 3:30pm - 5:30pm || Room: 17AB || Event Type: Reviewed Presentations
Track: Embedded Systems || Topic Area: Emerging Technologies

CHAIR:
Myoungsoo Jung - *Yonsei Univ., Seoul, Republic of Korea*

CO-CHAIR:
Yu Wang - *Tsinghua Univ., Beijing, China*

NVM technology provides promising solutions for memory and storage bottlenecks in the big data era. However, it also brings grand challenges in architecture, system and software. This session addresses several emerging issues in NVM design from NVM control unit to NVM cache. The topics in this session include bank-level parallelism, run-time monitoring for process variation, cache management, and in-memory processing.

84.1 Fine-Granularity Tile-Level Parallelism in Non-volatile Memory Architecture with Two-Dimensional Bank Subdivision (3:30)
Matthew Poremba - *Pennsylvania State Univ. & Advanced Micro Devices, Inc., University Park, PA*
Tao Zhang - *NVIDIA Corp & Pennsylvania State Univ., Santa Clara, CA*
Yuan Xie - *Univ. of California, Santa Barbara, CA*

84.2 MTJ variation monitor-assisted adaptive MRAM write (3:45)
Shaodi Wang, Hochul Lee, Cecile Grezes, Pedram Khalili, Kang Wang, Puneet Gupta - *Univ. of California, Los Angeles, CA*

84.3 AOS: Adaptive Overwrite Scheme for Energy-Efficient MLC STT-RAM Cache (4:00)
Xunchao Chen, Navid Khoshavi, Jian Zhou, Dan Huang, Ronald F. DeMara, Jun Wang - *Univ. of Central Florida, Orlando, FL*
Wujie Wen - *Florida International Univ., Miami, FL*
Yiran Chen - *Univ. of Pittsburgh, PA*

84.4 Two-Step State Transition Minimization for Lifetime and Performance Improvement on MLC STT-RAM (4:15)
Huizhang Luo - *Chongqing Univ., Chongqing, China*
Jingtong Hu - *Oklahoma State Univ., Stillwater, OK*
Liang Shi - *Chongqing Univ., Chongqing, China*
Chun Jason Xue - *City Univ. of Hong Kong, Hong Kong*
Qingfeng Zhuge - *Chongqing Univ., Chongqing, China*

84.5 Write-back aware shared last-level cache management for hybrid main memory (4:30)
Deshan Zhang, **Lei Ju**, Mengying Zhao, Xiang Gao, Zhiping Jia - *Shandong Univ., Jinan, China*

84.6 Pinatubo: A Processing-in-Memory Architecture for Bulk Bitwise Operations in Emerging Non-volatile Memories (4:45)
Shuangchen Li - *Univ. of California, Santa Barbara, CA*
Cong Xu - *Hewlett-Packard Labs., Palo Alto, CA*
Qiaosha Zou - *Univ. of California & Huawei Technologies Co., Ltd., Santa Barbara, China*
Jishen Zhao - *Univ. of California, Santa Cruz, CA*
Yu Lu - *Qualcomm, Inc., San Diego, CA*
Yuan Xie - *Univ. of California, Santa Barbara, CA*

A Q&A poster session will immediately follow the presentations from 5:00pm to 5:30pm.

85 WHAT IS THE REAL COST OF VERIFICATION

Time: 3:30pm - 4:30pm || Room: 18AB || Event Type: Panel || Track: EDA
Topic Area: Test & Verification

MODERATOR:
Kelly Larson - *Paradigm Works, Inc., Austin, TX*

It has become commonly accepted knowledge that verification comprises 50%, 60% or even 70% of design cost, but less well-known is where these percentages come from and what they mean. Does design cost include both hardware and software development? What about amortization of IP and EDA costs? Does verification cost include validation, DFT or timing closure? Are debug costs included? Pre or post silicon? How are company-wide infrastructure costs allocated? While identifying costs is important, it's equally important to look at improving value. The panel will explore options to measure and improve verification coverage, reduce rework, and improve the chances of first-time silicon success.

PANELISTS:
Harry Foster - *Mentor Graphics Corp., Wilsonville, OR*
Pranav Ashar - *Real Intent, Inc., Sunnyvale, CA*
Subhasish Mitra - *Stanford Univ., Stanford, CA*
Raviv Gal - *IBM Research - Haifa, Israel*

86 PREDICTABLE SYSTEM TIMING - PROBAB(ILISTICAL)LY?

Time: 4:30pm - 5:30pm || Room: 18AB || Event Type: Panel
Track: Automotive, Embedded Systems || Topic Area: Cyber-Physical Systems

MODERATOR:
Marco Di Natale - *Scuola Superiore Sant'Anna, Pisa, Italy*

The predictability of system timing is a default requirement for automotive systems just like for other real-time embedded system application domains. Especially for mixed-criticality applications, the ability to predict timing behavior soundly and accurately gets crucial to system efficiency, so that higher loads can be sustained (as desired) while warranting availability, reliability and responsiveness for the correct execution of critical components of the system (as required).

Those application domains are also witnessing a surge in performance requirements, which reflects the increase in the value-added that the software delivers to the system in those domains. The required levels of performance can only realistically be attained by employing high-performance hardware acceleration features such as cache hierarchies, multicore processors, etc. However, those features are increasingly complex for state-of-the-art static worst-case execution timing (WCET) analysis to handle with reasonable tightness and for affordable effort.

Measurement-based timing analysis is an alternative to static timing analysis that promises to be applicable to complex high-performance architectures at a much lower development cost and possibly higher precision. However, it is generally very challenging if not impossible to guarantee the correctness of measurement-based timing analyses, in particular for complex architectures.

To address this issue, a variation of measurement-based timing analysis called Measurement-Based Probabilistic Timing Analysis (MBPTA) has recently been developed. Its goal is to provide WCET estimates for arbitrarily low probabilities of exceedance, termed probabilistic WCET (pWCET). MBPTA relies on the selective injection of randomization across the execution stack of modern processors, transparent to the application, and with no effect on functional behavior. Randomization is intended to transform unknown timing distributions, which would otherwise incur arbitrarily frequent pathological variations – source of possibly serious repercussions – into well-behaved distributions, whose extreme cases can be quantified to arbitrarily low probability levels.

This panel aims at discussing the viability and the respective advantages of both probabilistic and classical static timing analysis approaches and how they fit the industrial needs and practices in terms of timing verification, both from an application perspective as well as from an processor vendor perspective.

PANELISTS:
Jaume Abella - *Barcelona Supercomputing Center, Barcelona, Spain*
Jan Reineke - *Saarland Univ., Saarbruecken, Germany*
Arne Hamann - *Robert Bosch GmbH, Renningen, Germany*
Glenn Farrall - *Infineon Technologies AG, Bristol, United Kingdom*

87 HOW MUCH MARGIN DO WE REALLY NEED?

Time: 3:30pm - 5:30pm || Room: 15 || Event Type: Invited Presentations
Track: EDA, Design || Topic Area: Lithography & DFM

CHAIR:
Jennifer Dworak - *Southern Methodist Univ., Dallas, TX*

ORGANIZER:
Rob Aitken - *ARM, Inc., San Jose, CA*

Designers add margin to every aspect of their designs, often with good reason. Timing margin in particular is critical to ensuring yield. But how much margin is enough? This session looks at three important aspects of timing signoff – how can tool providers include flexibility for designers to make informed decisions? What do chip makers need to do to ensure that they include enough margin at sign off without leaving performance on the table? Finally, how do margin and chip test interact, since final yield and quality are determined by the ability to detect and remove marginal parts before shipping them.

87.1 Recovering Margin - Challenges in Timing Sign-Off (3:30)
Isadore Katz - *CLK Design Automation, Inc., Boston, MA*

87.2 What Does it Take to Sign Off a Chip? (4:00)
Sorin Dobre - *Qualcomm, Inc., San Diego, CA*

87.3 A Box of Dots: Using Scan-Based Path Delay Test for Timing Verification (4:30)
Alfred Crouch - *SiliconAid Solutions, Austin, TX*
John Potter - *ASSET InterTech, Inc., Austin, TX*

THURSDAY IS TRAINING DAY

TRACK 1, PART I: HOW TO BUILD CLASS-BASED VERIFICATION ENVIRONMENTS IN SYSTEMVERILOG

Time: 10:15am - 1:15pm || Room: Ballroom E || Event Type: Thursday is Training Day || Track: EDA
Topic Area: Test & Verification

This session will teach the key SystemVerilog language skills needed to understand and build class-based constrained random verification environments, as used by UVM. The emphasis will be on learning to apply the concepts of object-oriented programming to the creation of a re-usable test bench infrastructure. Language features will be taught using working code examples, which delegates can run immediately on the EDA Playground website and will be available to use and share after the class.

Topics to be taught include the object-oriented and constrained random language features of SystemVerilog, and more particularly how to use these language features to build a verification environment that includes a component hierarchy and transaction-level communication.

The knowledge taught in this session is an essential prerequisite to the afternoon session on UVM.

This track is taught by Doulos CTO John Aynsley, winner of the Accellera Systems Initiative 2012 Technical Excellence Award for his contribution to the development of language standards

SPEAKER:
John Aynsley - *Doulos, Ringwood, United Kingdom*

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TRACK 2, PART I: SYSTEMVERILOG SYNTHESIS TUNED FOR ASIC AND FPGA DESIGN

Time: 10:15am - 1:15pm || Room: Ballroom F || Event Type: Thursday is Training Day || Track: EDA, Design
Topic Area: Logic & High-Level Synthesis

SystemVerilog can provide a very concise and readable language for RTL design. The use of SystemVerilog as a design language continues to increase as engineers gradually migrate to SystemVerilog from Verilog or VHDL. As a result, synthesis tool support for SystemVerilog is maturing in both the ASIC and FPGA domains.

This session will teach you how to use the SystemVerilog language for hardware design by focusing on the parts of the SystemVerilog language that are widely supported by commercial RTL synthesis tools. This session is aimed at engineers who are currently using Verilog or VHDL for RTL design, and who want to start taking advantage of the power of SystemVerilog to better express their hardware design intent. Language features will be taught using working code examples, which delegates can run immediately on the EDA Playground website and will be available to use and share after the class.

This track is taught by Doug Perry, Doulos Senior Member Technical Staff.

SPEAKER:
Doug Perry - *Doulos, San Jose, CA*

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THURSDAY IS TRAINING DAY

TRACK 3, PART I: INTRODUCTION TO EMBEDDED SECURITY: MAKING SECURITY HARD: HARDWARE SECURITY AND HOW TO USE IT

Time: 10:15am - 1:15pm || Room: Ballroom G || Event Type: Thursday is Training Day
Track: Embedded Systems, Security || Topic Area: System Software, General Interest

Security is a hot topic for connected devices. Having good software security is essential to reduce the risk of remote network-based attacks but IoT devices can often be physically accessed. They may also have other constraints such as limited CPU and memory resources or power requirements. There may even be situations where the main software environment cannot be trusted. In these cases, hardware security can really help. It can be used to prevent reverse engineering or offload computationally expensive operations. It can also help to isolate software. This short course will show how embedded security can be improved through the use of on-board and on-chip security hardware features and how these can be controlled by software.

This track is taught by Dr Carl Shaw, Director (Security Consultancy), MathEmbedded.

Doulos partners with MathEmbedded for training solutions in the Secure Embedded domain.

SPEAKER:
Carl Shaw - *MathEmbedded Ltd., United Kingdom*

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TRACK 4, PART I: TAKING YOUR C++ TO THE NEXT LEVEL

Time: 10:15am - 1:15pm || Room: 10AB || Event Type: Thursday is Training Day || Track: EDA, IoT
Topic Area: General Interest, System Software

ORGANIZER:
John Croix - *Cadence Design Systems, Inc., Austin, TX*

Writing robust, high-performance applications in C++ is about more than just converting algorithms from pseudo-code into C++ source files, compiling them, and linking them together. Application development involves specific, intricate knowledge of the language syntax itself, proper use of template libraries, unit testing methodologies and tools, knowledge of linker idiosyncrasies, shared-object library development, and, yes, cool ways to exploit C++ language features. The topics discussed at this session are directly applicable to all C++ applications, and attendees will leave with a better understanding of how to improve their own code, whether their applications are EDA related or not.

This DAC tutorial will focus on specific aspects of application development in C++, with presentations by C++ experts from Rackspace and NVIDIA. The session will cover generic C++ library development, unit test development, and linker/loader complexities. If time permits, a short Q&A with the presenters will follow.

SPEAKERS:

Jason Cohen - *NVIDIA Corp, Austin, TX*
Zach Laine - *NVIDIA Corp, Austin, TX*
Tim Simpson - *Rackspace US, Inc., Austin, TX*

THURSDAY IS TRAINING DAY

TRACK 5, PART I: FINDING CREATIVE SOLUTIONS TO COMPLEX PROBLEMS

Time: 10:15am - 1:15pm || Room: 9C || Event Type: Thursday is Training Day || Track: Design
Topic Area: General Interest

Elegant solutions may appear obvious in hindsight, but are difficult to identify in the moment. During this interactive session we'll learn very practical strategies for discovering creative solutions. Individual problem solving methods and tactics will be explored, along with ways to overcome barriers to innovative thinking. We then learn ways to approach interpersonal issues, emphasizing techniques for promoting collaboration and overcoming the emotional and psychological barriers of conflict. Finally, you'll learn ways to better manage and solve problems as a member of a team or group. Going beyond brainstorming, we'll explore tactics to harness the creative energy of the group while avoiding "analysis paralysis" and the dreaded "groupthink".

SPEAKER:
Gaylen Paulson - *Univ. of Texas at Austin, TX*

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TRACK 1, PART II: LEARN UVM USING THE EASIER UVM CODING GUIDELINES AND CODE GENERATOR

Time: 2:15pm - 5:15pm || Room: Ballroom E || Event Type: Thursday is Training Day
Track: EDA || Topic Area: Test & Verification

This session will teach the basics of UVM, the Universal Verification Methodology for SystemVerilog, by taking advantage of Doulos' Easier™ UVM Coding Guidelines and Code Generator. All the main concepts of UVM will be taught using working code examples. By running the Easier™ UVM Code Generator on the EDA Playground website, delegates will be able to run UVM examples immediately, experiment with what they have learned, and share their examples with others after the class.

The session is aimed at hands-on engineers who want to start writing UVM code themselves and are looking for some specific advice on the best place to start, the right UVM features and coding idiom to use, and the pitfalls to avoid.

This track is taught by Doulos CTO John Aynsley, winner of the Accellera Systems Initiative 2012 Technical Excellence Award for his contribution to the development of language standards.

SPEAKER:
John Aynsley - *Doulos, Ringwood, United Kingdom*

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TRACK 2, PART II: THE DEFINITIVE GUIDE TO SYSTEMC TLM-2.0: LEARN THE TECHNOLOGY STANDARD THAT UNDERPINS VIRTUAL PLATFORMS

Time: 2:15pm - 5:15pm || Room: Ballroom F || Event Type: Thursday is Training Day || Track: EDA
Topic Area: System Architectures & SoC, Codesign & System Design

Following its launch back in 2008, the SystemC TLM-2.0 standard quickly became the dominant standard for integrating transaction-level models in the context of building virtual platforms for architectural exploration and software development. TLM-2.0, which is now part of the IEEE 1666-2011 SystemC standard, standardizes a set of modeling mechanisms that allow transaction level models from different sources to be interoperable and yet to run at the fast execution speeds necessary to build a virtual platform for software development.

This session will introduce the main concepts of both SystemC and TLM-2.0, and will explain the tricks that allow TLM-2.0 to maintain speed and interoperability in the context of virtual platform modeling. The features of the standard will be demonstrated using working code examples, which delegates can run immediately on the EDA Playground website and will be available to use and share after the class.

This track is taught by David C. Black, Doulos Senior Member Technical Staff, who is co-author of the book, "SystemC: From the Ground Up."

SPEAKER:
David Black - *Doulos, Austin, TX*

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THURSDAY IS TRAINING DAY

TRACK 3, PART II: INTRODUCTION TO EMBEDDED LINUX SECURITY: KEYS TO UNDERSTANDING VULNERABILITIES IN EMBEDDED SYSTEMS AND HOW TO SECURE THEM

Time: 2:15pm - 5:15pm || Room: Ballroom G || Event Type: Thursday is Training Day
Track: Embedded Systems, Security || Topic Area: System Software, General Interest

Linux is being used in an increasing number of embedded devices including smart building and energy devices, set-top-boxes, automotive in-vehicle infotainment, Wi-Fi routers and home gateways, smart meters, industrial monitoring equipment and even domestic white goods.

Increasingly these devices are being connected to networks and this can leave them vulnerable to remote attacks that can result in brand damage, financial liabilities, product returns and even safety issues.

"Hardening" Linux systems to make them more resistant to attack is possible and is something that should be performed for every connected product. This introductory seminar introduces embedded systems developers to the techniques of how to identify vulnerabilities and begins to show ways in which the systems can be secured.

This track is taught by Adrian Thomasset, Senior Member Technical Staff, Doulos.

SPEAKER:
Adrian Thomasset - *Doulos, United Kingdom*

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TRACK 4, PART II: TAKING YOUR C++ TO THE NEXT LEVEL

Time: 2:15pm - 5:15pm || Room: 10AB || Event Type: Thursday is Training Day || Track: EDA, IoT
Topic Area: General Interest, System Software

ORGANIZER:
John Croix - *Cadence Design Systems, Inc., Austin, TX*

Writing robust, high-performance applications in C++ is about more than just converting algorithms from pseudo-code into C++ source files, compiling them, and linking them together. Application development involves specific, intricate knowledge of the language syntax itself, proper use of template libraries, unit testing methodologies and tools, knowledge of linker idiosyncrasies, shared-object library development, and, yes, cool ways to exploit C++ language features. The topics discussed at this session are directly applicable to all C++ applications, and attendees will leave with a better understanding of how to improve their own code, whether their applications are EDA related or not.

This DAC tutorial will focus on specific aspects of application development in C++, with presentations by C++ experts from NVIDIA and AMD.The session presents generic (template) programming techniques and the use of type erasure to solve classic object-oriented programming problems. After the two presentations, a detailed Q&A session, with speakers from parts I and II of the tutorial, will be held. Attendees can ask questions about any of the presentations or ask about aspects of the C++ programming language itself.

SPEAKERS:
Paul Fultz II - *Advanced Micro Devices, Inc., Austin, TX*
Zach Laine - *NVIDIA Corp, Austin, TX*

TRACK 5, PART II: MAXIMIZING MENTAL AGILITY

Time: 2:15pm - 5:15pm || Room: 9C || Event Type: Thursday is Training Day || Track: Design
Topic Area: General Interest

This program will train participants to develop six mental strategies to improve efficiency, creativity, motivation and job satisfaction. This program highlights the six facets of human thought that are simultaneously hidden and obvious, and easy-to-learn techniques that will help employees to be more productive, efficient, creative, motivated and satisfied in their work and personal lives. The techniques are presented in a fast-paced, interactive format that combines presented material with situational team-based learning modules, designed to transition the concepts into the participant's everyday thinking.

SPEAKER:
Art Markman - *Univ. of Texas at Austin, TX*

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COLOCATED CONFERENCES

ACM/IEEE INTERNATIONAL WORKSHOP ON SYSTEM LEVEL INTERCONNECT PREDICTION (SLIP) 2016

Date: Saturday, June 4 || Time: 8:00am - 5:30pm || Room: 12AB || Event Type: Colocated Conference
Track: EDA, Design || Topic Area: NoC & On-Chip Interconnects, Physical Design, System Architectures & SoC

ORGANIZERS:

Baris Taskin - *Drexel Univ., Philadelphia, PA*
Tsung-Yi Ho - *National Cheng Kung Univ., Tainan City, Taiwan*
Cheng Zhuo - *Intel Corp., Hillsboro, OR*
Emre Salman - *Stony Brook Univ., Stony Brook, NY*
Ioannis Savidis - *Drexel Univ., Philadelphia, PA*
Swaroop Ghosh - *Univ. of South Florida, Tampa, FL*
Amlan Ganguly - *Rochester Institute of Technology, Rochester, NY*

The general technical scope of the workshop is the design, analysis, prediction, and optimization of interconnect and communication fabrics in electronic systems. The organizing committee invites original contributions to the workshop. These contributions include papers, tutorials, panels, special sessions, and posters. We accept papers based on novelty and contributions to the advancement of the field. The accepted papers will be published in the ACM and IEEE digital libraries.

Technical topics include but are not limited to:

1. Interconnect prediction and optimization at various IC and system design stages
2. System-level design for FPGAs, NOCs and reconfigurable systems
3. Design, analysis, and optimization of power and clock networks
4. Interconnect reliability
5. Interconnect topologies and fabrics of multi- and many-core architectures
6. Design-for-manufacturing (DFM) and yield techniques for interconnects
7. High speed chip-to-chip interconnect design
8. Design and analysis of chip-package interfaces
9. Power consumption of interconnects
10. 3D interconnect design and prediction
11. Emerging interconnect technologies
12. Applications of interconnects to social, genetic, and biological systems
13. Co-optimization of interconnect technology and chip design

SLIP includes keynotes, regular paper sessions, interactive panels, tutorials, invited talks, and interactive poster sessions. Our program also includes lunch, refreshments, and a traditional social dinner with fun elements.

SPEAKERS:

Kaushik Roy - *Purdue Univ., West Lafayette, IN*
Saverio Fazzari - *Booz Allen Hamilton, Inc., Arlington, VA*
Swarup Bhunia - *Univ. of Florida, Gainesville, FL*
Sanu Mathew - *Intel Corp., Hillsboro, OR*

IEEE computer society www.SLIRonline.org acm TCVLSI VLSI

EMBEDDED TECHCON

Date: Tuesday, June 7 - Wednesday, June 8 || Time: 10:15am - 5:00pm || Room: 13AB & 14
Event Type: Colocated Conference || Track: Embedded Systems, IoT
Topic Area: Emerging Technologies, System Architectures & SoC, System Software

ORGANIZER:

Richard Nass - *OpenSystems Media, LLC, Fountain Hills, AZ*

Tuesday, June 7: 10:15am - 5:00pm

Wednesday, June 8: 10:15am - 5:00pm

Embedded TechCon, designed to educate today's design engineers in the most critical embedded product and technologies, will be held at the Austin Convention Center in Austin, Texas, on June 7th-8th, 2016. The live event extends OpenSystems Media's current on-line educational program, known as Embedded University.

The classes, which will be taught by leading industry experts, will cover key embedded topics like IoT, automotive, and security, while drawing from the industry's roots with topics like firmware development, debugging, and open-source hardware and software.

Embedded TechCon differentiates itself from other industry technical conferences by adhering to its "everything practical, nothing theoretical" theme. As such, designers will be trained by industry experts, often on equipment that's theirs to keep.

Embedded TechCon

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The **ACM Special Interest Group on Design Automation** specializes in applications of computing to all phases of the electrical and electronics design fields, including techniques, algorithms, and computer programs for computer-aided design and testing systems, structure and software. **www.acm.org/sigda**

Membership Options	Professional		Student
ACM Membership	❑ ~~$99~~	$84*	❑ $19
SIGDA Membership	❑ $25		❑ $15
ACM Membership + ACM Digital Library Subscription	❑ ~~$198~~	$168*	❑ $42

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PROMO CODE: CONF

CELUG/ESD ALLIANCE ENTERPRISE LICENSING CONFERENCE

Date: Tuesday, June 7 - Thursday, June 9 || Time: 9:00am - 5:00pm || Room: 9AB
Event Type: Colocated Conference || Track: EDA || Topic Area: General Interest

ORGANIZER:

Derek Magill - *Qualcomm, Inc., Austin, TX*

Tuesday, June 7 - 9:00am - 5:00pm
Wednesday, June 8 - 9:00am - 5:00pm
Thursday, June 9 - 9:00am - 12:00pm

EDA Licensing providers, ISVs, and Enterprise Customers will come together at an event colocated with the 53rd ACM/ESD Alliance/IEEE Design Automation Conference (DAC), June 5-9, 2016, at the Austin Convention Center in Austin, Texas.

CELUG (Centralized Enterprise Licensing Users Group) and the Electronic System Design (ESD) Alliance are co-hosting this three-day event colocated at DAC 2016.

This interactive event will focus on Enterprise Licensing, with presentations and panels addressing current and future challenges to making high technology tools and users more productive. This colocated event will bring Licensing Solution Providers and Independent Software Vendors together with Enterprise Customers from key industries for interactive, face-to-face meetings.

CELUG Centralized Enterprise Licensing User Group

ANNUAL IBM PLATFORM LSF TECHNICAL SEMINAR

Date: Wednesday, June 8 || Time: 11:30am - 5:00pm || Room: 10AB || Event Type: Colocated Conference
Track: EDA, Design || Topic Area: System Software, Modeling, Simulation & Timing, Business

ORGANIZER:

Peter Basmajian - *IBM Systems and Technology Group, Foster City, CA*

Join us at the IBM Platform LSF User Group during the Design Automation Conference (DAC).

You are invited to a complimentary seminar sponsored by IBM.

Learn new ways to accelerate time to results and lower costs with a scalable, efficient environment using IBM Platform Computing solutions.

High performance computing (HPC) technologies are evolving in exciting new ways. Businesses that can harness these advancements in resource, cluster management, and intelligent workload scheduling can gain competitive advantage as never before possible.

Who should attend?
IBM invites the following IT and technical professionals to our annual conference:
EDA and CAD/CAE Engineers
IT Directors and Managers
HPC and LSF Administrators
Academic Researchers

What You'll Learn:
Join us to hear about the new release of the IBM Platform LSF family. We will take a deep dive and show you how we've improved performance, manageability and ease of use. Learn how these latest innovations deliver tangible business value.

Join us for this annual opportunity to hear from the experts!
IBM product managers and developers will discuss the IBM Platform Computing product strategy and direction.

Annual IBM SDI and Platform LSF User Group
Austin Convention Center
Austin, TX

Agenda:
11:30-11:55am: Registration
11:55am-12:00pm: Welcome and Introduction
12:00-12:30pm: IBM Platform Computing Strategy & Portfolio Overview
12:30-1:25pm: Introducing IBM Platform LSF 10.1
1:30-2:00pm: Client Case Study Presentation
2:00-2:30pm: Break
2:30-4:00pm: Deep Dive Sessions: Optimizing Software Licenses with RTM & License Scheduler and Using LSF's Host Factory with OpenStack
4:00-4:30pm: Q&A and Closing Remarks

IBM

IWLS - INTERNATIONAL WORKSHOP ON LOGIC AND SYNTHESIS

Date: Friday, June 10 - Saturday, June 11 || Time: 8:00am - 9:00pm || Room: Thompson Conference Center
Event Type: Colocated Conference || Track: EDA, Design || Topic Area: Logic & High-Level Synthesis, Physical Design, Emerging Technologies

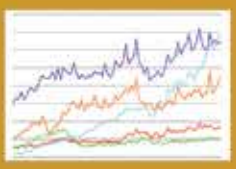
The International Workshop on Logic and Synthesis is the premier forum for research in synthesis, optimization, and verification of integrated circuits. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged. The workshop accepts complete papers as well as abstracts, highlighting important new problems in the early stages of development, without providing complete solutions. The emphasis is on novelty and intellectual rigor.

Topics of interest include (but are not limited to): synthesis and optimization; power and timing analysis; testing, validation and verification; architectures and compilation; and design experiences. Papers on the interaction of logic synthesis with front-end or back-end design steps are welcome, specially when considering the impact in the design flow. Submissions on modeling, analysis and synthesis for emerging technologies are also encouraged

international workshop on logic & synthesis IWLS

Electronic System Design Alliance™

Representing the semiconductor design ecosystem.

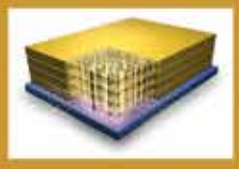


JOIN US!

The *Electronic System Design Alliance* provides a platform for member companies to address technical, marketing, economic and legislative issues affecting the entire industry. We also provide networking events and targeted programs to assist emerging companies in the design ecosystem.

ESD Alliance committees and working groups focus on critical issues that affect the design ecosystem including -- Export Regulations, License Management & Anti-Piracy, Market Statistics Service, O/S Interoperability, Emerging Companies, and Trade Shows.

NEW!



Check out our new committees and working groups:

IP Fingerprinting

This working group is bringing together IP vendors and users to develop a common methodology and best practices for IP fingerprinting -- a technology that provides a solution to efficient IP auditing.

Advanced Packaging

Bringing together manufacturers and designers to enable the widespread use of system scaling technologies such as 3D-IC and other multi-die approaches.

Embedded Software

Chip designers and embedded software designers working to develop best practices and methodologies for implementing the hardware and software interface.

Join the Electronic System Design Alliance

For more information about the benefits of membership, visit esd-alliance.org or email us at info@esd-alliance.org.

ADDITIONAL MEETINGS

A. RICHARD NEWTON YOUNG FELLOW PROGRAM WELCOME BREAKFAST & ORIENTATION

Date: Sunday, June 5 || Time: 7:30am - 9:00am || Room: 18CD || Event Type: Additional Meeting
Track: EDA || Topic Area: General Interest

The Newton Young Fellow Program is designed to assist young students at the beginning of a career in Electronic Design Automation and Embedded Systems. Each Newton Young Fellow will actively engage in DAC through a number of events including meetings with design automation luminaries, attendance at technical sessions and exhibits, participation in student-related events at DAC.

In addition, Newton Young Fellows will participate in a welcome orientation breakfast on Sunday morning, attend the Design Automation Summer School program, present posters of their academic/research work on Tuesday evening (colocated with the SIGDA Ph.D. Forum), and participate in a closing award ceremony for Young Fellows on Thursday evening.

Following a 50-year tradition, DAC strives to foster a vibrant and worldwide community of electronic design and embedded systems professionals; the fellowship actively supports and attempts to build an active cohort of the next generation of EDA and Embedded Systems professionals.

Welcome Breakfast and Orientation
Sunday, June 5
7:30 - 9:00am
Room: 18CD

Poster Presentation (colocated with the Ph.D. Forum)
Tuesday, June 7
7:00 - 9:00pm
Ballroom D

Closing Session and Award Ceremony
Thursday, June 9
6:00 - 6:45pm
Room: 12AB

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YOUNG FACULTY WORKSHOP

Date: Sunday, June 5 || Time: 8:30am - 7:00pm || Room: 12AB || Event Type: Additional Meeting
Track: Design, EDA || Topic Area: General Interest

ORGANIZERS:

Jinjun Xiong - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Eli Bozorgzadeh - *Univ. of California, Irvine, CA*
Soha Hassoun - *Tufts Univ., Medford, MA*
(In Memory) Steve Levitan - *Univ. of Pittsburgh, PA*
Patrick Haspel - *Cadence Design Systems, Inc.*
Michael Huebner - *Ruhr Univ. Bochum*

This is a special workshop organized for current, or soon to be, young faculty in the field of electronic design automation (EDA).

The workshop will be organized as presentations by EDA senior professionals, with additional opportunities to network with some of the established researchers and funding officers in the field of EDA. The themes this year include: Getting an Academic Job, Research - papers, conferences and grants, The NSF proposal process for CAREER and other programs, Teaching - Best practices, Special Issues, University programs in EDA industries, and a “Speed Networking” lunch event.

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Conferences

ASP-DAC, CANDE, DAC, DATE, ESWEEK, ETS, FMCAD, ICCAD, IOLTS, MEMOCODE, MPSoC, NOCS, PATMOS, VLSI-SoC, WF-IoT, and many other technically sponsored events.

Publications

IEEE Transactions on Computer-Aided Design (*TCAD*), *IEEE Design & Test* (*D&T*), *IEEE Embedded Systems Letters*, and *CEDA Currents*.

Awards

CEDA honors innovative and substantial technical contributions to EDA, best published papers, or contributions during the early stages of one's research career.

IEEE CEDA

The only place for EDA and embedded systems professionals, researchers, and students to come together and discover new technologies that are advancing the state of the art!

CEDA is a nonprofit entity that provides a platform for dissemination of ideas, community feedback, and individual recognition through its various awards, publications, and conferences.

Visit us at http://ieee-ceda.org.

Join the CEDA mailing list for our Ad-Free Quarterly Newsletter, *CEDA Currents*, on major news regarding the profession and CEDA. To join, just send an (empty) email to **ceda-subscribe@listes.epfl.ch**.

CEDA is willing to support any EDA-related activities.
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WE ARE ALWAYS OPEN TO IDEAS!

DESIGN AUTOMATION SUMMER SCHOOL

Date: Sunday, June 5 || Time: 9:00am - 6:00pm || Room: 18CD || Event Type: Additional Meeting
Track: IoT, Security || Topic Area: Codesign & System Design, Cyber-Physical Systems, Emerging Technologies

he Design Automation Summer School (DASS) is a one-day intensive course on research and development in design automation (DA). Each topic in this course will be covered by a distinguished speaker who will define the topic, describe recent accomplishments, and indicate remaining challenges. This program is intended to introduce and outline emerging challenges, and to foster creative thinking in the next generation of EDA engineers.

The 2016 SIGDA Design Automation Summer School is co-hosted by A. Richard Newton Young Fellowship Program at DAC. All the students receiving the fellowship (excluding the mentors) are required to attend DASS event. For additional details go to: http://www.sigda.org/dass

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GARY SMITH EDA AT ESD ALLIANCE KICKOFF SUNDAY NIGHT

Date: Sunday, June 5 || Time: 5:00pm - 5:30pm || Room: Ballroom D || Event Type: Additional Meeting
Track: EDA || Topic Area: General Interest

Laurie Balch kicks off the annual ESD Alliance reception.

Come hear the 27th annual update on the state of EDA by Laurie of Gary Smith EDA.

“Extending the Bounds of EDA”
Laurie Balch

This year’s talk will focus on the challenges and opportunities facing EDA vendors, including a view of the annual EDA forecast.

Where will the industry need to expand and how can it best address the needs of electronic product developers? How will future engineering requirements impact the EDA landscape? What are the growth prospects for EDA vendors?

DAC reception immediately follows.

SPEAKER:

Laurie Balch - *Gary Smith EDA, Santa Clara, CA*

CEDA CAREER PERSPECTIVES PANEL

Date: Sunday, June 5 || Time: 7:00pm - 9:00pm || Room: Ballroom D || Event Type: Additional Meeting
Track: EDA || Topic Area: General Interest

ORGANIZERS:

Soha Hassoun - *Tufts Univ., Medford, MA*
Peng Li - *Texas A&M Univ., College Station, TX*
Kevin Nesmith - *EDDR Software, LLC, TX*
Rasit Topaloglu - *IBM Corp., Poughkeepsie, NY*

Millennials with an EDA background face an abundance of career choices. Which one fits best: Join a large company? Stay in academia? Join a hip startup? Become a consultant? Making a conscious career choice is certainly not easy. The panelist of this session come from different EDA-related jobs and are in different phases of their careers. They will provide a glimpse into their worlds and lifestyles: what do they like and dislike? What is the compensation? How is the work-life balance? Any regrets? These unique insights will help the next generation in deciding on a career path.

PANELISTS:

Zaher Andraus - *Reveal Design Automation, Detroit, Michigan*
Pranavi Chandupatla - *ARM, Austin, TX*
Zhuo Li -*Cadence Design Systems, Inc., Austin, TX*
Bei Yu - *CSE Dept., Chinese Univ. of Hong Kong*

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VARIATION-AWARE DESIGN AT ADVANCED AND LOW-POWER PROCESSES

Date: Monday, June 6 || Time: 10:30am - 11:30am || Room: 9BC || Event Type: Additional Meeting
Track: EDA, Design || Topic Area: Circuit Design, Low-Power & Reliability, Modeling, Simulation & Timing

Variation effects have an ever greater impact on low-power, low-voltage processes and advanced FinFET/FDSOI nodes; at each, new sources of variation must be considered. Furthermore, increased competition is forcing tighter design margins to make high-performance, low-power, low-cost products. Designers must do more variation analysis than ever to achieve these tighter margins, using advanced variation-aware technology for speed, accuracy and coverage to deliver competitive chips on schedule.

The panel discussion will focus on recent, highly effective ways to address variation-aware design for Memory, Analog/RF and Standard Cell design. The methodologies will include high-sigma Monte Carlo, PVT, statistical PVT, and hierarchical Monte Carlo.

Opening by Amit Gupta (CEO, Solido) on custom IC design market data.

PANELISTS:

Azeez Bhavnagarwala - *ARM, Inc., San Jose, CA*
Glen Wiedemeier - *IBM Corp., Austin, TX*
Jeff Dyck - *Solido Design Automation, Inc., Saskatoon, Canada*

DESIGN, AUTOMATION AND TEST IN EUROPE

DATE 17

27—31 MARCH, 2017

The european event for electronic system design & test

SWISSTECH, LAUSANNE, SWITZERLAND

DATE 2017 — CALL FOR PAPERS

Scope of the Event

The 20th DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. It puts strong emphasis on both ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.

Structure of the Event

The five-day event consists of a conference with plenary invited papers, regular papers, panels, hot-topic sessions, tutorials, workshops, two special focus days and a track for executives. The scientific conference is complemented by a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms, embedded software, and (industrial) design experiences from different application domains, such as automotive, wireless, telecom and multimedia applications. The organization of user group meetings, fringe meetings, a university booth, a PhD forum, vendor presentations and social events offers a wide variety of extra opportunities to meet and exchange information on relevant issues for the design and test community. Special space will also be allocated for EU-funded projects to show their results. More details are given on the DATE website (www.date-conference.com).

Areas of Interest

Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, CAD languages, algorithms and tools, testing of electronic circuits and systems, embedded software, applications design and industrial design experiences. Topics of interest include, but are not restricted to:

- System Specification and Modeling
- System Design, Synthesis and Optimization
- Simulation and Validation
- Design of Low Power Systems
- Temperature-Aware Design
- Power Estimation and Optimization
- Temperature Modeling and Management
- Emerging Technologies, Systems and Applications
- Formal Methods and Verification
- Network on Chip
- Architectural and Microarchitectural Design
- Architectural and High-Level Synthesis
- Reconfigurable Computing
- Logic and Technology Dependent Synthesis for Deep-Submicron Circuits
- Physical Design and Verification
- Analogue and Mixed-Signal Circuits and Systems
- Interconnect, EMC, EMD and Packaging Modeling
- Multiprocessor System-on-Chip and Computing Systems
- Communication, Consumer and Multimedia Systems
- Transportation Systems
- Medical, Healthcare and Assistive Technology Systems
- Energy Generation, Recovery and Management Systems
- Secure, Dependable and Adaptive Systems
- Test for Defects, Variability, and Reliability
- Test Generation, Simulation and Diagnosis
- Test for Mixed-Signal, Analog, RF, MEMS
- Test Access, Design-for-Test, Test Compression, System Test
- On-Line Testing and Fault Tolerance
- Real-time, Networked and Dependable Systems
- Compilers and Code Generation for Embedded Systems; Software-centric System Design Exploration
- Model-based Design and Verification for Embedded Systems
- Embedded Software Architectures and Principles; Software for MPSoC, Multi/many-core and GPU-based Systems

Submission of Papers

All papers have to be submitted electronically by Sunday September 11, 2016 via: **www.date-conference.com**

Papers can be submitted either for standard oral presentation or for interactive presentation. **The Programme Committee also encourages proposals for Special Sessions, Tutorials, Friday Workshops, University Booth, PhD Forum and Exhibition Theatre.**

Event Secretariat

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LIRMM, Montpellier, France
giorgio.dinatale@lirmm.fr

SYNOPSYS LUNCH: ROBUST AMS DESIGN VERIFICATION AT ADVANCED NODES

Date: Monday, June 6 || Time: 11:30am - 1:30pm || Room: Hilton Hotel, 6th floor, Austin Grand Ballroom G
Event Type: Additional Meeting || Track: EDA || Topic Area: Test & Verification

Industry leaders will discuss their design verification challenges that stem from cutting-edge FinFET technologies and increasing design complexity in memory, analog, and mixed-signal applications, and how they overcome such challenges by using Synopsys AMS circuit simulation solutions to ensure design robustness.

SYNOPSYS IC COMPILER II LUNCH: ACHIEVING INDUSTRY-BEST QOR ON ADVANCED DESIGNS

Date: Monday, June 6 || Time: 11:30am - 1:30pm || Room: Hilton Hotel, 6th floor, Austin Grand Ballroom H
Event Type: Additional Meeting || Track: EDA || Topic Area: Physical Design

Are you on IC Compiler II yet? Hear how industry leaders are achieving success with their advanced designs using IC Compiler II.

Leading customers will share their experiences using IC Compiler II technology to address physical design challenges and accelerate products to market.

WRITING A GOOD TECHNICAL PAPER - THE DO'S AND DONT'S

Date: Monday, June 6 || Time: 1:30pm - 3:00pm || Room: 18AB || Event Type: Additional Meeting
Track: EDA || Topic Area: General Interest

ORGANIZERS:

Helmut Graeb - *Technische Univ. München, Germany*
Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

I will share my experiences as an author, reviewer and editor on how to write a good technical paper.

The topics addressed will include how to decide an appropriate publication outlet, whether a work is ready for publication, presentation skills, writing rebuttals to reviewers, and in strengthening the technical message.

SPEAKER:

Vijaykrishnan Narayanan - *Pennsylvania State Univ., State College, PA*

LOW-POWER IMAGE RECOGNITION CHALLENGE (LPRIC) AWARDS PRESENTATION

Date: Monday, June 6 || Time: 3:00pm - 3:15pm || Room: DAC Pavilion - Booth 1839
Event Type: Additional Meeting || Track: EDA, Design || Topic Area: Business, General Interest, Emerging Technologies

LPRIC will announce the winners of the competition that was held on Sunday, June 5.

For more information, please go to http://lpirc.net/index.html

COOLEY'S DAC TROUBLEMAKER PANEL

Date: Monday, June 6 || Time: 3:00pm - 4:00pm || Room: 9BC || Event Type: Additional Meeting
Track: EDA, Design || Topic Area: Business, General Interest, Emerging Technologies

MODERATOR:

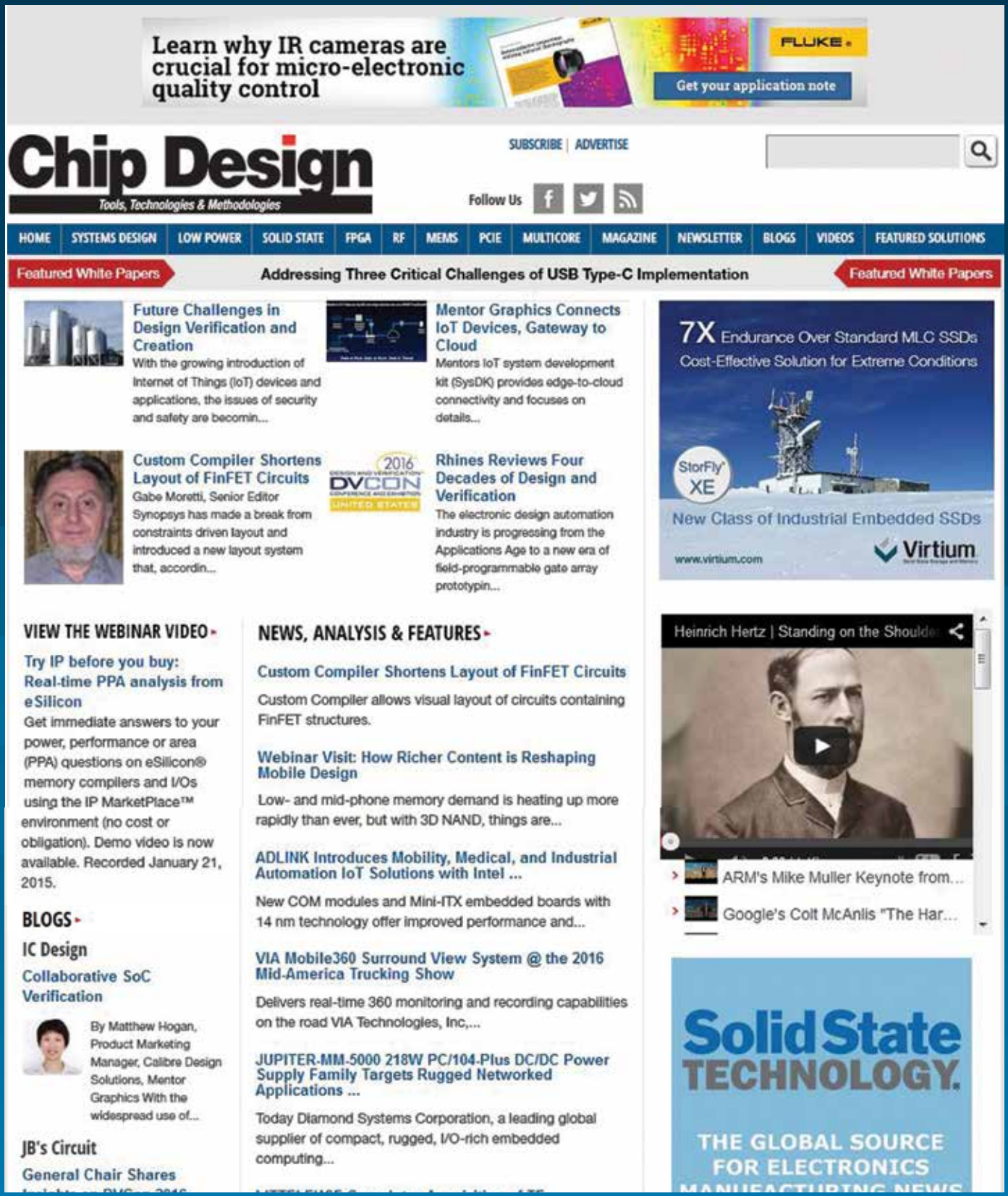
John Cooley - *Deepchip*

Come watch the EDA troublemakers answer the edgy, user-submitted questions about this year's most controversial issues! It's an old style open Q&A from the days before corporate marketing took over every aspect of EDA company images.

PANELISTS:

Joe Sawicki - *Mentor Graphics Corp.*
Anirudh Devgan - *Cadence Design Systems, Inc.*
Dean Drako - *IC Manage, Inc.*
Amit Gupta - *Solido Design Automation, Inc.,*
Raik Brinkmann - *OneSpin Solutions GmbH*
Jim Hogan - *Vista Ventures*

Keep Current With the Advanced IC Design Market



Visit www.ChipDesignMag.com

SYNOPSYS PRIMETIME SIG DINNER: WORK SMARTER WITH ADVANCED SIGNOFF TECHNOLOGY

Date: Monday, June 6 || Time: 7:00pm - 9:00pm || Room: Brazos Hall, 204 E 4th Street
Event Type: Additional Meeting || Track: EDA || Topic Area: General Interest

Synopsys hosts an annual event for the PrimeTime Special Interest Group at DAC, providing an opportunity for users to stay connected with the latest developments in timing analysis. We are pleased to host this PrimeTime SIG event at DAC 2016.

This year, Synopsys will unveil revolutionary technologies that help designers work smarter and improve productivity and design quality.

SYNOPSYS AND SAMSUNG BREAKFAST: READY TO DESIGN! SYNOPSYS AND SAMSUNG FOUNDRY 10NM ENABLEMENT SOLUTIONS FOR CUSTOMER TAPEOUT SUCCESS

Date: Tuesday, June 7 || Time: 7:15am - 8:45am || Room: Hilton Hotel, 6th floor, Austin Grand Ballroom G
Event Type: Additional Meeting || Track: EDA, Design || Topic Area: System Architectures & SoC, Emerging Technologies

Attend this breakfast panel to learn how Samsung and Synopsys are enabling Samsung Foundry's 10nm FinFET technology to meet the added functionality needs of advanced SoC designs.

Visit dac2016.synopsys.com for more information and to register.

UVM: THE NEXT 5 YEARS

Date: Tuesday, June 7 || Time: 7:30am - 9:00am || Room: 9C || Event Type: Additional Meeting
Topic Area: General Interest

UVM, the Universal Verification Methodology, is used by thousands of engineers worldwide in nearly all digital verification flows. Today, the IEEE P1800.2 committee is diligently working to standardize UVM. But what's next for UVM? Future possibilities include UVM multi-language, UVM for mixed-signal, and UVM for acceleration. Accellera is also in the late stages of bringing a native SystemC implementation of UVM to the community.

Please join us and our panel of experts for breakfast as we discuss the future of UVM and the challenges the industry is facing. We will also have an update by Accellera Chair Shishpal Rawat and the presentation of the Accellera Leadership Award. Event is free but registration at www.accellera.org is required.

SYNOPSYS CUSTOM COMPILER LUNCH: CUTTING LAYOUT TASKS FROM DAYS TO HOURS

Date: Tuesday, June 7 || Time: 11:30am - 1:30pm || Room: Hilton Hotel, 6th floor, Austin Grand Ballroom G
Event Type: Additional Meeting || Track: EDA, Design || Topic Area: System Software

FinFET devices have added significant complexity to the design flow, and many companies are seeking new solutions for custom design. Custom Compiler's pioneering visually-assisted automation can cut layout tasks from days to hours.

Join us to hear users discuss their experiences with FinFET custom design challenges and how they have deployed Custom Compiler to improve their custom design productivity for both FinFET and established nodes.

SYNOPSYS LUNCH: SOC LEADERS VERIFY WITH SYNOPSYS

Date: Tuesday, June 7 || Time: 11:30am - 1:30pm || Room: Hilton Hotel, 6th floor, Austin Grand Ballroom H
Event Type: Additional Meeting || Track: EDA || Topic Area: Test & Verification

Synopsys will highlight next-generation verification technologies as well as discussions about the latest developments in the verification landscape and advanced technology trends.

In addition, a panel of industry experts will share their viewpoints on what is driving SoC complexity, how their teams have achieved success and how you can apply their insights on your next project.

IEEE CEDA LUNCHEON AND DISTINGUISHED LECTURE IN HONOR OF PROF. EDWARD J. MCCLUSKEY

Date: Tuesday, June 7 || Time: 12:00pm - 1:30pm || Room: Ballroom D || Event Type: Additional Meeting
Track: Design, EDA || Topic Area: Test & Verification, Logic & High-Level Synthesis

DISTINGUISHED SPEAKER:

Dr. Arvind Krishna - *Senior Vice President and Director, IBM Research*

Arvind Krishna is senior vice president and director, IBM Research. He is only the eleventh person to hold this position in the seven-decade history of the IBM Research labs. In this role, he helps guide the company's overall technical strategy, overseeing a global organization of approximately 3,000 scientists and technologists located at 12 labs on six continents.

Arvind was most recently general manager of IBM Systems and Technology Group's Development and Manufacturing organization, responsible for the advanced engineering and development of a full technology portfolio, ranging from advanced semiconductor materials to leading-edge microprocessors, servers and storage systems. His team developed Power 8, the industry's first processor designed for Big Data; introduced OpenPOWER; brought the world's fastest 22nm silicon process to the market; announced Software Defined Storage scaling to exabytes; and brought other innovations across Mainframe and Storage products to the marketplace.

He was previously general manager of IBM Information Management, which included database, information integration and Big Data software solutions. Over his years in Information Management, Arvind helped grow the division's revenue by roughly 50 percent through a mix of organic innovation and acquisition. Prior to that, he was vice president of strategy for IBM Software, where he identified more than 10 companies to acquire and led the integration of their operations into IBM. He has held several key technical roles in IBM Software and IBM Research, where he pioneered IBM's security software business.

Arvind has an undergraduate degree from the Indian Institute of Technology, Kanpur and a Ph.D. from the University of Illinois at Urbana-Champaign. He is the recipient of a distinguished alumni award from the University of Illinois, is the co-author of 15 patents, has been the editor of IEEE and ACM journals, and has published extensively in technical conferences and journals.

CEDA
IEEE Council on Electronic Design Automation

TRIBUTE SPEAKERS:

Dr. Bill Joyner - *Senior Science Director, Semiconductor Research Corporation*

Prof. Daniel P. Siewiorek - *Buhl University Professor of Electrical and Computer Engineering and Computer Science Carnegie Mellon University*

Dr. Tom Williams - *Synopsys Fellow (Retired)*

SYNOPSYS AND GLOBALFOUNDRIES DINNER: WHAT'S IMPORTANT FOR IOT—POWER, PERFORMANCE OR INTEGRATION...OR ALL OF THE ABOVE?

Date: Tuesday, June 7 || Time: 6:15pm - 8:15pm || Room: Hilton Hotel, 6th floor, Austin Grand Ballroom G
Event Type: Additional Meeting || Track: IoT, Design || Topic Area: Physical Design, Emerging Technologies, General Interest

Attend this dinner panel to learn how GLOBALFOUNDRIES and Synopsys together have built an integrated reference flow that provides body bias control for maximizing SoC energy efficiency and performance and, ultimately, end-product differentiation.

Visit dac2016.synopsys.com for more information and to register.

ACM SIGDA PH.D. FORUM

Date: Tuesday, June 7 || Time: 7:00pm - 9:00pm || Room: Ballroom D || Event Type: Additional Meeting
Track: EDA || Topic Area: General Interest

ORGANIZERS:

Swaroop Ghosh - *Univ. of South Florida*
Xin Li - *Carnegie Mellon Univ. (Past Chair)*
Yiyu Shi - *Univ. of Notre Dame*
Hai Li - *Univ. of Pittsburgh*

The Ph.D. Forum at the Design Automation Conference is a poster session hosted by ACM SIGDA for senior Ph.D. students to present and discuss their dissertation research with people in the EDA community.

Participation in the forum is highly competitive with acceptance rate of around 30%. The forum is open to all members of the design automation community and is free-of-charge.

For more information, please visit the ACM SIGDA Ph.D. Forum website.

28TH ACM SIGDA UNIVERSITY DEMONSTRATION

Date: Tuesday, June 7 || Time: 7:00pm - 9:00pm || Room: Ballroom D || Event Type: Additional Meeting
Track: EDA || Topic Area: General Interest

University Booth comes back to DAC this year after one year break with a new format and a new title: University Demonstration. This year marks the 28th University Demonstration at the Design Automation Conference. UD is an opportunity for university researchers to display their results and to interact with participants at DAC. Presenters and attendees at DAC are especially encouraged to participate, but participation is open to all members of the university community. The demonstrations include new EDA tools, EDA tool applications, design projects, and instructional materials.

For further details and videos from previous years please visit the ACM SIGDA University Booth site.

Booth Coordinators
Chair: Soonhoi Ha - Seoul National University, Korea
Vice Chair: Sudeep Pasricha - Colorado State Univ., Fort Collins, CO
Publicity Chair: Qi Zhu - Univ. of California, Riverside, CA

DECODING FORMAL TRAINING DAY: "ACHIEVING FORMAL SIGN-OFF"

Date: Thursday, June 9 || Time: 10:30am - 5:00pm || Room: Hilton Hotel, Austin
Event Type: Additional Meeting || Track: EDA, Design || Topic Area: Emerging Technologies, Modeling, Simulation & Timing, System Architectures & SoC

The Decoding Formal Training Day: "Achieving Formal Sign-off" is a one-day primer on select topics in Advanced Formal Verification, intended for those who are new to formal verification or want to learn more about the specific topic areas. This training day is a sampler of Oski's two-week Advanced Formal Training program.

Topics may include writing end-to-end formal checkers, handling formal complexity, using abstraction models, managing constraints efficiently, and using formal coverage. The day will be organized as a series of presentations, with opportunities for networking over breakfast, lunch and breaks. More information is available at www.oskitechnology.com.

A. RICHARD NEWTON YOUNG FELLOW PROGRAM CLOSING SESSION & AWARD CEREMONY

Date: Thursday, June 9 || Time: 6:00pm - 6:45pm || Room: 12AB || Event Type: Additional Meeting
Track: EDA || Topic Area: General Interest

The Newton Young Fellow Program is designed to assist young students at the beginning of a career in Electronic Design Automation and Embedded Systems. Each Newton Young Fellow will actively engage in DAC through a number of events including meetings with design automation luminaries, attendance at technical sessions and exhibits, participation in student-related events at DAC.

In addition, Newton Young Fellows will participate in a welcome orientation breakfast on Sunday morning, attend the Design Automation Summer School program, present posters of their academic/research work on Tuesday evening (colocated with the SIGDA Ph.D. Forum), and participate in a closing award ceremony for Young Fellows on Thursday evening.

Following a 50-year tradition, DAC strives to foster a vibrant and worldwide community of electronic design and embedded systems professionals; the fellowship actively supports and attempts to build an active cohort of the next generation of EDA and Embedded Systems professionals.

Visit us at booth #1226

EDACAFÉ

Visit EDACAFÉ at DAC 2016 in booth #1226, and be entered to win a Kindle Fire!

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Video interviews with key industry players.
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Detailed information about thousands of
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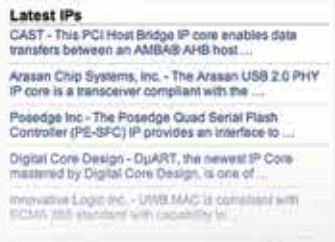

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DAC PAVILION - BOOTH 1839

EDA INDUSTRY TRENDS AND WHAT'S HOT AT DAC

Date: Monday, June 6 || Time: 10:30am - 11:00am || Room: DAC Pavilion - Booth 1839
Event Type: DAC Pavilion || Track: EDA, Design || Topic Area: General Interest

ORGANIZER:

Anne Cirkel - *Mentor Graphics Corp., Wilsonville, OR*

In longstanding Gary Smith EDA tradition, EDA chief analyst Laurie Balch of Gary Smith EDA will share her views on the latest directions for the EDA technology and business fronts. What new trends are facing the EDA, semiconductor and design communities and how will they impact you? What are the hot 'must see' products at this year's conference? How can you prepare for the future of electronics design? Plus, get a rundown of the annual Gary Smith EDA Sunday night kickoff talk.

SPEAKER:

Laurie Balch - *Gary Smith EDA, San Jose, CA*

UNSCRIPTED: AART DE GEUS

Date: Monday, June 6 || Time: 11:30am - 12:15pm || Room: DAC Pavilion - Booth 1839
Event Type: DAC Pavilion || Track: EDA, Design || Topic Area: General Interest

MODERATOR:

Ed Sperling - *Semiconductor Engineering, San Jose, CA*

ORGANIZER:

Kathryn Schmidt - *Synopsys, Inc., Mountain View, CA*

Synopsys' chairman and co-CEO talks with Semiconductor Engineering's Ed Sperling about Moore's Law, how designs are changing, the growing role of software, and where the money will be in the future.

SPEAKER:

Aart de Geus - *Synopsys, Inc., Mountain View, CA*

SKY TALK: WIRELESS IMPLANTABLE MICROSYSTEMS: MINIMALLY INVASIVE INTERFACES TO THE BRAIN

Time: 1:00pm - 1:30pm || Room: DAC Pavilion - Booth 1839 || Event Type: SKY Talk
Track: IoT, Embedded Systems || Topic Area: Circuit Design, Cyber-Physical Systems, Emerging Technologies

ORGANIZER:

Sharon Hu - *Univ. of Norte Dame, Norte Dame, IN*

Smart and connected medical implants are the next frontier in the Internet of Things (IoT) and are set to revolutionize healthcare. Advancing our ability to interface technology with biological environments will enable patients to be monitored and receive treatment at home, and in the long term, have chronically implanted electronic devices seamlessly integrate with their everyday lives. As an example, clinically viable and minimally invasive neural interfaces stand to transform disease care for patients of neurological conditions. Recently there has been an explosion of research in Brain-Machine Interfaces (BMI) that has shown incredible results in using electronic signals from the motor cortex of the brain to control artificial limbs, providing hope for patients with spinal cord injuries. A major impediment to clinical translation is that state-of-the-art clinical neural interfaces are large, wired and require open-skull operation which leaves the patient at risk of infection and unable to move. Future, less invasive interfaces with increased numbers of electrodes, signal processing, and wireless connectivity will enable advanced prosthetics, disease control and completely new user-computer interfaces.

Substantial improvements in neural implant longevity are needed to transition BMI systems from research labs to clinical practice. In this talk I will describe the development of a minimally invasive, wireless neural implant to enable chronic and stable neural recording. The implant is based on micro-electrocorticography (μECoG), an electrophysiological technique where electrical potentials are recorded from the surface of the cerebral cortex, reducing cortical scarring when compared with microelectrode recording techniques that pierce into the cortex. Wireless powering and readout are combined with a flexible, microfabricated antenna and electrode array with an ultra-low power integrated circuit. The low power consumption of the integrated circuit enables remote powering well below established IEEE and FCC safety limits, while the small size and flexibility of the implant minimizes the foreign body response. The improved implant safety and longevity gives wireless μECoG excellent prospects to become the technology of choice for clinically relevant neural interfaces in the foreseeable future.

SPEAKER:

Rikky Muller - *Univ. of California, Berkeley & Cortera Neurotechnologies, Berkeley, CA*

LANZA'S TECH VISION CHALLENGE: DARING TO MOVE TO OPEN SOURCE

Date: Monday, June 6 || Time: 2:00pm - 2:45pm || Room: DAC Pavilion - Booth 1839
Event Type: DAC Pavilion || Track: EDA, IP || Topic Area: General Interest

MODERATOR:

Lucio Lanza - *Lanza TechVentures, Palo Alto, CA*

ORGANIZER:

Michael "Mac" McNamara - *Adapt-IP, Palo Alto, CA*

The Semiconductor Industry is at a crossroads. The larger, consolidated semiconductor companies will continue to chase Moore's Law, delivering bigger, more complex chips with loads of functionality done at smaller process nodes, paying handsomely for design tools to enable first-silicon success, and winning the coveted key sockets. At the same time, the emerging Internet of Things market is destined to upend that time-tested "advanced-node" model, as developers opt for older, less costly process technologies, using commodity design tools and selecting proven IP blocks to quickly and efficiently assemble chips. As demand for IoT devices grows exponentially, might open source EDA tools and IP become viable, or even the winning combination that enables the low-cost design of an IoT SoC?

Join Lucio Lanza for a fireside chat on the pros and cons of a move to an open source EDA tools and IP design flow for the IoT SoC.

PANELISTS:

Warren Savage - *IPextreme, Campbell, CA*
Mark Templeton - *Scientific Ventures, LLC, Los Altos, CA*
Michael Wishart - *eFabless.com, San Jose, CA*

LET'S CONNECT EVERYTHING! BIG OPPORTUNITIES FOR LITTLE DEVICES

Date: Monday, June 6 || Time: 3:30pm - 4:00pm || Room: DAC Pavilion - Booth 1839
Event Type: DAC Pavilion || Track: IoT, Embedded Systems || Topic Area: Cyber-Physical Systems, System Software

ORGANIZER:

Patrick Groeneveld - *Synopsys, Inc., Mountain View, CA*

Industry analysts foresee astonishingly rapid expansion of IoT business opportunities between now and the end of the decade. This accelerated growth is fueled by technical progress in two areas. First, new generations of small, power efficient, network-capable SoCs enable integration of computing capabilities into the "things" all around us. Second, open industry standards bring secure, Internet-scale connectivity to all IoT platforms, including the smallest and most power constrained devices. Standardization enables independent development of hardware and software components across the entire IoT value-chain, thereby increasing innovation and reducing costs.

In this talk, we explore the key SoC features, industry standards, and software design patterns that enable the INTERNET of Things to reach its full potential.

SPEAKER:

Bill Curtis - *ARM Ltd., Austin, TX*

IFIXIT HOVERBOARD TEARDOWN

Date: Monday, June 6 || Time: 4:30pm - 5:00pm || Room: DAC Pavilion - Booth 1839
Event Type: DAC Pavilion || Track: Embedded Systems || Topic Area: General Interest

ORGANIZER:

Michelle Clancy - *Cayenne Communication, San Jose, CA*

Hoverboards are surely among the hottest tech toys around — also among the most controversial, given the numerous stories and videos featuring these gizmos catching fire. This unfortunate tendency was enough to get them banned by most major U.S. airlines. Since it wasn't an option to bring your hoverboard to Austin, you might be especially interested in checking out the teardown. Expect this to go way beyond kicking the tires. In fact the tires will surely come off during disassembly — the better for inspecting the motors. Also likely to be stripped out: the circuit board including the main microprocessor, and the various sensors and modules that help keep these things balanced, most of the time. (The Instagram video of Justin Bieber falling off his board has 1.1m likes.)

Stop by, if only to see how much space the battery takes up in a hoverboard chassis, and what's so flammable in there anyway.

SPEAKERS:

Andrew Goldberg - *iFixIt, San Luis Obispo, CA*
Sam Lionheart - *iFixIt, San Luis Obispo, CA*

SOLVING THE DESIGN COST PUZZLE: HOW IP FITS

Date: Tuesday, June 7 || Time: 10:30am - 11:00am || Room: DAC Pavilion - Booth 1839
Event Type: DAC Pavilion || Track: IP, EDA || Topic Area: General Interest, Business

ORGANIZER:

Bob Smith - *ESD Alliance, San Jose, CA*

ESD Alliance and Semico will address trends and issues driving the rapidly growing market for 3rd party semiconductor Intellectual Property. Key information provides attendees an understanding of the underlying market forces that are driving the expanding use of 3rd party semiconductor IP and the outlook and challenges ahead.

Issues at the forefront of the design community include how die area partitioning, the rise in IP block content per SoC and rising gate counts all contribute to growing SIP market revenues. Other areas to explore include emerging IP such as Programmable Fabric, Discretes (capacitors and inductors), and the impact of rising design costs on design starts, units and IP licensing revenues as well as the impact of new 10nm and below processes that are already well under development.

SPEAKER:

Jim Feldhan - *Semico Research Corp., Phoenix, AZ*

UNSCRIPTED: WALLY RHINES

Date: Tuesday, June 7 || Time: 11:30am - 12:15pm || Room: DAC Pavilion - Booth 1839
Event Type: DAC Pavilion || Track: EDA, Automotive || Topic Area: General Interest

MODERATOR:

Ed Sperling - *Semiconductor Engineering, San Jose, CA*

ORGANIZER:

Laura Parker - *Mentor Graphics Corp., Wilsonville, OR*

Mentor Graphics' Chairman and CEO talks with Semiconductor Engineering's Ed Sperling in a live interview about consolidation, automotive software, and what the semiconductor industry will look like in five years.

SPEAKER:

Wally Rhines - *Mentor Graphics Corp., Wilsonville, OR*

SKY TALK: RISC-V: INSTRUCTION SETS WANT TO BE FREE

Date: Tuesday, June 7 || Time: 1:00pm - 1:30pm || Room: DAC Pavilion - Booth 1839
Event Type: SKY Talk || Track: IoT, IP || Topic Area: System Architectures & SoC, Codesign & System Design, General Interest

ORGANIZER:

Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

The most important interface in a computer system is the instruction set architecture (ISA) as it connects software to hardware. So, given the prevalence of open standards for almost all other important interfaces, why is the ISA still proprietary? We argue that a free ISA is a necessary precursor to future hardware innovation, and there's no good technical reason not to have free, open ISAs just as we have free, open networking standards and free, open operating systems.

The free and open RISC-V ISA began development at UC Berkeley in 2010, with the frozen base user ISA standard released in May 2014, and has since seen rapid uptake around the globe, including the first commercial shipments.

This talk will cover the technical features of the RISC-V ISA design , which has the goals of scaling from the tiniest implementations for IoT up to the largest warehouse-scale computers, with support for extensive customization. We'll also describe three different industry-competitive open-source cores developed at UC Berkeley, all written in Chisel, a productive new open-source hardware design language. Finally, we'll describe the uptake of RISC-V and the development of the RISC-V ecosystem, including the RISC-V Foundation.

SPEAKER:

Krste Asanovic - *Univ. of California, Berkeley & SiFive, Inc., Berkeley, CA*

STEERING SAFETY INNOVATION IN AUTONOMOUS CAR ELECTRONICS

Date: Tuesday, June 7 || Time: 2:00pm - 2:45pm || Room: DAC Pavilion - Booth 1839
Event Type: DAC Pavilion || Track: EDA, Automotive || Topic Area: General Interest, Circuit Design

MODERATOR:

James Hogan - *Vista Ventures, Los Gatos, CA*

ORGANIZER:

Michael "Mac" McNamara - *Adapt-IP, Palo Alto, CA*

The sophistication of the electronics that "drive" autonomous cars goes well beyond the obviously inherent system intelligence. Achieving the safety and reliability standards to which these devices must comply involves an unparalleled level of engineering innovation. Failsafe ICs that can self-repair their own operational issues sounds like technology fantasy, but this is an all too real requirement of the ISO 26262 regulations.

This panel of experts on various facets of automotive electronics specification, design and verification will steer us through a number of aspects of failsafe devices, revealing a roadmap of autonomous car electronics for which a no-crash guarantee is more than just desirable.

PANELISTS:

Philippe Laugier - *Melexis, Paris, France*
Martin Lukasiewycz - *Bosch Research, Stuttgart, Germany*
Raik Brinkmann - *OneSpin Solutions GmbH, Munich, Germany*

MORE IDEAS = MORE SOLUTIONS

Date: Tuesday, June 7 || Time: 3:30pm - 4:00pm || Room: DAC Pavilion - Booth 1839
Event Type: DAC Pavilion || Track: Design, IoT || Topic Area: Emerging Technologies, General Interest, Physical Design

ORGANIZER:
Ann Mutschler - *Sperling Media Group, San Jose, CA*

The world's greatest challenges need new science, technology, engineering, and math (STEM) ideas and insights. Half of the world's potential ideamakers—women and girls—are discouraged from developing their ideas because of social bias or inequity. More girls with more ideas create more solutions. Learn about women and girls who are changing the game with their innovations and solutions, and how Girlstart is engaging more girls in STEM.

SPEAKER:
Julie Shannan - *Girlstart, Austin, TX*

IFIXIT DRONE TEARDOWN

Date: Tuesday, June 7 || Time: 4:30pm - 5:00pm || Room: DAC Pavilion - Booth 1839
Event Type: DAC Pavilion || Track: Embedded Systems, IoT || Topic Area: General Interest

ORGANIZER:
Michelle Clancy - *Cayenne Communication, San Jose, CA*

iFixit routinely tackles drones and will do so again this year at DAC. At press time the model hadn't been determined but trust iFixit to choose well. Drones may look like toys, though behind the colorful fascia lies some very sophisticated electronics—which make flying the things easier all the time. You wouldn't guess that all the components iFixit will remove could lead to that much fun for drone hobbyists (and that many headaches for potential regulators).

SPEAKERS:
Andrew Goldberg - *iFixIt, San Luis Obispo, CA*
Samantha Lionheart - *iFixIt, San Luis Obispo, CA*

WHERE ARE WE WITH 3D IC AND TSV?

Date: Wednesday, June 8 || Time: 10:30am - 11:00am || Room: DAC Pavilion - Booth 1839
Event Type: DAC Pavilion || Track: EDA, Design || Topic Area: General Interest, Circuit Design, Lithography & DFM

ORGANIZER:
Anne Cirkel - *Mentor Graphics Corp., Wilsonville, OR*

Jan Vardaman, founder and president of Tech Search Inc. and a world recognized authority on advanced packaging technology, will talk about the state of packaging technology and 3D IC today. Jan will give insight into the obstacles that we have to overcome, into applications and where the industry needs to focus. The role of design will be highlighted throughout the presentation. Join us for an insightful perspective from design into manufacturing.

SPEAKER:
Jan Vardaman - *TechSearch International, Inc., Austin, TX*

UNSCRIPTED: LIP-BU TAN

Date: Wednesday, June 8 || Time: 11:30am - 12:15pm || Room: DAC Pavilion - Booth 1839
Event Type: DAC Pavilion || Track: EDA || Topic Area: General Interest

MODERATOR:
Ed Sperling - *Semiconductor Engineering, San Jose, CA*
ORGANIZER:
Qi Wang - *Cadence Design Systems, Inc., San Jose, CA*

Cadence's president and CEO talks with Semiconductor Engineering's Ed Sperling about where the money is flowing, how it's being spent or mis-spent, and how that will play out across the semiconductor industry.

SPEAKER:
Lip-Bu Tan - *Cadence Design Systems, Inc., San Jose, CA*

SKY TALK: SECURITY AT DIFFERENT LAYERS OF ABSTRACTIONS: APPLICATION, OPERATING SYSTEMS, AND HARDWARE

Date: Wednesday, June 8 || Time: 1:00pm - 1:30pm || Room: DAC Pavilion - Booth 1839
Event Type: SKY Talk || Track: Security, Embedded Systems || Topic Area: Business

ORGANIZER:

Ramesh Karri - *New York Univ., Brooklyn, NY*

When it comes to computer security, attackers often seek out weaknesses at the abstraction boundaries in a system. Therefore, boundaries between layers such as the hardware, operating system, and application have a significant security impact. This talk will address how security is influenced by different dimensions of computing including hardware and software abstractions and scale, along with how threat models can help to manage this complexity.

It concludes with a perspective on the largest security problems of the day: the ability for one entity to prove their security posture to another, simplifying security, and addressing the talent shortage. This talk is accessible to anyone interested in security and how it impacts the broad computing ecosystem.

SPEAKER:

Bryan Payne - *Netflix, Los Gatos, CA*

DESIGNING FOR THE IOT: REVOLUTION OR RENAISSANCE?

Date: Wednesday, June 8 || Time: 2:00pm - 2:45pm || Room: DAC Pavilion - Booth 1839
Event Type: DAC Pavilion || Track: IoT, Embedded Systems || Topic Area: General Interest

ORGANIZER:

Michael “Mac” McNamara - *Adapt-IP, Palo Alto, CA*

Somehow “embedded systems design” has become “Internet of Things,” as if it’s a whole new science. Fact is, we’ve been designing IoT devices since forever. Some are great; some less so. In this talk we examine trends in the embedded/IoT business and look at where it’s heading, with stops along the way to enjoy some of the scenic turnouts.

SPEAKER:

Jim Turley - *Silicon Insider, Pacific Grove, CA*

CHASING DOWN EVERY LAST PICOJOULE IN THE INTERNET OF THINGS

Date: Wednesday, June 8 || Time: 3:30pm - 4:00pm || Room: DAC Pavilion - Booth 1839
Event Type: DAC Pavilion || Track: Design, IoT || Topic Area: Low-Power & Reliability, Circuit Design, General Interest

ORGANIZER:

Zhuo Li - *Cadence Design Systems, Inc., Austin, TX*

The emergence of the Internet of Things (IoT) will be closely tied to the emergence of ultra-low power electronics. Billions of battery-powered devices will be shipped as part of the IoT explosion, which will create a need to keep billions of batteries charged up. To fully realize the IoT vision will require energy-efficient microcontrollers, radios, sensors, and power electronics. It will also require dramatic improvements to the energy efficiency of software, something that is often overlooked. One of the most promising techniques for achieving the ultra-efficient energy requirements demanded by IoT is sub-threshold circuit operation.

In this talk I will discuss a variety of approaches for minimizing energy usage in IoT electronics and will focus particularly on the opportunity and challenges presented by sub-threshold operation.

SPEAKER:

Scott Hanson - *Ambiq Micro, Austin, TX*

IFIXIT APPLE TEARDOWN

Date: Wednesday, June 8 || Time: 4:30pm - 5:00pm || Room: DAC Pavilion - Booth 1839
Event Type: DAC Pavilion || Track: Embedded Systems, IoT || Topic Area: General Interest

ORGANIZER:

Michelle Clancy - *Cayenne Communication, San Jose, CA*

Last year at DAC it was a modest little product called Apple Watch that went under the knife. Yes, it can be painful to watch a spudger being applied to anything designed by Sir Jonathan Ive, “Apple’s greatest product,” according to a sprawling feature in The New Yorker last year. Still, iFixit has a job to do, one that can be somewhat difficult given Apple’s famous aversion to tinkering and tampering.

This is the company, after all, that developed the five-pointed Pentalobe screw. Don’t worry, iFixit made relatively short work of the Apple Watch last year and is sure to do the same with the next device. Sorry, Sir Jony.

SPEAKERS:

Samantha Lionheart - *iFixIt, San Luis Obispo, CA*
Andrew Goldberg - *iFixIt, San Luis Obispo, CA*

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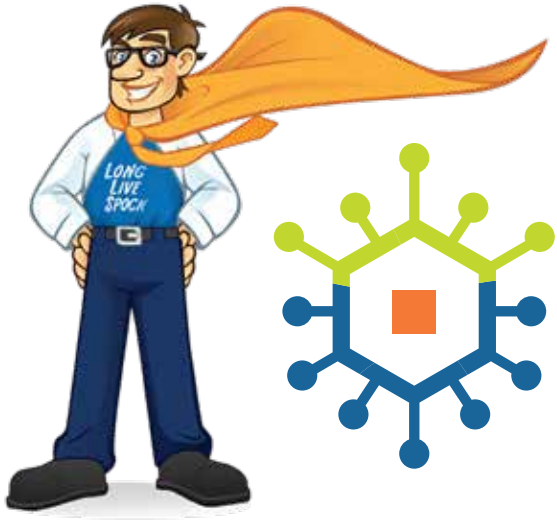

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Have fun and meet people as you make your way towards becoming one of this year's big winners!

Raffle prizes and the grand prize winner will be announced on Wednesday, June 8, 2016, at 4:00pm at the DAC Pavilion.
As some prizes may be shipped to winning contestants, you do not need to be present to win.

Grand Prize: Virtual Reality Headset

Raffle prizes: $150 Gift Card to the Apple Store
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Game Begins: 10:00am, Monday, June 6 | Game Ends: 4:00pm, Wednesday, June 8

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** Check the Mobile App for the most up-to-date exhibitor list!*

2. Find a member of the DAC Executive Committee: **100 points**

Each member of the committee will be wearing a button with a QR code to scan.

3. Design/IP Poster Sessions: **50 points**

The Monday and Tuesday Design/IP poster sessions will have 4 QR codes located throughout the session. Scan the code for 50 points each. Each code may only be scanned once.

4. Find the missing treasure hidden around the show each day: **150 points**

This gets you the most points! Each day of the exhibit (Monday, Tuesday and Wednesday) DAC will hide Elliott, the Engineering Superhero action figure. Elliott will have a QR code on him, scan the code and earn the point. Please return Elliott to his hidden area for the next person to find.

PRIZES

*DAC Attack ends at **4:00pm on June 8th.** Raffle prizes and the grand prize winner will be announced on Wednesday, June 8, 2016, at 5:00pm at the DAC Pavilion and by broadcast message within the App.*

Registered attendees are eligible to win any of the prizes! There are two types of prizes: raffle prizes and the grand prize. Raffle winners will be selected from the top 50% of highest points scored. The Grand Prize will be randomly selected from the top 10% of the highest points scored.

Grand Prize:
Virtual Reality Headset

Raffle Prizes:
- $150 Gift Card to the Apple Store
- $150 Gift Card to Amazon
- Beats Solo Headphones
- Phantom Drone

RULES AND HELPFUL INFORMATION

- Please play fair! We reserve the right to remove points that were obtained in a fraudulent manner.
- Look for the QR markers around the exhibit floor located at each booth. If you do not see a QR code, ask the exhibitor where they are placed. Each code you scan through the DAC Mobile App earns you a variety of points that go towards your total tally.
- Check the leaderboard in the app or the Social Media boards at the show to see how many points you have, and where you stand on the leaderboard. Please note that the leaderboard updates approximately every 5 minutes.
- Registered attendees are eligible to win any of the prizes! Exhibitors and exhibit staff are not eligible to win.
- As some prizes may be shipped to winning contestants, you do not need to be present to win.

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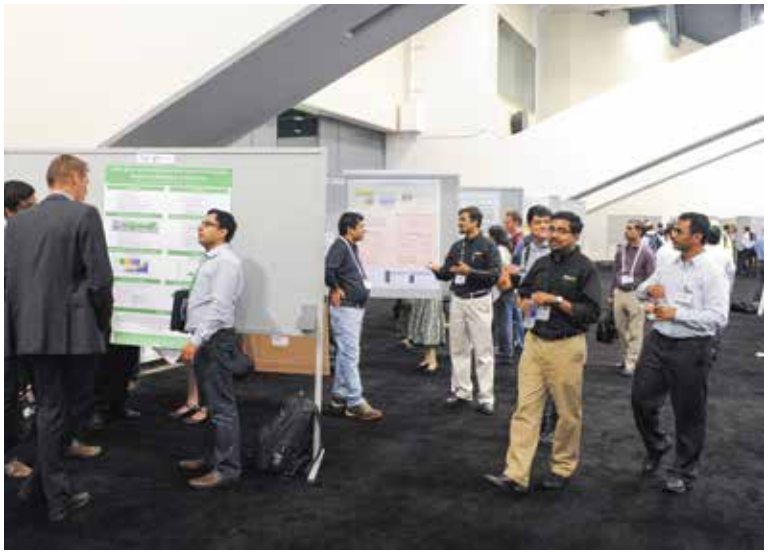

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