Program Highlights

Technical Program - details on pgs. 14 - 35

The technical program covers over 160 papers, panels and special sessions in five parallel tracks covering system level design, synthesis, physical design, verification, interconnect, power and IP issues. Highlights include a focus on embedded systems (see right) as well as a number of special sessions with invited paper presentations on the future of nanometer design, visualization and animation in VLSI design, the impact of subwavelength lithography and on closing the gap between full custom design and ASICs.

TUESDAY KEYNOTE
Henry Samueli

Co-Chairman and Chief Technical Officer
Broadcom Corporation, Irvine, CA
Tuesday, June 19 - 9:00 AM
Room: Hilton Pavilion (Las Vegas Hilton)

Best Paper Awards

Best Paper Awards of $1000 each will be announced at the Tuesday morning General Session. Papers eligible for awards in this category are nominated by the Program Committee and selected by a referee process. Awards will be given in each of the following categories:

1. Design Synthesis, Test and Validation
2. Analog/RF/Electrical Modeling and Simulation
3. Design Methodology (2)
4. Embedded Systems

Ph.D Forum
Tuesday, June 19 - details on pg. 64

A chance for Ph.D students and industry representatives to get together. Students get feedback on their research proposals; industry gets a chance to meet students and preview their work.

Embedded Systems - See sessions: 3, 17, 23, 28, 32, 37, 41, 42, 49

Recognizing the increasing role of embedded software and IP in complex SoC designs we have provided a special focus on embedded systems topics. Over 35 papers and panels will cover topics such as embedded compilation, hardware/software co-design, system modeling and power optimization. In addition, special invited sessions will discuss the critical topic of on-chip communication architectures, as well as provide a real-life practical embedded case study dealing with the implementation of the Bluetooth wireless standard. Also, a panel of experts will examine the multifaceted space of embedded systems and the role of EDA in this space.

THURSDAY KEYNOTE
Willem P. Roelandts

President and Chief Executive Officer
Xilinx, Inc., San Jose, CA
Thursday, June 21 - 1:00 PM
Room: N109 - N114

Tutorials – Friday, June 22 - details on pgs. 36 - 41

1) Design-for-Test Techniques for SoC Designs
2) Interactive Tutorial on Fundamentals of Signal Integrity for High-Speed/High-Density Design
3) CAD tools for mixed-signal and RF ICs
4) Design-Manufacturing Interface for UDSM Era: Designer and CAD Tool Developer Perspectives
5) Low Power Tools and Methodologies for the ASIC Industry
6) Field Programmable Devices: Architecture and CAD Tools

Microelectronic System Educators Conference
June 17 – 18 - Las Vegas Hilton, Nevada

For more information, visit www.mseconference.org.

On-Site Information Desk

The information desk will be located in the Grand Concourse. (702) 943-3500

Exhibit Highlights

Exhibit Floor

Monday - Wednesday, June 18-20, 2001 10:00 AM - 6:00 PM

Over 260 EDA, Silicon, IP and Embedded Systems companies participate in the DAC exhibition and demo suites. All exhibits and suites are located in Halls C1-C5 of the Las Vegas Convention Center.

Embedded Systems Showcase

The Embedded Systems showcase offers exhibitors and attendees a highly focused area to display and view tools for the design of embedded systems-on-chip.

Featured Product Segments

- *Embedded Systems Hardware:* SoC, IP re-use, on-chip buses
- *Embedded Systems Software:* run-time schedulers, middleware, compilers
- *HW/SW Co-Design:* specification languages, interfaces and integration, partitioning, synthesis
- *Validation:* debug, performance estimation and analysis, co-simulation
- *Applications:* application-architecture interaction, networked and distributed systems, multimedia systems

The latest innovations are at your fingertips with exhibitors highlighting their latest products.

No badge needed to attend Exhibitor Presentations on Monday, June 18.

Exhibit-Only

- Free Monday Exhibit-Only Passes - call toll-free **1-800-321-4573**, or register on line at **www.dac.com**.
- $40 full exhibit-only registration will allow you to attend exhibits Monday through Wednesday.

Exhibitor Presentations - Monday, June 18, 2001

- A full day of 15-minute Exhibitor Presentations - choose from 168 presentations; see pages 50 - 59 for details.

Demo Suites

Monday - Wednesday, June 18-20, 2001 .....**8:00 AM - 9:00 PM**
Thursday, June 21, 2001 .....**8:00 AM - 5:00 PM**

- Demo Suites will be in Halls C4 & C5 of the Las Vegas Convention Center.
- Exhibiting companies will have the opportunity to give their customers private demos without leaving the Convention Center.
- Demo Suites are available by invitation only.

Important Information At-A-Glance

	Exhibit Hours: (badge required)	Demo Suite Hours: (by invitation only)
Monday, June 18	10:00 AM to 6:00 PM	8:00 AM to 9:00 PM
Tuesday, June 19	10:00 AM to 6:00 PM	8:00 AM to 9:00 PM
Wednesday, June 20	10:00 AM to 6:00 PM	8:00 AM to 9:00 PM
Thursday, June 21	–	8:00 AM to 5:00 PM

Children under 14 years of age will not be admitted into the exhibit hall or demo suite area.

At-Conference Registration Hours

The registration desk will be located in the Grand Concourse of the Las Vegas Convention Center and will be open at the following times:

Sunday, June 17 .....8:00 AM to 4:00 PM
Monday, June 18 .....8:00 AM to 6:00 PM
Tuesday, June 19 .....7:30 AM to 5:00 PM
Wednesday, June 20.....7:30 AM to 5:00 PM
Thursday, June 21 .....7:30 AM to 3:00 PM

Tutorial Registration .....Friday, June 22, 8:00 AM to 1:00 PM

To avoid long lines register in advance by May 21, 2001.

Free Monday Exhibit-Only Passes

Register by June 1, 2001, and receive your badge via the US mail for immediate access to the exhibit hall at 10:00 AM, June 18, 2001 Call 1-800-321-4573 or 1-303-530-4333, or visit the DAC web site at www.dac.com.

Conference Survey

Again this year, we would like you to voice your opinion on various aspects of the conference. DAC is conducting surveys to determine how to best serve your needs. Please take a few moments to participate if you are approached by one of our surveyors. Look for interviewers wearing "???" buttons at various locations around the show. Help make a difference in DAC and receive a gift for participating.

Workshop for Women in Design Automation
Sunday, June 17 - details on pg. 6

Smart Risk Taking = Innovation - This unique program offers the opportunity to hear successful, professional women speak on topics relevant to their careers.

Interoperability Workshop
Sunday, June 17 - details on pg. 7

This workshop invites leading Semiconductor, System and EDA companies to discuss the need for a new design system architecture and supporting standard data model API.

Conference Information

About the Conference

The 38th Design Automation Conference provides a high-quality program facilitating technology interchange among design automation researchers and developers, the engineers who use DA systems to design, test and manufacture circuits and systems, and the vendors who provide both electronic design automation (EDA) systems and silicon. Five full days of activities are planned. New product introductions and application notes will be highlighted on Monday in the Exhibitor Presentations, and more than 260 companies will exhibit the latest commercially available products Monday through Wednesday.

This year's conference highlights the role of embedded systems in today's electronic design. This is reflected in an "Embedded Systems Showcase" on the exhibit floor, a plenary panel session of top executives on Wednesday on "Embedded System Design: The Real Story", and multiple technical sessions sprinkled throughout the program addressing the design challenges and solutions of embedded systems.

Technical innovations from DA research and development and the use of DA in design of chips and systems will be presented in five parallel sessions, Tuesday through Thursday, in the Technical Program. Two keynote addresses outline the challenges the EDA field is facing: the first one, featured on Tuesday morning, by Dr. Henri Samueli, Co-founder and Chief Technical Officer of Broadcom Corporation, and the second one on Thursday afternoon by Willem Roelandts, President and Chief Executive Officer of Xilinx, Inc.

The Technical Program consists of panel discussions, special sessions, and technical paper sessions. The Design Tools track focuses on new techniques for enhancing the performance and capabilities of EDA tools. The Design Methods track focuses on the results and insights gained by applying EDA tools to actual system designs.

In addition to the Plenary Panel, there are seven other panel discussions covering topics that range from dealing with the challenge posed by FPGAs to ASICs, to the verification of embedded cores, and an analysis of the supply chain in the electronics industry. The program also features 26 invited presentations, covering exciting topics such as the design of Bluetooth chip-sets to "interconnect-networks-on-a-chip". The conference concludes with six full-day tutorials on Friday.

Virtual DAC (www.dac.com)

Virtual DAC offers two powerful on-line tools for attendees to make the most of their time at DAC. The "DAC Floor" is designed to allow attendees to plan the exhibitors they want to visit and to create a floor plan marking the locations of the selected exhibitors. The "DAC Planner" is designed for attendees to plan which technical sessions and other important DAC events they want to attend. Together the two services allow attendees to organize, in advance, how they want to utilize their time at DAC.

Exhibit Information

Exhibits

There will be over 260 exhibiting companies at the 38th DAC. For a listing and other information, see pages 46 - 47. **Children under the age of 14 will NOT be allowed in the exhibit hall or demo suite area.**

Embedded Systems Showcase

The Embedded Systems showcase offers exhibitors and attendees a highly focused area to display and view tools for the design of: embedded systems, embedded software cores, IP, compilers & middleware, and other products critical to the design of Embedded Systems. Besides giving embedded designers direct access to the latest tools and methodologies for automating the design of embedded systems and components in SoC design, the Embedded Systems Showcase also provides a forum where vendors and embedded systems designers can meet and exchange ideas, opinions and new discoveries. In addition, a full-fledged embedded systems technical paper track will also be featured at DAC, providing timely, in-depth information for attendees designing embedded systems.

Free Monday Exhibit-Only Passes

The 38th DAC is offering Free Monday Exhibit-Only Passes. These passes are used to enter exhibits free of charge on Monday, June 18, 2001, and may be obtained from DAC Exhibitors, the DAC Free Monday Hot Line: toll-free 1-800-321-4573, 1-303-530-4333, or on line at www.dac.com.

Advance registration for the Free Monday Exhibit-Only Passes ends June 1, 2001. After June 1, 2001, Free Monday Exhibit-Only Passes will be available AT-CONFERENCE ONLY.

Exhibit-Only Admission

To enter the exhibits Monday, June 18, 2001, through Wednesday, June 20, 2001, purchase an Exhibit-Only Pass for $40.00. To avoid long lines, register in advance by using the registration form located on the inside back cover, or register on-line at www.dac.com.

Exhibitor Presentations

Exhibitor Presentations will be held on Monday, June 18, 2001, from 9:00 AM to 6:00 PM. The Exhibitor Presentations will be 15-minute time slots with six sessions running concurrently. For more information see the matrix and abstracts for Exhibitor Presentations on pages 48 - 59. No badge needed.

DACnet-2001

The Design Automation Conference is pleased to provide conference attendees and exhibitors the DACnet Mail and Information System. The DACnet system allows attendees direct internet access for the duration of DAC. Once established, users can log-in to any of the DACnet stations at the conference.

Each workstation will have a browser available for immediate web and virtual DAC access, and telnet access. If you would like to establish an email account at DAC, just follow the instructions at a DACnet location. Pre-registration is not required or allowed this year. If you have any questions about DACnet, email kevin@dac.com.

Workshop for Women in Design Automation

Sunday, June 17 • 8:00am - 4:00pm

Smart Risk Taking = Innovation

Room: N115

WORKSHOP CHAIR:
Mar Hershenson,
CEO, Barcelona Design, Inc.

Creating a climate that embraces risk in order to achieve true innovation is perhaps the most daunting challenge facing today's fast-paced companies. Innovation, by definition, means doing things differently, exploring new territory and taking risks. At this year's Workshop for Women in Design Automation, prominent EDA industry leaders will divulge their own strategies for developing corporate cultures that encourage and reward smart risk taking to improve product development and delivery. You will leave the Workshop armed with practical knowledge that you can use to make a positive difference in your workplace.

9:00 am - Keynote Address
Lynn LeBlanc, Cadence Design Systems, Inc.
Senior Vice President,
Office of Customer Advocacy

Lynn has twenty years of experience in the technology industry with a reputation for developing highly effective organizations and launching first-to-market technologies. In her current role, Lynn has responsibility for worldwide customer satisfaction for Cadence and directs innovative programs that enhance and strengthen customer partnerships. Prior to her current appointment at Cadence, Lynn held senior management positions at Mentor Graphics, iReady, Octel Communications and IBM. In her keynote address, Lynn will share her experiences with creating empowering environments that foster respect, tolerate risk and celebrate success.

10:15 am - Panel: *Embracing the Culture of Risk: A Mandate for Successful Organizations*

Moderator: **Lynda Kaye**

During this interactive session, panelists will provide insights into the development and management of successful, risk tolerant corporate cultures. They will share personal successes, failures, philosophies and observations and respond to questions from audience members.

Kathleen Doler – Electronic Business Magazine
Deirdre Hanford – Synopsys, Inc.
Penny Herscher – Simplex Solutions, Inc.
Nancy Nettleton – Sun Microsystems
Walden C. Rhines – Mentor Graphics Corp.
Gabriele Saucier – Design and Reuse

ORGANIZERS: *Lynda Kaye* – President, Mango Communications
Luciana Guarnieri – Marketing Manager, Barcelona Design, Inc.

STEERING COMMITTEE: *Karen Bartleson* – Director of Interoperability, Synopsys, Inc.
Marie R. Pistilli – Co-Chair, Board of Directors, MP Associates, Inc.
Ellen J. Yoffa – DAC Executive Committee, EDA Industry Chair

Schedule

(breakfast, lunch and the reception will be in room N119)

8:00 am Registration and Continental Breakfast
9:00 am Keynote Address: Lynn LeBlanc
10:00 am Break
10:15 am Panel: *Embracing the Culture of Risk: A Mandate for Successful Organizations*
12:00 pm Lunch Speaker: Mar Hershenson *From Idea to Start-Up - How to Get There*
1:00 pm Interactive Workshop 1 – *Innovative Marketing*
Leader: **Kuhoo Goyal** - TechBites Interactive
1:45 pm Interactive Workshop 2 – *Risk and Reward for Engineering Organizations*
Leader: **Lori Watrous-de Versterre**, Mentor Graphics Corp.
2:30 pm Interactive Workshop 3 – *New Approaches to Business Development*
Leader: **Leslie Landers**, Interra, Inc.
3:15 pm Break
3:40 pm Achievement Award Ceremony – Join us as we honor the recipient of this year's *Marie R. Pistilli Women in EDA Achievement Award.*
3:55 pm Closing Remarks: Mar Hershenson
4:00 pm Reception: Sponsored by the EDA Consortium

Interoperability Workshop

Sunday, June 17 • 12:00pm - 5:00pm

: N115

Room: N117

Interoperability among EDA tools has long been a topic of passionate discussion and many standard file formats have been proposed to help. But, the rapid advance in semiconductor technology combined with the need for more predictable and productive automated design processes are demanding a much tighter coupling of new EDA tools. There is a growing community of technical experts who believe that for EDA to keep pace with semiconductor technology, new more modular applications will need to operate on shared design data in memory. Several EDA companies have announced design systems with suites of tools tightly coupled around their proprietary data models. But to be able to assemble such systems with the best components from multiple suppliers, we will need a standard application programming interface for sharing design data.

This Workshop brings together design system architects from the leading Semiconductor, System and EDA companies to discuss:

- The benefits seen to date from tightly-coupled applications
- The technical issues in achieving tight coupling of tools
- The pressing need for a standard API for accessing design data
- The Open Source Model as a mechanism for achieving and advancing such a standard

WORKSHOP ORGANIZERS: ***John Darringer*** - Mgr. System-Design, IBM Research
Terry Blanchard - Mgr. VLSI Technology Center, Hewlett-Packard Co.
Greg Spirakis - General Mgr. Design Technology, Intel Corp.

Schedule

12:00pm Lunch *(will be in room N108)*

1:00pm Welcome and Workshop Objectives: ***John Darringer***

1:15pm Session 1 - *Tight Coupling Progress and Issues from the User Community* *Chair:* ***Terry Blanchard*** - Mgr. VLSI Technology Ctr., Hewlett-Packard Co.
Yi-hung Chee - Principal Engineer, CAD Infrastructure, Intel Corp.
Sumit Dasgupta - Dir. of SoC-IP Design Systems, Motorola, Inc.
Jean-pierre Geronomi - Dir. of CAD, ST Microelectronics
Joe Morrell - Sr. Technical Staff, IBM Corp.
Scott Petersen - Dir. Silicon Optimization, LSI Logic Corp.
Jim Wilmore - CAD System Architect, Hewlett-Packard Co.

2:30pm Session 2 - *Tight Coupling Progress and Issues from the EDA Companies* *Chair:* ***Greg Spirakis*** - General Manager Design Technology, Intel Corp.
Mark Bales - Corporate Fellow, Cadence Design Systems, Inc.
Tim Burks - Dir. of Engineering, Magma Design Automation, Inc.
Raul Campasano - Sr. VP, GM Tool Design Group, Synopsys, Inc.
Greg Dufour - Strategic Technology Advancement, Mentor Graphics Corp.
Vivek Raghavan - Head of Physical Design Products, Avant! Corp.
Bob Shortt - Mgr. R&D, Monterey Design Systems

3:30pm Break

3:45pm Panel: *Can There be a Standard Interface for Tight Coupling?* Chair: ***Richard Goering*** - Editor, EE Times
Presentation: *The Design API Coalition and Open Source* - Don Cottrell - Si2
Panel members to be selected from workshop speakers and audience.

4:45pm Wrap-up: ***John Darringer***

5:00pm Adjourn

Tuesday Keynote – Designing in the New Millennium, It's Even Harder Than We Thought

Henry Samueli
Co-Chairman and Chief Technical Officer
Broadcom Corporation, Irvine, CA
Tuesday, June 19, 2001, 9:00 am - 10:15 am
Room: Hilton Pavilion

Abstract: System-on-a-chip (SoC) design has taken on a new level of sophistication in the new millennium with the advent of 100 million transistor chips incorporating dozens of blocks of IP originating from a wide variety of internal and external sources. Today's SoC designs incorporate general purpose processor cores, programmable DSP cores, dedicated DSP engines, dedicated protocol engines, large random logic and memory blocks and precision high-speed analog blocks. A cornerstone of Broadcom's strategy in achieving rapid time-to-market lies in the heavy use of design automation tools, augmented with in house customization and methodology development. This talk will give an overview of the challenges the design community will face in the coming years in developing very complex SoC's, and will also discuss Broadcom's EDA strategy to address these problems.

Biography: Dr. Henry Samueli is a co-founder of Broadcom Corporation and has served as Co-Chairman and Chief Technical Officer (CTO) since the company's inception in 1991. As CTO he is responsible for all research and product development activities for the company. Dr. Samueli has over 20 years experience in the fields of digital signal processing (DSP) and communications systems engineering. He is widely recognized as one of the world's leading experts in the field of broadband communications circuits, having published more than 100 technical papers on the subject. Dr. Samueli also co-founded PairGain Technologies in 1988 and served as Chief Scientist of the company until 1994. He was the principal architect of PairGain's high bit-rate digital subscriber line (HDSL) transceiver. Since 1985, Dr. Samueli has been a professor in the Electrical Engineering Department at UCLA, where he supervises advanced research programs in DSP and broadband communications circuits. He has been on leave of absence from UCLA since 1995. From 1980-1985, Dr. Samueli held various engineering management positions in the Electronics and Technology Division of TRW, where he was responsible for the hardware development of various military satellite and digital radio communications systems. Dr. Samueli received a B.S., M.S. and Ph.D. in Electrical Engineering from UCLA in 1975, 1976 and 1980, respectively.

Thursday Keynote – FPGAs Enter the Mainstream

Willem P. Roelandts
President and Chief Executive Officer
Xilinx, Inc., San Jose, CA
Thursday, June 21, 2001, 1:00 pm - 1:45 pm
Room: N109 - N114

Abstract: A few years ago field programmable gate arrays (FPGAs) were expensive, slow and small. But thanks to recent breakthroughs in technology, FPGAs today offer tens of millions of system gates, they operate at 200 MHz or more and they cost less than $10. Meanwhile, FPGA software tools are faster than ever, compiling million-gate designs in 30 minutes and contributing to significant improvements in the productivity of digital logic designers. Even more FPGA advancements are on the horizon: embedded processors, high-level language support, remotely configurable hardware, and fast serial I/Os. With this accelerating pace of change, the CEO of Xilinx believes it's feasible that programmable logic will be an integral part of all digital electronic products within the next decade.

Biography: Willem P. "Wim" Roelandts has served as president and chief executive officer of Xilinx since January 1996. He is responsible for formulating the company's overall strategy, vision and focus necessary for Xilinx to continue its pace of rapid growth and expansion.

During Roelandts' tenure at Xilinx, revenue has tripled to about $1.5 billion. Today Xilinx is widely recognized as one of the best managed and most financially sound high technology companies in the world. In 2000, BusinessWeek ranked Xilinx the sixth most profitable company in the magazine's listing of the top 100 information technology companies. FORTUNE recently added Xilinx to the magazine's coveted list of the top 100 companies to work for. And Forbes magazine now includes Xilinx in its list of America's 400 best big companies. Under Roelandts' leadership, Xilinx has also become the leading supplier of programmable logic chips, one of the fastest growing segments of the overall semiconductor industry. Market researcher Dataquest now ranks Xilinx as the sixth largest supplier of custom logic chips in the world.

Since joining Xilinx, Roelandts has played an increasingly active role in industry affairs. He serves on the board of directors of the Semiconductor Industry Association and the Technology Network, and he is president of the Fabless Semiconductor Association. Roelandts also frequently acts as a keynote speaker at industry conferences and trade shows.

Roelandts joined Xilinx after a 30-year career in management at Hewlett-Packard Co. In his last position there, he served as senior vice president and was responsible for all aspects of HP's then $6 billion worldwide computer systems business, including research and development, manufacturing, marketing, professional services and sales.

Roelandts joined Hewlett-Packard in 1967 as a service engineer in Belgium. He was promoted to customer-engineering/systems engineering manager in 1973. In 1975, he was transferred to HP's former Grenoble (France) Division where he was product support manager, European support center manager and research and development manager.

In 1982, Roelandts was named operations manager for the Grenoble Networks Operation. In 1983, he was named R&D manager for HP's Information Networks Division in Cupertino, California. He was promoted to division general manager in 1984, and to general manager for the Information Networks Group in 1985.

Roelandts was elected as HP vice president in 1988 and became general manager of the Computer Systems Group later that year. He was named general manager of the Networked Systems Group in 1990 when HP realigned its computer business activities and was named general manager of the Computer Systems Organization in 1992. He was elected a senior vice president in 1993.

Roelandts was born January 4, 1945, in Lennik, Belgium. He earned his bachelor's degree in electrical engineering from Rijks Hogere Technische School in Anderlecht, Belgium, in 1965.

Tuesday, June 19, 2001

9:00 to 10:15 — **Opening Session and Keynote Speaker** (no badge required) **Location: Hilton Pavilion** (Las Vegas Hilton)

Designing in the New Millennium, It's Even Harder Than We Thought

Henry Samueli - Co-Chairman and Chief Technical Officer, Broadcom Corporation, Irvine, CA

BREAK 10:15 - 10:30

	Room N111 - N114	Room N109 - N110	Room N115 - N117	Room N119 - N120	Room N107 - N108
	Session 1	Session 2	Session 3	Session 4	Session 5
10:30 to 12:00	**PANEL:** The Electronics Industry Supply Chain: Who Will do What?	**SPECIAL SESSION:** Nanometer Futures	System-Level Configurability: Bus Interface and Processor Design	Making Verification More Efficient	SoC and High-Level DFT

LUNCH 12:00 - 2:00

	Session 6	Session 7	Session 8	Session 9	Session 10
2:00 to 4:00	**PANEL:** The Next HDL: If C++ is the Answer, What Was the Question?	**SPECIAL SESSION:** Design for Subwavelength Manufacturability: Impact on EDA	New Ideas in Logic Synthesis	Analog Design and Modeling	Scan-Based Testing

BREAK 4:00 - 4:30

	Session 11	Session 12	Session 13	Session 14	Session 15
4:30 to 6:00	**PANEL:** Your Core - My Problem? Integration and Verification of IP	**SPECIAL SESSION:** Configurable Computing: Reconfiguring the Industry	Interconnect Design Optimization	Power Estimation Techniques	Functional Validation Based on Boolean Reasoning (BDD, SAT)

DAC Cocktail Party at the Las Vegas Convention Center 6:00pm - 7:00pm

Ph.D Forum at the Las Vegas Convention Center 7:00pm - 9:00pm • Room N250

Exhibit Hours 10:00am - 6:00pm / **Demo Suite Hours** 8:00am - 9:00pm

All Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Presenters will be available in rooms N104 and N118 for additional 20-minute question and answer sessions.

Wednesday, June 20, 2001

	Room N111 - N114	Room N109 - N110	Room N115 - N117	Room N119 - N120	Room N107 - N108
	Session 16	**Session 17**	**Session 18**	**Session 19**	**Session 20**
8:30 to 10:00	**SPECIAL SESSION:** Verification: Life Beyond Algorithms	**SPECIAL SESSION:** Dissecting an Embedded System: Lessons from Bluetooth	Algorithmic and Compiler Transformations for High-Level Synthesis	Gate Delay Calculation	Memory, Bus and Current Testing
	BREAK 10:00 – 10:30				
	Plenary Panel				
10:30 to 12:00	**Embedded System Design: The Real Story** Room N109-N114 This panel of senior executives, users and providers of embedded systems will examine this burgeoning and increasingly important space.				
	LUNCH 12:00 – 2:00				
	Session 21	**Session 22**	**Session 23**	**Session 24**	**Session 25**
2:00 to 4:00	**PANEL:** (When) Will FPGAs Kill ASICs?	**SPECIAL SESSION:** Inductance 101 and Beyond	Memory Optimization Techniques for DSP Processors	Technology Dependent Logic Synthesis	Collaborative and Distributed Design Frameworks
	BREAK 4:00 – 4:30				
	Session 26	**Session 27**	**Session 28**	**Session 29**	**Session 30**
4:30 to 6:00	**PANEL:** When Will the Analog Design Flow Catch Up with the Digital Methodology?	**SPECIAL SESSION:** Closing the Gap Between ASIC and Custom: Design Examples	Energy and Flexibility Driven Scheduling	Representation and Optimization for Digital Arithmetic Circuits	Techniques for IP Protection

38th DAC • VIVA Las Vegas Party • 7:30pm – 10:30pm • Hilton Center (Las Vegas Hilton)

Exhibit Hours 10:00am - 6:00pm / **Demo Suite Hours** 8:00am - 9:00pm

All Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Presenters will be available in rooms N104 and N118 for additional 20-minute question and answer sessions.

Thursday, June 21, 2001

	Room N111 - N114	Room N109 - N110	Room N115 - N117	Room N119 - N120	Room N107 - N108
	Session 31	**Session 32**	**Session 33**	**Session 34**	**Session 35**
8:30 to 10:00	**SPECIAL SESSION:** Visualization and Animation for VLSI Design	Application-Specific Customization for Systems-on-a-chip	Satisfiability Solvers and Techniques	Power and Interconnect Analysis	Domain Specific Design Methodologies
	BREAK 10:00 – 10:30				
	Session 36	**Session 37**	**Session 38**	**Session 39**	**Session 40**
10:30 to 12:00	**PANEL:** Debate: Who Has Nanometer Design under Control?	Analysis and Implementation for Embedded Systems	Industrial Case Studies in Verification	Integrated High-Level Synthesis Based Solutions	Timing Verification and Simulation
	Keynote – *FPGAs Enter the Mainstream* • 1:00 – 1:45 • Room: N109 - N114 ***Willem P. Roelandts*** - President and Chief Executive Officer, Xilinx, Inc.				
	Session 41	**Session 42**	**Session 43**	**Session 44**	**Session 45**
2:00 to 4:00	**SPECIAL SESSION:** On-Chip Communication Architectures	Compiler and Architecture Interactions	Timing with Crosstalk	Low Power Design: Systems to Interconnect	Floorplanning Representations and Placement Algorithms
	BREAK 4:00 – 4:30				
	Session 46	**Session 47**	**Session 48**	**Session 49**	**Session 50**
4:30 to 6:00	**PANEL:** What Drives EDA Innovation?	Signal Integrity: Avoidance and Test Techniques	Novel Approaches to Microprocessor Design and Verification	Scheduling Techniques for Power Management	Novel Devices and Yield Optimization

Demo Suite Hours 8:00am - 5:00pm

All Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.
Presenters will be available in rooms N104 and N118 for additional 20-minute question and answer sessions.

Opening Session

Location: Hilton Pavilion (Las Vegas Hilton)

Opening Remarks: Jan Rabaey - General Chair, 38th DAC

Awards Presented By: Steven P. Levitan, ACM/SIGDA Representative; Bing Sheu, IEEE/CAS Representative

Opening Keynote Address: Henry Samueli, Co-Chairman and Chief Technical Officer, Broadcom Corporation, Irvine, CA

Awards/Scholarships

P.O. Pistilli Scholarships (ACSEE)

Scholarships will be awarded to five high school students of under-represented minorities who will be pursuing a degree in Electrical Engineering or Computer Science.

Graduate Scholarships

Scholarships will be awarded to five graduate students to support research in Design Automation.

Student Design Contest Award

Award will be presented to the school sponsoring the best entry to the contest.

Best Paper Awards

Best Paper Awards will be given in the following areas:

1. Design Synthesis, Test and Validation
2. Analog/RF/Electrical Modeling and Simulation
3. Design Methodology (2)
4. Embedded Systems

Individual Awards

2001 IEEE Fellows
ACM/SIGDA Outstanding Ph.D Dissertation Award in Electronic Design Automation
ACM/SIGDA Distinguished Service Award
Outstanding New Faculty Award

Tuesday
June 19

9:00
to
10:15

No badge required

Tuesday June 19

10:30 to 12:00

All speakers are denoted in bold

S – denotes short paper

Session 1

rm: N111-N114

PANEL: THE ELECTRONICS INDUSTRY SUPPLY CHAIN: WHO WILL DO WHAT?

CHAIR: *Rita Glover - EDA Today, Kingman, AZ*
ORGANIZER: *Rita Glover*

The makeup and relationships within the design supply chain are changing rapidly. One-stop shopping, whereby a system house procures most of its design and fabrication services from a single source, is now being supplemented by a host of outsourcing suppliers. These players are developing online integration platforms for outsourced design engineering, business transactions, and data management. This evolution is being felt by the entire design automation industry, whether it be focused on the electronic design for chips, boards, or systems, or even the mechanical design of their packaging and housing. What are the implications of this trend on cost, demand for services, and time to market? How can all parties ride this wave of the future to achieve the best outcome in terms of collaborative design capabilities and quality of results?

PANELISTS:

Rich Becks - Seagate, Longmont, CO
Rick Cassidy - TSMC, San Jose, CA
Henry Jurgens - Celestica, Toronto, ON, Canada
Richard Kubin - Nortel, Research Triangle Park, NC
Ted Vucurevich - Cadence Design Systems, Inc., San Jose, CA

Session 2

rm: N109-N110

SPECIAL SESSION: NANOMETER FUTURES

CHAIR: *Andrew B. Kahng - Univ. of California at San Diego, La Jolla, CA*
ORGANIZERS: *Andrew B. Kahng, Kurt Keutzer*

This session uncovers the cost and quality landmines that are inherent in the technology roadmap for nanometer silicon — and how the EDA and IC industries must plan to respond. The first talk identifies power as the key challenge to all aspects of quality and performance in nanometer technologies. Power-speed tradeoffs are analyzed at device, circuit and other levels. Leakage is the primary challenge to CMOS scaling, and area/delay/cost penalties may block scaling of today's leakage reduction techniques. Finally, power distribution raises issues regarding the viability of packaging and integration strategies. The second talk examines the consequences of production volumes, time-to-market and manufacturability: How will the billions of dollars to be spent on nanometer fablines affect the design-manufacturing interface? How must IC design respond to the future manufacturing cost structure? And how must IC technology roadmaps themselves adapt to nanometer economic realities?

2.1 Future Performance Roadblocks In Nanometer Design
Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*
2.2 IC Design In the High-Cost Nanometer Technologies Era
Wojciech Maly - *Carnegie Mellon Univ., Pittsburgh, PA*

Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Session 3

rm:N115-N117

SYSTEM-LEVEL CONFIGURABILITY: BUS INTERFACE AND PROCESSOR DESIGN

CHAIR: *Pieter van der Wolf* - Philips Research Lab., Eindhoven, The Netherlands

ORGANIZERS: *Kees Vissers, Kurt Keutzer*

This session presents technologies that enable and exploit system-level configurability, focusing on system bus networks, interfaces, and configurable processors. The first paper presents a novel high-performance protocol for system buses. The second paper addresses the design of interfaces that enable multi-clock and hybrid synchronous / asynchronous systems. The third paper presents tools for the customization of on-chip bus topologies. The last paper presents an approach for estimating design metrics (area, speed, and power), for a configurable processor IP core.

3.1 LOTTERYBUS: A New High-Performance Communication Architecture for System-on-Chip Designs

Kanishka Lahiri - *Univ. of California at San Diego, La Jolla, CA*
Anand Raghunathan, Ganesh Lakshminarayana - *NEC Corp., Princeton, NJ*

3.2 Robust Interfaces for Mixed-Timing Systems with Application to Latency-Insensitive Protocols

Tiberiu Chelcea, Steven M. Nowick - *Columbia Univ., New York, NY*

3.3S Latency-Driven Design of Multi-Purpose Systems-on-Chip

Milenko Drinic, Seapahn Meguerdichian, Darko Kirovski - *Univ. of California, Los Angeles, CA*

3.4S Estimation of Speed, Area, and Power of Parameterizable, Soft IP

Jagesh V. Sanghavi, Albert Wang - *Tensilica, Inc., Santa Clara, CA*

Session 4

rm: N119-N120

MAKING VERIFICATION MORE EFFICIENT

CHAIR: *Masahiro Fujita* - Univ. of Tokyo, Tokyo, Japan

ORGANIZERS: *Limor Fix, Timothy Kam*

With the current limitation in capacity and runtime, verification can be a bottleneck in a design flow. The research presented in this session targets improving the efficiency of verification. The first paper employs multiple engines including BDD-ATPG and 3-value simulation. A novel microprocessor architecture is verified with the proposed design-for-verifiability technique in the second paper. The third paper proposed how various verilog RTL constructs can be symbolically simulated.

4.1 Formal Property Verification by Abstraction Refinement with Formal Simulation and Hybrid Engines

Dong Wang - *Carnegie Mellon Univ., Pittsburgh, PA*
Pei-Hsin Ho, Jiang Long, James Kukula - *Synopsys, Inc., Beaverton, OR*
Yunshan Zhu, Tony Ma - *Synopsys, Inc., Mountain View, CA,*
Robert Damiano - *Synopsys, Inc., Beaverton, OR*

4.2 Scalable Hybrid Verification of Complex Microprocessors

Maher N. Mneimneh, Fadi A. Aloul, Saugata Chatterjee, Chris Weaver, Karem A. Sakallah, Todd Austin - *Univ. of Michigan, Ann Arbor, MI*

4.3 Symbolic RTL Simulation

Alfred Koelbl - *Technical Univ. of Munich, Munich, Germany*
James Kukula, Robert Damiano - *Synopsys, Inc., Beaverton, OR*

Session 5

rm: N107-N108

SoC AND HIGH-LEVEL DFT

CHAIR: *Yervant Zorian - LogicVision, Inc., San Jose, CA*

ORGANIZERS: *Anand Raghunathan, Irith Pomeranz*

This session starts with a paper addressing issues related to the VSIA/IEEE P1500 standard for SoC testing. The second paper deals with instruction-level DFT to support self-testing of SoC with processor cores. The third paper proposes a BIST-based DFT methodology using RTL testability analysis.

5.1 A Unified DFT Architecture for Use with IEEE 1149.1 and VSIA/IEEE P1500 Compliant Test Access Controllers

Bulent I. Dervisoglu - *Cadence Design Systems, Inc., San Jose, CA*

5.2 Instruction-Level DFT for Testing Processor and IP Cores in System-on-a-Chip

WeiCheng Lai, Tim Cheng - *Univ. of California, Santa Barbara, CA*

5.3 Test Strategies for BIST at the Algorithmic and Register-Transfer Levels

Kelly Ockunzzi - *IBM Corp., Burlington, VT*
Chris Papachristou - *Case Western Reserve Univ., Cleveland, OH*

Tuesday June 19

2:00 to 4:00

All speakers are denoted in bold

S – denotes short paper

Session 6

rm: N111-N114

PANEL: THE NEXT HDL: IF C++ IS THE ANSWER, WHAT WAS THE QUESTION?

CHAIR: *Rajesh K. Gupta* - Univ. of California, Irvine, CA
ORGANIZER: *Shishpal Rawat*

The focus of this panel is on issues surrounding use of C++ in modeling and the integration of silicon IP and system-on-chip designs. In the last two years there have been several announcements promoting C++ based solutions and of multiple consortia (SystemC, Cynapps, Accellera, SpecC) that represent increasing commercial interest both from tool vendors as well as perhaps expression of genuine needs from design houses. There are, however, serious questions about what value proposition a C++ based design methodology brings to the IC or system designer? What has changed in the modeling technology (and/or available tools) that gives a new capability? Is synthesis the right target? or Validation? Tester modeling or testbench generation? This panel brings together advocates and opponents from the design houses and tool developers to highlight the modeling advances.

PANELISTS:

Gérard Berry - Esterel Technologies, Villeneuve-Loubet, France
Ramesh Chandra - ST Microelectronics, San Diego, CA
Daniel Gajski - Univ. of California, Irvine, CA
Kris Konigsfeld - Intel Corp., Hillsboro, OR
Patrick Schaumont - IMEC, Leuven, Belgium
Ingrid Verbauwhede - Univ. of California, Los Angeles, CA

Session 7

rm: N109-N110

SPECIAL SESSION: DESIGN FOR SUBWAVELENGTH MANUFACTURABILITY: IMPACT ON EDA

CHAIR: *Frank Schellenberg - Mentor Graphics Corp., San Jose, CA*
ORGANIZERS: *Lars Liebman, Andrew B. Kahng*

Minimum feature sizes that are much smaller than stepper wavelengths stress the design flow and the design-manufacturing interface as never before. Already, optical proximity correction (OPC), phase-shifting masks (PSM), and pattern density control break traditional flows and reuse paradigms, and dramatically increase design cost. How must EDA change to meet this challenge? The first two papers present experiences and cost-benefit analysis of IDMs who have developed and deployed complete layout and verification methodologies at 150nm and below. The next three papers describe vendor experiences with OPC- and PSM-enabling tools and methodologies. The session will conclude with open Q&A for all presenters.

7.1 Reticle Enhancement Technology: Implications and Challenges for Physical Design

Warren Grobman, Ruoping Wang, Ruiqi Tian, Ertugrul Demircan, Matt Thompson, **Chi-Min Yuan** - *Motorola DigitalDNA Labs, Austin, TX*

7.2 Enabling Alternating Phase Mask Design for a Full Logic Gate Level

Lars Liebmann, Ioana Graur - *IBM Corp., Fishkill, NY*
Fook-Luen Heng, Jennifer Lund - *IBM Corp., Yorktown Heights, NY*

7.3S Layout Design Methodologies for Sub-Wavelength Manufacturing

Mike Rieger, Jeff Mayhew, Jiangwei Li - *Avant! Corp., Fremont, CA*

7.4S Production Adoption of OPC and the Impact on Design and Layout

F. M. Schellenberg, N. Cobb, Y. Granik - *Mentor Graphics Corp., San Jose, CA*
L. Capodieci, R. Socha - *ASML MaskTools, Santa Clara, CA*

7.5S A Practical Application of Full-Feature Alternating Phase-Shifting Technology for a Phase-Aware Standard-Cell Design Flow

Michel Cote, Philippe Hurat, Martin Lefebvre, Michael Sanie - *Numerical Technologies, Inc., San Jose, CA*

7.6S Open Session for Q & A

Session 8

rm: N115-N117

NEW IDEAS IN LOGIC SYNTHESIS

CHAIR: *Yusuke Matsunaga - Fujitsu Labs. Ltd., Kawasaki, Japan*

ORGANIZERS: *Timothy Kam, Masahiro Fujita*

The first paper introduces a new logic synthesis technique considering reliability issues of LSI. The remaining three papers discuss new algorithms in combinational logic synthesis targeting decomposition of incompletely specified logic functions, factoring of read-once functions, and logic synthesis with exclusive-o2 gates.

8.1 Layout-Driven Hot-Carrier Degradation Minimization Using Logic Restructuring Techniques

Jim Chang, Kai Wang, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*

8.2 An Algorithm for Bi-Decomposition of Logic Functions

Alan Mishchenko - *Portland State Univ., Portland, OR*
Bernd Steinbach - *Freiberg Univ. of Mining and Technology, Freiberg, Germany*
Marek Perkowski - *Portland State Univ., Portland, OR*

8.3 Factoring and Recognition of Read-Once Functions Using Cographs and Normality

Martin C. Golumbic, **Aviad Mintz** - *Bar Ilan Univ., Ramat Gan, Israel*
Udi Rotics - *Netanya Academic College, Netanya, Israel*

8.4 Logic Minimization Using Exclusive OR Gates

Valentina Ciriani - *Univ. di Pisa, Pisa, Italy*

Session 9

rm: N119-N120

ANALOG DESIGN AND MODELING

CHAIR: *Alper Demir - CeLight, Inc., Springfield, NJ*

ORGANIZERS: *Joel Phillips, Noel Menezes*

The first paper in this session presents a working design of a high-speed clock and data recovery circuit for optical networking applications. The remaining papers describe progress in a collection of analog CAD topics — stochastic analysis of data converters, partitioning of mixed-signal designs, and efficient analog symbolic analysis.

9.1 Student Design Contest: Design of Half-Rate Clock and Data Recovery Circuits for Optical Communication Systems

Jafar Savoj, Behzad Razavi - *Univ. of California, Los Angeles, CA*

9.2 A Novel Method for Stochastic Nonlinearity Analysis of a CMOS Pipeline ADC

David Goren, **Israel A. Wagner**, Eliyahu Shamsaev - *IBM Corp., Haifa, Israel*

9.3 Behavioral Partitioning in the Synthesis of Mixed Analog-Digital Systems

Sree Ganesan, Ranga Vemuri - *Univ. of Cincinnati, Cincinnati, OH*

9.4 Efficient DDD-Based Symbolic Analysis of Large Analog Circuits

Wim Verhaegen, Georges G. Gielen - *Katholieke Univ., Leuven, Belgium*

Session 10

rm: N107-N108

SCAN-BASED TESTING

CHAIR: *T. M. Mak - Intel Corp., Santa Clara, CA*

ORGANIZERS: *Anand Raghunathan, Tim Cheng*

This session deals with issues related to fault coverage improvement, test volume and test time reduction for scan-based designs. The first paper uses limited scan operations to improve random pattern fault coverage. The next three papers describe different compaction techniques. The last paper deals with a compression technique for test data and power reduction.

10.1 Random Limited-Scan to Improve Random Pattern Testing of Scan Circuits

Irith Pomeranz - *Purdue Univ., West Lafayette, IN*

10.2 Test Volume and Application Time Reduction Through Scan Chain Concealment

Ismet Bayraktaroglu, Alex Orailoglu - *Univ. of California at San Diego, La Jolla, CA*

10.3 An Approach to Test Compaction for Scan Circuits that Enhances At-Speed Testing

Irith Pomeranz - *Purdue Univ., West Lafayette, IN*
Sudhakar M. Reddy - *Univ. of Iowa, Iowa City, IA*

10.4S Generating Efficient Tests for Continuous Scan

Sying Jyan Wang, Sheng Nan Chiou - *National Chung-Hsing Univ., Taichung, Taiwan, ROC*

10.5S Combining Low-Power Scan Testing and Test Data Compression for System-on-a-Chip

Anshuman Chandra, Krishnendu Chakrabarty - *Duke Univ., Durham, NC*

Tuesday
June 19

4:30
to
6:00

All speakers are denoted in **bold**

S – denotes short paper

Session 11

rm: **N111-N114**

PANEL: YOUR CORE – MY PROBLEM? INTEGRATION AND VERIFICATION OF IP

CHAIR: *Gabe Moretti* - EDN Magazine, Niwot, CO
ORGANIZERS: *Nanette Collins, Gabe Moretti, Dave Kelf*

As the popularity of reusing existing designs — or Intellectual Property (IP) — continues to grow, design challenges escalate. The most time-consuming and critical part of IP design and reuse is verifying that it will work as designed and as the user intends. Designers are pushing the limits of IP for new, distinctive and innovative applications. With this innovation come problems that will need creative solutions. Product verification, for example, will become more and more important in ensuring the correctness of designs. Over the years, various solutions have come on the market, all seemingly useful, but none reducing the time or manpower it takes to verify a design. With designs becoming increasingly more complex with each new project and verification consuming up to 70% a design cycle, something must be done to alleviate the bottleneck. The panel will look at various alternatives for IP verification today, including universal simulation, hardware acceleration, formal verification, and semi-formal verification. Panelists, who are experienced designers and representatives of organizations offering EDA tools to beat the verification bottleneck will work toward identifying the methodology best suited for IP design.

PANELISTS:

Tom Anderson - 0-In Design Automation, San Jose, CA
Janick Bergeron - Qualis Design Corp., Lake Oswego, OR
Ashish Dixit - Tensilica, Inc., Santa Clara, CA
Peter Flake - Co-Design Automation, Inc., Los Altos, CA
Tim Hopes - ARM, Maidenhead, UK
Ramesh Narayanaswamy - Tharas Systems Inc., Santa Clara, CA

Session 12

rm: **N109-N110**

SPECIAL SESSION: CONFIGURABLE COMPUTING: RECONFIGURING THE INDUSTRY

CHAIR: *Diederik Verkest* - IMEC, Leuven, Belgium
ORGANIZERS: *Diederik Verkest, Kurt Keutzer*

Cost effective systems use specialization to optimize factors such as power consumption, processing throughput, flexibility, or combinations thereof. Reconfiguration has been proposed as a mechanism to create run-time specialization. This session will address the concept of reconfiguration at different hierarchical levels, the architectural aspects of reconfigurable computing, the link between application domain and reconfigurability needs, and the design techniques supporting reconfiguration.

12.1 The Reconfiguration Hierarchy: From Systems to Circuits
Patrick Schaumont - *IMEC, Leuven, Belgium*
Ingrid Verbauwhede, Majid Sarrafzadeh - *Univ. of California, Los Angeles, CA*
Kurt Keutzer - *Univ. of California, Berkeley, CA*

12.2 ReConfigurable Computing In Wireless
Bill Salefski, Levent Caglar - *Chameleon Systems, Inc., San Jose, CA*

12.3 Hardware/Software Instruction Set Configurability for System-on-Chip Processors
Albert Wang, Chris Rowen, Dror Mayden, Earl Killian - *Tensilica, Inc., Santa Clara, CA*

Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Session 13

rm: N115-N117

INTERCONNECT DESIGN OPTIMIZATION

CHAIR: *Martin D. F. Wong - Univ. of Texas, Austin, TX*
ORGANIZERS: *Jason Cong, Louis Scheffer, Patrick Groeneveld*

This session presents various approaches to the design and planning of interconnect. The first two papers deal with global wiring optimization, while the third paper addresses the crosstalk minimization problem. The final paper presents new results on optimal switchbox interconnect design for FPGAs.

13.1 A Practical Methodology for Early Buffer and Wire Resource Allocation

Charles J. Alpert, Jiang Hu - *IBM Corp., Austin, TX*
Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*
Paul Villarrubia - *IBM Corp., Austin, TX*

13.2S Creating and Exploiting Flexibility in Steiner Trees

Elaheh Bozorgzadeh - *Univ. of California, Los Angeles, CA*
Ryan Kastner - *Univ. of California, Santa Monica, CA*
Majid Sarrafzadeh - *Univ. of California, Los Angeles, CA*

13.3S Simultaneous Shield Insertion and Net Ordering for Coupled RLC Nets Under Explicit Noise Constraint

Kevin Lepak, Irwan Luwandi, **Lei He** - *Univ. of Wisconsin, Madison, WI*

13.4 On Optimum Switch Box Designs for 2-D FPGAs

Hongbing Fan - *Univ. of Victoria, Victoria, BC, Canada*
Jiping Liu - *Univ. of Lethbridge, Lethbridge, AB, Canada*
Yu Liang Wu, Chak Chung Cheung - *Chinese Univ. of Hong Kong, Hong Kong, China*

Session 14

rm: N119-N120

POWER ESTIMATION TECHNIQUES

CHAIR: *Massoud Pedram - Univ. of Southern California, Los Angeles, CA*
ORGANIZERS: *Donatella Sciuto, Kazutoshi Wakabayashi*

The first two papers of the session introduce two models for evaluating power consumption in combinational circuits. The first paper estimates switching activities by capturing complex dependencies among signals using probabilistic techniques. The second paper deals with power sensitivity estimation of a presynthesized circuit. Finally, the third paper considers a different level of abstraction by presenting a software energy estimation methodology considering current consumption.

14.1 Dependency Perserving Probabilistic Modeling of Switching Activity Using Bayesian Networks

Sanjukta Bhanja, Nagarajan Ranganathan - *Univ. of South Florida, Tampa, FL*

14.2 A Static Estimation Technique of Power Sensitivity in Logic Circuit

Taewhan Kim - *KAIST, Taejon, Korea*
Kiseok Chung - *Intel Corp., Santa Clara, CA*
C. L. Liu - *National Tsing-Hua Univ., Hsinchu, Taiwan, ROC*

14.3 JouleTrack - A Web Based Tool for Software Energy Profiling

Amit Sinha, Anantha P. Chandrakasan - *Massachusetts Institute of Tech., Cambridge, MA*

Session 15

rm: N107-N108

FUNCTIONAL VALIDATION BASED ON BOOLEAN REASONING (BDD, SAT)

CHAIR: *Limor Fix - Intel Semiconductors Ltd., Haifa, Israel*
ORGANIZERS: *Masahiro Fujita, Timothy Kam*

Many tasks in EDA, such as equivalence checking, property checking, logic synthesis, and false path analysis are based on Boolean Function analysis using BDD Technology and SAT solvers. In this session, state of the art SAT solvers will be presented. The benefit of circuit information for optimizing SAT and BDD will be discussed, and the use of symbolic simulation for partial equivalence checking will be demonstrated.

15.1 Effective Use of Boolean Satisfiability Procedures in the Formal Verification of Superscaler and VLIW Microprocessors

Miroslav N. Velev, Randal E. Bryant - *Carnegie Mellon Univ., Pittsburgh, PA*

15.2 Circuit-Based Boolean Reasoning

Andreas Kuehlmann - *Cadence Berkeley Labs., Berkeley, CA*
Malay K. Ganai - *Univ. of Texas, Austin, TX*
Viresh Paruthi - *IBM Corp., Austin, TX*

15.3 Checking Equivalence for Partial Implementations

Christoph Scholl, Bernd Becker - *Univ. of Freiburg, Freiburg, Germany*

Wednesday June 20

8:30 to 10:00

All speakers are denoted in bold

S – denotes short paper

Session 16

rm: N111-N114

SPECIAL SESSION: VERIFICATION: LIFE BEYOND ALGORITHMS

CHAIR: *Carl Pixley - Motorola, Inc., Austin, TX*
ORGANIZER: *Carl Pixley*

The speakers will address the nuts and bolts of commercial verification projects, describing the various techniques used, the resources required and the effectiveness of different techniques. The general education of engineers in verification is addressed in the final paper.

16.1 Validating the Intel® Pentium® 4 Microprocessor
Bob Bentley - *Intel Corp., Hillsboro, OR*

16.2 Nuts and Bolts of Core and SoC Verification
Ken Albin - *Motorola, Inc., Austin, TX*

16.3 Teaching Future Verification Engineers – The Forgotten Side of Logic Development
Bruce Wile - *IBM Corp.*, Poughkeepsie, NY
Fusun Ozguner, Duane Marhefka - *Ohio State Univ., Columbus, OH*
Lyle Hanrahan - *IBM Corp., Rochester, MN*
Jennifer Strofer - *IBM Corp., Austin, TX*

Session 17

rm: N109-N110

SPECIAL SESSION: DISSECTING AN EMBEDDED SYSTEM: LESSONS FROM BLUETOOTH

CHAIR: *Jan Rabaey - Univ. of California, Berkeley, CA*
ORGANIZERS: *Jan Rabaey, Anantha Chandrakasan*

Ad-hoc wireless networking based on the Bluetooth Standard is one of the hottest topics in wireless today. The design process and methodology of a leading-edge bluetooth chip set will be presented and analyzed. The tough specifications of Bluetooth and its complexity necessitate advanced design verification and test techniques, which are the focus of this session.

17.1 Bluetooth IP-Selection Criteria and Reusable Baseband IP, a Case Study
Torbjorn Grahm - *Ericsson Tech. Licensing AB, Lund, Sweden*

17.2 One-Chip Bluetooth Challenges
Paul van Zeijl - *Ericsson EuroLab., Emmen, The Netherlands*

Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Session 18

rm: N115-N117

ALGORITHMIC AND COMPILER TRANSFORMATIONS FOR HIGH-LEVEL SYNTHESIS

CHAIR: *Hiroto Yasuura - Kyushu Univ., Fukuoka, Japan*
ORGANIZERS: *Kazutoshi Wakabayashi, Rajesh K. Gupta*

The quality of synthesized circuits is a major concern for many high-level synthesis solutions. This session addresses techniques that work with HLS algorithms to improve synthesis results. The first paper presents global transformations for controller synthesis. The second and third papers examine techniques using parallelizing compilers that directly effect HLS solutions. The last paper examines arithmetic-level optimizations.

18.1 Transformations for the Synthesis and Optimization of Asynchronous Distributed Control

Michael Theobald, Steven M. Nowick - *Columbia Univ., New York, NY*

18.2S Speculation Techniques for High Level Synthesis of Control Intensive Designs

Sumit Gupta, Nick O. Savoiu, Sunwoo Kim, Nikil Dutt, Rajesh K. Gupta, Alexandru Nicolau - *Univ. of California, Irvine, CA*

18.3S Parallelizing DSP Nested Loops on Reconfigurable Architectures Using Data Contexed Switching

Kiran K. Bondalapati - *Univ. of Southern California, Los Angeles, CA*

18.4 Using Symbolic Algebra in Algorithmic Level DSP Synthesis

Armita Peymandoust, Giovanni De Micheli - *Stanford Univ., Stanford, CA*

Session 19

rm: N119-N120

GATE DELAY CALCULATION

CHAIR: *Satya Pullela - Monterey Design Systems, Sunnyvale, CA*
ORGANIZERS: *Jaijeet Roychowdhury, Joel Phillips*

This session has three papers on gate delay calculation. The first paper uses BDDs to quickly explore the space of switching transitions, enabling accurate delay simulation of only a few sets of transitions. The second paper derives an empirical delay model for a NAND gate, accounting for simultaneous switching and relative input positions, and outlines applications to timing analysis and incremental timing refinement. The third paper analysis the effect of power supply variations on gate delay with three techniques, obtaining increasingly tight upper bounds on worst-case delay.

19.1 Computing Logic-Stage Delays Using Circuit Simulation and Symbolic Elmore Analysis

Clay McDonald, Randal E. Bryant - *Carnegie Mellon Univ., Pittsburgh, PA*

19.2 A New Gate Delay Model for Simultaneous Switching and Its Applications

LiangChi Chen, Sandeep K. Gupta, Melvin A. Breuer - *Univ. of California, Los Angeles, CA*

19.3 Static Timing Analysis Including Power Supply Noise Effect on Propagation Delay in VLSI Circuit

Geng Bai, Sudhakar Bobba, Ibrahim N. Hajj - *Univ. of Illinois, Urbana, IL*

Session 20

rm: N107-N108

MEMORY, BUS AND CURRENT TESTING

CHAIR: *Magdy S. Abadir - Motorola, Inc., Austin, TX*
ORGANIZERS: *Irith Pomeranz, Tim Cheng*

This session includes a paper on test generation and test scheduling for multiport memories, papers on bus testing and a paper on fault characterization and DFT for CMOS/BiCMOS circuits. In the area of bus testing, the papers cover IDDT testing and the use of embedded processor cores for interconnect crosstalk defects.

20.1 Simulation-Based Test Algorithm Generation and Port Scheduling for Multi-Port Memories

ChiFeng Wu, ChihTsun Huang, KuoLiang Cheng, ChihWea Wang, ChengWen Wu - *National Tsing-Hua Univ., Hsinchu, Taiwan, ROC*

20.2 Improving Bus Test Via IDDT and Boundary Scan

Shiyu Yang - *Intel Corp., Hillsboro, OR*
Chris Papachristou, Massood Tabib-Azar - *Case Western Reserve Univ., Cleveland, OH*

20.3S Design-for-Testability for Detecting IDDQ Faults and Fault Characterizations in CMOS/BICMOS Circuits

Kaamran Raahemifar - *Ryerson Polytechnic Univ., Toronto, ON, Canada*
Majid Ahmadi - *Univ. of Windsor, Windsor, ON, Canada*

20.4S Testing for Interconnect Crosstalk Defects Using On-Chip Embedded Processor Core

Li Chen, Xiaoliang Ba, Sujit Dey - *Univ. of California at San Diego, La Jolla, CA*

Wednesday
June 20

10:30
to
12:00

All speakers are denoted in **bold**

S – denotes short paper

PLENARY PANEL

rm: N109-N114

EMBEDDED SYSTEM DESIGN: THE REAL STORY

CHAIR: *Alberto L. Sangiovanni-Vincentelli - Univ. of California, Berkeley, CA*

ORGANIZERS: *Randy Harr, Wayne Wolf*

PRESENTERS: *Augusto de Oliveira - Philips, Sunnyvale, CA*
Roger Fordham - Motorola, Inc., Schaumberg, IL
Mark Pinto - Agere Systems, Allentown, PA
Jim Ready - MontaVista Software, Sunnyvale, CA
Fabio Romeo - Magneti Marelli, Torino, Italy

Description: Every object in common use tomorrow will have an electronic component that, we hope, will enhance its functionality, its reliability, and its safety. An automobile, a cellular phone, and a home are already complex electronic systems and will become more so. The billion-transistor ASIC complexity that has been touted as the challenge for methodologies and EDA does pale in comparison when mixed with the complexity of embedded systems. Embedded systems are heterogeneous, they are connected to networks, they have multiple and conflicting requirements of cost, performance, functionality, safety, and time to market. Being late to the market for just a few weeks may mean the loss of hundreds of millions of dollars, but being wrong can be tragic.

The entire electronics industry has been restructuring to face the challenges of embedded system design and production. Less frequently are such designs carried out by a single company. With outsourcing of both design and manufacturing, each contributor focuses on its core competency. Hence, the interfaces among system, IP providers, semiconductor-design companies and manufacturing companies are becoming the pivotal points to understand for the future of the electronics industry.

Several ideas are emerging to cope with complexity, time-to-market and cost of designing these pervasive embedded systems and their integrated circuits. Platform-based design, for example, has become an important design style and, if well implemented, is essential to providing reuse of software and hardware components over two or more possibly disparate design projects as well as a clean interface among system, IP and semiconductor companies. Since the flexibility of a platform is strictly connected to the re-usability of the programmable and reconfigurable parts, reusable software design, crystal ball architecture selection and complex configuration methods are becoming essential ingredients of embedded system design. Embedded software traditionally has had different characteristics when compared with traditional large software systems encountered in data base applications and computer systems. Real-time reactions to the environment and complex signal processing are typical for most applications of embedded systems such as cellular phones and engine controllers. The real-time requirements pose the most interesting challenges to embedded software design. Indeed the choice of implementation of a function as a hardware module or a software program is the result of trade-offs involving time-to-market, power consumption, performance and cost.

The participants in this panel are among the key enablers of the new embedded system design frontier and will address:

- The issues associated with critical markets now dependent upon embedded systems: automotive, cellular and consumer electronics.
- The embedded software design challenges and trends in view of the latest research and industrial offerings.
- Platform-based design as an effective way of reducing risk and complexity of the overall design process as well as sustaining the electronics supply chain.

Alberto L. Sangiovanni-Vincentelli
Alberto Sangiovanni-Vincentelli is Professor of Electrical Engineering and Computer Sciences at the University of California at Berkeley, where he serves on the Advisory Board of the Lester Center of the Haas School of Business and of the Center for Western European Studies, and is a member of the Berkeley Roundtable of the International Economy. He is a co-founder of Cadence and Synopsys and serves on the boards of a variety of new and established companies. He is author of over 500 papers and eleven books, and is a Fellow of the IEEE and a Member of the National Academy of Engineering.

Augusto de Oliveira
Augusto de Oliveira is currently Chief Architect for the Consumer Systems Business Unit of Philips Semiconductors, responsible for digital video platform software and hardware architectures. He previously held technical and management positions with Philips in Brazil, The Netherlands and the United States, including manager of the Philips MIPS Technology Center and CTO and Systems Development Manager for the Handheld Computing Group. He has also worked at Philips Research and Philips Business Communications.

Roger Fordham
Roger Fordham is Director of Performance Excellence for the Motorola Global Software Group and has the responsibility for advanced software development environments for Motorola's communications businesses and for establishing the software business and engineering culture and development environment in software development centers worldwide. He has worked for Motorola on four continents, establishing and directing the company's software development business and lecturing on software development, engineering, and culture. He is a Fellow of the Institute of Engineers Australia and has been active in national and international software engineering standards activities and educational endeavors.

Mark Pinto
Mark Pinto is Chief Technical Officer of Agere Systems, formerly the Microelectronics Group of Lucent Technologies and is responsible for technology strategy and research activities in electronic and optoelectronic devices, integrated circuit design, and software and systems. He is also Vice President of Platform Technologies, leading the company's efforts to deliver system-on-a-chip hardware cores, communications software elements, development software, methodologies, tools, models and analysis. He has authored more than 150 journal and professional conference papers and has eight patents in semiconductor devices. He is a Fellow of the IEEE.

Jim Ready
Jim Ready is founder, President and CEO of MontaVista Software, which provides the Linux operating system to the embedded systems market through its Hard Hat Linux flagship product, and offers embedded systems expertise to the open source Linux community. He was co-founder and president of Ready Systems, which developed the first commercially viable real time operating system product, and CTO of its successor, Microtec Research, which was later acquired by Mentor Graphics. He has over 25 years of technical and entrepreneurial experience and is a recognized authority in the embedded systems and real-time software industry.

Fabio Romeo
Fabio Romeo is Executive Vice President of Magneti-Marelli corporate, and President and General Manager of the Electronic System Division, which manufactures electronic products for the corporation and develops dashboard and infotelematics products. He previously held positions at Politecnico di Milano and at Honeywell Information Systems, Italy. He has been active in the development of embedded systems for automotive applications, particularly in the definition of design methodologies necessary to guarantee reduced time-to-market, hardware-software independence, and increased quality levels in software and hardware.

Wednesday June 20

2:00 to 4:00

All speakers are denoted in bold

S – denotes short paper

Session 21

rm: N111-N114

PANEL: (WHEN) WILL FPGAS KILL ASICS?

CHAIR: *Rob A. Rutenbar - Carnegie Mellon Univ., Pittsburgh, PA*
ORGANIZER: *Rob A. Rutenbar*

There was a time in the dim historical past when foundries actually made ASICs with only 5000 to 50,000 logic gates. But FPGAs and CPLDs conquered those markets and pushed ASIC silicon toward opportunities with more logic, volume, and speed. Today's largest FPGAs approach the few-million-gate size of a typical ASIC design,and continue to sprout embedded cores, such as CPUs, memories, and interfaces. And given the risks of non-working nanometer silicon, FPGA costs and time-to-market are looking awfully attractive. So, will FPGAs kill ASICs? ASIC technologists certainly think not. ASICs are themselves sprouting patches of programmable FPGA fabric, and pushing new realms of size and especially speed. New tools claim to have tamed the convergence problems of older ASIC flows. Is the future to be found in a market full of FPGAs with ASIC-like cores? ASICs with FPGA cores? Other exotic hybrids? Our panelists will share their disagreements on these prognostications.

PANELISTS:

Max Baron - Microprocessor Report, Sunnyvale, CA
Thomas Daniel - LSI Logic Corp., Milpitas, CA
Rajeev Jayaraman - Xilinx, Inc., San Jose, CA
Zvi Or-Bach - eASIC, San Jose, CA
Jonathan Rose - Altera Corp., Univ. of Toronto, Toronto, ON, Canada
Carl Sechen - Univ. of Washington, Seattle, WA

Session 22

rm: N109-N110

SPECIAL SESSION: INDUCTANCE 101 AND BEYOND

CHAIR: *Phillip Restle - IBM Corp., TJ Watson Research Ctr., Yorktown Heights, NY*
ORGANIZERS: *Joel Phillips, Noel Menezes*

Inductance issues create new signal integrity and delay problems for multigigahertz designs. A basic introduction to the cause and effect of inductance in VLSI circuits is presented along with an industry approach to handling inductance effects in designs. Two final papers present strategies for on-chip inductance modeling.

22.1 Inductance 101: Modeling and Extraction
Michael Beattie, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

22.2 Inductance 101: Analysis and Design Issues
Kaushik Gala, David Blaauw, Junfeng Wang, Vladimir Zolotov, Min Zhao - *Motorola, Inc., Austin, TX*

22.3 Modeling Magnetic Coupling for Gigascale Interconnect
Michael W. Beattie, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

22.4 Min/Max On-Chip Inductance Models and Delay Metrics
Yi Chang Lu - *Stanford Univ., Stanford, CA*
Mustafa Celik, Tak Young - *Monterey Design Inc., Sunnyvale, CA*
Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Session 23

rm: N115-N117

MEMORY OPTIMIZATION TECHNIQUES FOR DSP PROCESSORS

CHAIR: *Daniel Connors - Univ. of Colorado, Boulder, CO*
ORGANIZERS: *Dirk Grunwald, Marco Di Natale*

These papers describe mechanisms to reduce memory size or bandwidth for embedded applications. The first paper presents compiler algorithms to exploit multiword memory transfer. The second shows how to reduce address register changes for common DSPs and the last two papers show how to automatically reduce the total memory needed by applications.

23.1 Utilizing Memory Bandwidth in DSP Embedded Processors

Catherine H. Gebotys - *Univ. of Waterloo, Waterloo, ON, Canada*

23.2 Address Code Generation for Digital Signal Processors

Sathishkumar Udayanarayanan - *Conexant Systems Inc., Tustin Ranch, CA*
Chaitali Chakrabarti - *Arizona State Univ., Tempe, AZ*

23.3 Reducing Memory Requirements of Nested Loops for Embedded Systems

J. Ramanujam - *Louisiana State Univ., Baton Rouge, LA*
Mahmut Kandemir - *Penn State Univ., University Park, PA*
Jinpyo Hong, Ashish Narayan - *Louisiana State Univ., Baton Rouge, LA*

23.4 Detection of Partially Simultaneously Alive Signals in Storage Requirement Estimation for Data Intensive Applications

Per G. Kjeldsberg - *Norwegian Univ. of Science and Tech., Trondheim, Norway*
Francky Catthoor - *IMEC, Leuven, Belgium*
Einar J. Aas - *Norwegian Univ. of Science and Tech., Trondheim, Norway*

Session 24

rm: N119-N120

TECHNOLOGY DEPENDENT LOGIC SYNTHESIS

CHAIR: *Peichen Pan - APLUS Design Technologies, Inc., Los Angeles, CA*
ORGANIZERS: *Jason Cong, Malgorzata Marek-Sadowska*

This session introduces us to power problems in technology dependent synthesis. The first paper describes an idea to speed up structural mapping. The second paper introduces some of the issues of incorporating domino circuitry in technology mapping. Latch and latency control and optimization during wave steering is the topic of the third paper. Paper four describes the problem of two level clustering in the context of FPGA synthesis.

24.1 A New Structural Pattern Matching Algorithm for Technology Mapping

Min Zhao, David Blaauw- *Motorola, Inc., Austin, TX*
Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

24.2 Technology Mapping for SOI Domino Logic Incorporating Solutions for the Parasitic Bipolar Effect

Arvind K. Karandikar, Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

24.3 Latency and Latch Count Minimization in Wave Steered Circuits

Amit Singh, **Arindam Mukherjee**, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*

24.4 Performance-Driven Multi-Level Clustering with Application to Hierarchical FPGA Mapping

Jason Cong, **Michail Romesis** - *Univ. of California, Los Angeles, CA*

Session 25

rm: N107-N108

COLLABORATIVE AND DISTRIBUTED DESIGN FRAMEWORKS

CHAIR: *Yi-Hung Chee - Intel Corp., Santa Clara, CA*
ORGANIZERS: *Noel Menezes, Vivek Tiwari*

The use of collaborative frameworks for expediting design tasks is receiving increased attention due to the increasing complexity of current ICs. The first paper deals with a novel approach to design process management while the second paper presents a universal client with a user-configurable GUI for distributed design. A collaborative framework for training and design, and an object-oriented framework for specification and synthesis are described in the final papers.

25.1 Application of Constraint-Based Heuristics in Collaborative Design

Juan Antonio Carballo - *IBM Corp., Austin, TX*
Stephen W. Director - *Univ. of Michigan, Ann Arbor, MI*

25.2 A Universal Client for Distributed Networked Design and Computing

Franc Brglez, Hemang Lavana - *N. Carolina State Univ., Raleigh, NC*

25.3 Hypermedia-Aided Design

Darko R. Kirovski, **Miodrag Potkonjak** - *Univ. of California, Los Angeles, CA*

25.4 A Framework for Object Oriented Hardware Specification, Verification, and Synthesis

Tommy Kuhn, **Tobias Oppold**, Markus Winterholer, Wolfgang Rosenstiel - *Univ. of Tuebingen, Tuebingen, Germany*
Marc Edwards - *Cisco Systems, Research Triangle Park, NC*
Yaron Kashai - *Verisity Design, Inc., Mountain View, CA*

Wednesday June 20

4:30 to 6:00

All speakers are denoted in bold

S – denotes short paper

Session 26

rm: N111-N114

PANEL: WHEN WILL THE ANALOG DESIGN FLOW CATCH UP WITH DIGITAL METHODOLOGY?

CHAIR: *Georges Gielen - Katholieke Univ., Leuven, Belgium*
ORGANIZERS: *Mike Sottak, Mike Murray, Linda Kaye*

Despite the fact that more and more electronic design is comprised of analog and mixed signal content, the design flows and methodologies in this area are lagging behind the pace of innovation in digital design. For sure, analog designers are in shorter supply, but this only makes the need for improvements and efficiency that much greater. Only of late have we seen production-worthy attempts at functions such as analog synthesis and optimization reach the market. What is needed in today's analog design flow? What are the key technologies that are missing? How does the existing "food chain" need to work together to drive greater efficiencies? A distinguished panel of suppliers and users will analyze these issues and project future trends.

PANELISTS:

Mar Hershenson - Barcelona Design, Sunnyvale, CA
Ken Kundert - Cadence Design Systems, Inc., San Jose, CA
Phillipe Magarshack - ST Microelectronics, Crolles, France
Akira Matsuzawa - Matsushita, Osaka, Japan
Ronald Rohrer - Neolinear, Inc., Pittsburgh, PA
Ping Yang - TSMC, Richardson, TX

Session 27

rm: N109-N110

SPECIAL SESSION: CLOSING THE GAP BETWEEN ASIC AND CUSTOM: DESIGN EXAMPLES

CHAIR: *Bryan Ackland - Lucent Technologies, Bell Labs., Holmdel, NJ*
ORGANIZER: *Kenji Yoshida*

A significant performance gap exists between integrated circuits designed in a custom methodology, and those designed in an ASIC (RTL synthesis) methodology. DAC hosted a session last year that focused on techniques to bridge this gap. This year's session looks at real circuit examples that have successfully done so.

27.1 Achieving 550Mhz in an ASIC Methodology

D. Chinnery, Kurt Keutzer, B. Nikolic - *Univ. of California, Berkeley, CA*

27.2 A Semi-Custom Design Flow in High-Performance Microprocessor Design

Gregory A. Northrop, Pong-Fei Lu- *IBM Corp., TJ Watson Research Ctr., Yorktown Heights, NY*

27.3 Reducing the Frequency Gap Between ASIC and Custom Designs

Stephen E. Rich, Matthew J. Parker, Jim Schwartz - *Intel Corp., Hillsboro, OR*

Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Session 28

rm: N115-N117

ENERGY AND FLEXIBILITY DRIVEN SCHEDULING

CHAIR: *Marco Di Natale - Univ. of Pisa, Pisa, Italy*
ORGANIZERS: *Donatella Sciuto, Luciano Lavagno*

This session looks at several applications of static scheduling in the context of real time embedded systems. The first paper presents a voltage scheduling algorithm based on static timing analysis that controls the supply voltage to exploit all available slack. The second paper takes battery characterization into account to optimally schedule tasks in a real time embedded system. The third paper discusses how to implement new functionality on an already existing system such that running applications are not disturbed.

28.1 Low-Energy Intra-Task Voltage Scheduling Using Static Timing Analysis

Dongkun Shin, Jihong Kim - *Seoul National Univ., Seoul, Korea*
Seongsoo Lee - *Ewha Womans Univ., Seoul, Korea*

28.2 Battery-Aware Static Scheduling for Distributed Real-Time Embedded Systems

Jiong Luo, Niraj Jha - *Princeton Univ., Princeton, NJ*

28.3 An Approach to Incremental Design of Distributed Embedded Systems

Paul Pop, Petru Eles, Traian Pop, Zebo Peng - *Linkoping Univ., Linkoping, Sweden*

Session 29

rm: N119-N120

REPRESENTATION AND OPTIMIZATION FOR DIGITAL ARITHMETIC CIRCUITS

CHAIR: *Miodrag Potkonjak - Univ. of California, Los Angeles, CA*
ORGANIZERS: *Kazutoshi Wakabayashi, Rajesh K. Gupta*

Optimization of arithmetic operations is crucial for many signal processing applications and more generally for datapath circuits in broader applications. The first paper in this session presents a novel signal representation for carry-save arithmetic optimizations across register boundaries. The second paper examines precision and signal clustering for improved data path designs. The last paper presents an approach for digital filter synthesis using the minimal signed digit representations.

29.1 Signal Representation Guided Synthesis Using Carry-Save Adders For Synchronous Circuits

Zhan Yu - *Univ. of California, Los Angeles, CA*
MengLin Yu - *Lucent Technologies, Holmdel, NJ*
Alan N. Willson Jr. - *Univ. of California, Los Angeles, CA*

29.2 Improved Merging of Datapath Operators Using Information Content and Required Precision Analysis

Anmol Mathur, Sanjeev Saluja - *Cadence Design Systems, Inc., San Jose, CA*

29.3 Digital Filter Synthesis Based on Minimal Signed Digit Representation

In Cheol Park, **Hyeong Ju Kang** - *KAIST, Taejeon, Korea*

Session 30

rm: N107-N108

TECHNIQUES FOR IP PROTECTION

CHAIR: *Ian Mackintosh - Sonics Inc., Mountain View, CA*
ORGANIZERS: *Kenji Yoshida, Majid Sarrafzadeh*

The first three papers propose three new techniques for enabling watermarking of hardware IP. They introduce a technique for public authentication of hardware IP, an optimal watermarking technique with respect to credibility and a watermarking technique for partitioning. The last paper introduces a technique for measuring how many IC's are produced for a given licensed design.

30.1 Publicly Detectable Techniques for the Protection of Virtual Components

Gang Qu - *Univ. of Maryland, College Park, MD*

30.2 Watermarking of SAT Using Combinatorial Isolation Lemmas

Rupak Majumdar, **Jennifer L. Wong** - *Univ. of California, Los Angeles, CA*

30.3S Watermarking Graph Partitioning Solutions

Miodrag Potkonjak, Greg Wolfe - *Univ. of California, Los Angeles, CA*

30.4S Hardware and Software Metering

Farinaz Koushanfar - *Univ. of California, Los Angeles, CA*
Gang Qu - *Univ. of Maryland, College Park, MD*

Thursday June 21

8:30 to 10:00

All speakers are denoted in bold

S – denotes short paper

Session 31

rm: N111-N114

SPECIAL SESSION: VISUALIZATION AND ANIMATION FOR VLSI DESIGN

CHAIR: *Chandu Visweswariah - IBM Corp., TJ Watson Research Ctr., Yorktown Heights, NY*

ORGANIZERS: *Chandu Visweswariah, Majid Sarrafzadeh*

This visually rich session will demonstrate the use of modern visualization and animation for dealing with large amounts of data to generate intuition about circuit behavior, large layouts or complex algorithms. These visualization methods are suprisingly accessible and easy to use. Eye-popping animation and visualization methods for understanding DSM interconnects, clock distribution networks, large VLSI layouts and various CAD-related algorithms will be shown.

31.1 Technical Visualizations in VLSI Design

Phillip Restle - *IBM Corp., TJ Watson Research Ctr., Yorktown Heights, NY*

31.2 Using Texture Mapping with Mipmapping to Render a VLSI Layout

Jeffrey M. Solomon, Mark A. Horowitz - *Stanford Univ., Stanford, CA*

31.3 Web-Based Algorithm Animation

Marc Njork - *Compaq Systems Research Ctr., Palo Alto, CA*

Session 32

rm: N109-N110

APPLICATION-SPECIFIC CUSTOMIZATION FOR SYSTEMS-ON-A-CHIP

CHAIR: *Kees Vissers - Trimedia Technologies Inc., Milpitas, CA*

ORGANIZERS: *Kurt Keutzer, Dirk Grunwald*

This session examines a number of ways in which systems-on-a-chip can be adapted or customized for particular applications. The first paper looks at tailoring processor architectures for media applications. The second looks at exploring a family of multiprocessor architectures for communication problems. The third paper looks at customizations for power management.

32.1 Extending the Scope of Embedded Processors in Codesigns Through Microarchitectural Customizations

Peter Petrov, Alex Orailoglu - *Univ. of California at San Diego, La Jolla, CA*

32.2 Automatic Generation of Application-Specific Architectures for Heterogeneous Multiprocessor System-on-Chip

Damien Lyonnard, Sungjoo Yoo, Amer Baghdadi, Ahmed A. Jerraya - *TIMA Lab., Grenoble, France*

32.3 Dynamic Voltage Scaling for Portable Systems

Tajana Simunic - *Stanford Univ., Stanford, CA*

Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Session 33

rm: N115-N117

SATISFIABILITY SOLVERS AND TECHNIQUES

CHAIR: *Karem Sakallah - Univ. of Michigan, Ann Arbor, MI*
ORGANIZERS: *Andrew B. Kahng, Kurt Keutzer, Limor Fix*

Boolean satisfiability techniques have been used successfully in a variety of EDA applications such as formal verification, testing and timing analysis. This session presents new and advanced satisfiability solvers and techniques that dramatically advance the performance of Boolean Satisfiability engines, and extend their scope to incremental formulations.

33.1 Engineering a (Super?) Efficient SAT Solver

Matthew W. Moskewicz - *Univ. of California, Berkeley, CA*
Conor F. Madigan - *Massachusetts Institute of Tech., Boston, MA*
Ying Zhao, Lintao Zhang, Sharad Malik - *Princeton Univ., Princeton, NJ*

33.2 Dynamic Detection and Removal of Inactive Clauses in SAT with Application in Image Computation

Aarti Gupta, Anubhav Gupta, Zijiang Yang, Pranav N. Ashar - *NEC USA, Princeton, NJ*

33.3S SATIRE: A New Incremental Satisfiability Engine

Jesse P. Whittemore, Joonyoung Kim, Karem A. Sakallah - *Univ. of Michigan, Ann Arbor, MI*

33.4S A Framework on Low Complexity Static Learning

Emil I. Gizdarski, Hideo Fujiwara - *Nara Institute of Science and Tech., Ikoma, Japan*

Session 34

rm: N119-N120

POWER AND INTERCONNECT ANALYSIS

CHAIR: *L. Miguel Silveira - INESC/IST, Lisboa, Portugal*
ORGANIZERS: *Joel Phillips, Mustafa Celik*

This session features papers in power issues — energy dissipation of interconnect, power network analysis and optimization. A final contribution presents a method for high-frequency inductance calculations.

34.1 Fast Power/Ground Network Optimization Based on Equivalent Circuit Modeling

X.-D. Sheldon Tan - *Altera Corp., San Jose, CA*
C.-J. Richard Shi - *Univ. of Washington, Seattle, WA*

34.2S An Interconnect Energy Model Considering Coupling Effects

Taku Uchino, Jason Cong - *Univ. of California, Los Angeles, CA*

34.3S Efficient Large-Scale Power Grid Analysis Based on Preconditioned Krylov-Subspace Iterative Methods

Tsung Hao Chen, Charlie Chung Ping Chen - *Univ. of Wisconsin, Madison, WI*

34.4S Conduction Modes Basis Functions for Efficient Electromagnetic Analysis of On-Chip and Off-Chip Interconnect

Luca Daniel, Alberto L. Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*
Jacob White - *Massachusetts Institute of Tech., Cambridge, MA*

34.5S Analysis of Non-Uniform Temperature-Dependent Interconnect Performance in High Performance ICs

Amir H. Ajami - *Univ. of Southern California, Los Angeles, CA*
Kaustav Banerjee - *Stanford Univ., Stanford, CA*
Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*
Lukas P.P.P. Van Ginneken - *Magma Design Inc., Cupertino, CA*

Session 35

rm: N107-N108

DOMAIN SPECIFIC DESIGN METHODOLOGIES

CHAIR: *Yosinori Watanabe - Cadence Berkeley Labs., Berkeley, CA*
ORGANIZERS: *Anand Raghunathan, Shin-ichi Minato*

In this session, we explore design methodologies that focus on specific application domains. The paper attacks the following three domain instances: direct digital frequency synthesizers for communication systems, symmetric block ciphers for cryptgraphic analysis, Viterbi decoders and IIR filters in DSPs. These case studies will hint at new methodologies for designing real-life applications.

35.1 UHDL Based Design and Design Methodology for Reusable High Performance Direct Digital Frequency Synthesis

Ireneusz Janiszewski, Bernhard Hoppe, Hermann Meuth - *FH Darmstadt, Darmstadt, Germany*

35.2 Concurrent Error Detection Schemes for Side-Channel Fault-Analysis of 128-bit Symmetric Block Ciphers

Ramesh Karri, Kaijie Wu, Yongkook Kim, Piyush Mishra - *Polytechnic Univ., New York, NY*

35.3 MetaCores: Design and Optimization Techniques

Seapahn Meguerdichian, Farinaz Koushanfar - *Univ. of California, Los Angeles, CA*
Dusan Petranovic, Advait Mogre - *LSI Logic Corp., Milpitas, CA*

Thursday June 21

10:30 to 12:00

All speakers are denoted in bold

S – denotes short paper

Session 36

rm: **N111-N114**

PANEL: DEBATE: WHO HAS NANOMETER DESIGN UNDER CONTROL?

CHAIR: *Andrew B. Kahng - Univ. of California at San Diego, La Jolla, CA*
ORGANIZER: *Bing Sheu*

As fabrication technology moves to 100 nm and below, profound nanometer effects become critical in developing silicon chips with hundreds of millions of transistors. Both EDA suppliers and system houses have been re-tooling, and new methodologies have been emerging. Will these efforts meet the challenges of nanometer silicon such as performance closure, power, reliability, manufacturability, and cost? Which aspects of nanometer design are, or are not, under control? This session will consist of a debate between two teams of distinguished representatives from EDA suppliers and system design houses. Which side has the right answers and roadmap? You and a panel of judges will decide!

PANELISTS:

Shekhar Borkar - Intel Corp., Hillsboro, OR
Ed Cheng - Synopsys, Inc., Mountain View, CA
John Cohn - IBM Corp., Essex Junction, VT
Nancy Nettleton - Sun Microsystems, Mountain View, CA
Lou Scheffer - Cadence Design Systems, Inc., San Jose, CA
Sang Wang - Nassda Corp., Santa Clara, CA

Session 37

rm: **N109-N110**

ANALYSIS AND IMPLEMENTATION FOR EMBEDDED SYSTEMS

CHAIR: *Grant Martin - Cadence Design Systems, Inc., San Jose, CA*
ORGANIZERS: *Dirk Grunwald, Kurt Keutzer, Luciano Lavagno*

This set of papers describes system level design tools and design flows for system design, performance trade offs and power estimation. The first paper uses simulink for rapid design of data-dominated applications. The remaining papers provide power models using automatic formalisms and the other using a combination of design captive and application characteristics.

37.1 A Hardware/Software Co-Design Flow and IP Library Based on Simulink

Leonardo Reyneri, Franceso Cucinotta, Alessandro Serra - *Politecnico di Torino, Turin, Italy*
Luciano Lavagno - *Univ. di Udine, Udine, Italy*

37.2 System-Level Power/Performance Analysis for Embedded Systems Design

Radu Marculescu, Amit Nandi - *Carnegie Mellon Univ., Pittsburgh, PA*

37.3 High-Level Software Energy Macro-Modeling

Tat K. Tan - *Princeton Univ., Princeton, NJ*
Anand Raghunathan, Ganesh Lakshminarayana - *NEC USA, Princeton, NJ*
Niraj Jha - *Princeton Univ., Princeton, NJ*

Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Session 38

rm: N115-N117

INDUSTRIAL CASE STUDIES IN VERIFICATION

CHAIR: *Carl Pixley* - Motorola, Inc., Austin, TX
ORGANIZERS: *Anand Raghunathan, Carl Pixley*

Verification is well-known to be one of the most expensive, delaying and critical aspects of the design process. We present three industrial case studies that illustrate novel approaches to integrating functional verification techniques: simulation, emulation and formal verification.

38.1 Model Checking of S3C2400X Industrial Embedded SoC Product

Hoon Choi, Byeongwhee Yun, Yuntae Lee, Hyunglae Roh - *Samsung Electronics, Yongin, Korea*

38.2 Semi-Formal Test Generation with Genevieve

Julia Dushina, Mike Benjamin - *ST Microelectronics, Bristol, UK*
Daniel Geist - *IBM Corp., Haifa, Israel*

38.3 A Transaction-Based Unified Simulation/Emulation Architecture for Functional Verification

Murali Kudlugi - *IKOS Systems, Inc., Waltham, MA*
Soha Hassoun - *Tufts Univ.*, Medford, MA
Charles Selvidge - *IKOS Systems, Inc., Waltham, MA*
Duaine Pryor - *IKOS Systems, Inc., Cueprtino, CA*

Session 39

rm: N119-N120

INTEGRATED HIGH-LEVEL SYNTHESIS BASED SOLUTIONS

CHAIR: *Kazutoshi Wakabayashi* - *NEC Corp., Kawasaki, Japan*
ORGANIZERS: *Kazutoshi Wakabayashi, Rajesh K. Gupta*

The focus of this session is on design flows that seek to integrate high-level synthesis into physical design. The first paper presents integration of HLS with power-net design targeted for mixed signal ICs. The second paper considers HLS with placement targeted for reconfigurable computing architectures. The last paper explores design exploration using multiple HLS tools.

39.1 Integrated High-Level Synthesis and Power-Net Routing for Digital Design under Switching Noise Constraints

Alex Doboli - *State Univ. of New York, Stony Brook, NY*
Ranga Vemuri - *Univ. of Cincinnati, Cincinnati, OH*

39.2 Integrating Scheduling and Physical Design into a Coherent Compilation Cycle for Reconfigurable Computing Architectures

Kia Bazargan - *Univ. of Minnesota, Minneapolis, MN*
Majid Sarrafzadeh - *Univ. of California, Los Angeles, CA*

39.3 Statistical Design Space Exploration for Application-Specific Unit Synthesis

Davide Bruni - *Univ. di Bologna, Bologna, Italy*
Alessandro Bogliolo - *Univ. di Ferrara, Ferrara, Italy*
Luca Benini - *Univ. di Bologna, Bologna, Italy*

Session 40

rm: N107-N108

TIMING VERIFICATION AND SIMULATION

CHAIR: *Ashok Vittal* - *Synopsys, Inc., Mountain View, CA*
ORGANIZER: *Narendra Shenoy*

This session deals with various aspects of timing issues including analysis, optimization, characterization and modeling for simulation that arise in EDA. Paper one describes techniques to support efficient verification with complex timing variations. Optimizing for crosstalk effects is the subject of paper two. Paper three is relevant in the context of sub-circuit characterization. Paper four deals with scheduling and synchronization for multiple clock domains.

40.1 Fast Statistical Timing Analysis By Probabilistic Event Propagation

Jing-Jia Liou, Kwang-Ting Cheng - *Univ. of California, Santa Barbara, CA*
Sandip Kundu - *Intel Corp., Austin, TX*
Angela Krstic - *Univ. of California, Santa Barbara, CA*

40.2S Functional Correlation Analysis in Crosstalk Induced Critical Paths Identification and Removal

Tong Xiao, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*

40.3S An Advanced Timing Characterization Method Using Mode Dependency

Hakan Yalcin, Robert Palermo, Mohammad S. Mortazavi - *Cadence Design Systems, Inc., San Jose, CA*
Cyrus S. Bamji - *Canesta Inc., Santa Clara, CA*
Karem A. Sakallah, John P. Hayes - *Univ. of Michigan, Ann Arbor, MI*

40.4 Static Scheduling of Multiple Asynchronous Domains for Functional Verification

Murali Kudlugi, Charles Selvidge - *IKOS Systems, Inc., Waltham, MA*
Russell G. Tessier - *Univ. of Massachusetts, Amherst, MA*

Thursday June 21

2:00 to 4:00

All speakers are denoted in bold

S – denotes short paper

Session 41

rm: **N111-N114**

SPECIAL SESSION: ON-CHIP COMMUNICATION ARCHITECTURES

CHAIR: *Anand Raghunathan - NEC USA C&C Research Lab., Princeton, NJ*
ORGANIZERS: *Anand Raghunathan, Sharad Malik*

Designing a high quality communication architecture is increasingly becoming critical to meeting performance, power, and turn around time constraints in the design of System-on-Chips.

This special session consists of invited presentations from designers of on-chip communication architectures used today, as well as researchers involved in developing architectures and design methodologies of the future.

The first presentation will highlight the role played by on-chip communication architectures in system design, describe the challenges involved, and present a communication-based design paradigm. The second presentation will describe how micro-network based architectures can be used to implement communication between SoC components. The third presentation will provide a design example from the domain of high-performance network processors, focusing on the challenges involved in on-chip communication, and how they are addressed. The final presentation will examine technology trends and their implications on on-chip communication architecture design, arguing the case for the use of packet-switched on-chip networks.

41.1 Addressing the System-on-a-Chip Interconnect Woes Through Communication-Based Design

Jan Rabaey, Alberto L. Sangiovanni-Vincentelli- *Univ. of California, Berkeley, CA*
Sharad Malik - *Princeton Univ., Princeton, NJ*
Kurt Keutzer - *Univ. of California, Berkeley, CA*

41.2 MicroNetwork-Based Integration for SOCs

Drew Wingard - *Sonics, Inc., Mountain View, CA*

41.3 Communication Architecture Design and Challenges for Gigahertz Network Processors

Faraydon Karim - *ST Microelectronics, San Diego, CA*

41.4 Route Packets, Not Wires: On-Chip Interconnection Networks

William Dally - *Stanford Univ., Stanford, CA*

Session 42

rm: **N109-N110**

COMPILER AND ARCHITECTURE INTERACTIONS

CHAIR: *Stephen Neuendorffer - Univ. of California, Berkeley, CA*
ORGANIZERS: *Donatella Sciuto, Marco Di Natale*

The efficient use and simulation of architecture components requires a fine tuning of the compiler algorithms or even a tight integration between components and compiler design. This session contains four papers spanning from compiler optimization techniques for reducing data transfers in clustered VLIW architectures to compiler-controlled scratch-pad memory management, to fast simulation of fixed point systems through code transformation.

42.1 Dynamic Management of Scratch-Pad Memory Space

Mahmut T. Kandemir - *Penn State Univ., University Park, PA*
J. Ramanujam - *Louisiana State Univ., Baton Rouge, LA*
Mary Jane Irwin, Vijaykrishnan Narayanan, Ismail Kadayif, Amisha Parikh - *Penn State Univ., University Park, PA*

42.2 Clustered VLIW Architectures with Predicated Switching

Margarida F. Jacome, Gustavo A. de Veciana, Satish Pillai - *Univ. of Texas, Austin, TX*

42.3 High-Quality Operation Binding for Clustered VLIW Datapaths

Viktor S. Lapinskii, Margarida F. Jacome, Gustavo A. de Veciana - *Univ. of Texas, Austin, TX*

42.4 Fast Bit-True Simulation

Holger Keding, Martin Coors, Olaf Luethje, Heinrich Meyr - *Integrated Signal Processing Systems, Aachen, Germany*

Session 43

rm: N115-N117

TIMING WITH CROSSTALK

CHAIR: *Sachin S. Sapatnekar - Univ. of Minnesota, Minneapolis, MN*

ORGANIZERS: *Jaijeet Roychowdhury, Mustafa Celik*

This session deals with the impact of crosstalk on timing. The first paper uses a theoretical approach to analyze some practical issues such as convergence. The second paper introduces a new driver model for accurate coupled noise modeling and then discusses worst case alignment. The third paper uses functional information to eliminate false coupling interactions to avoid pessimistic delay calculation. The last paper proposes a post-layout optimization technique to reduce coupling induced delay.

43.1 Timing Analysis with Crosstalk as Fixpoints on Complete Lattice

Hai Zhou, Narendra Shenoy, William Nicholls - *Synopsys, Inc., Mountain View, CA*

43.2 Driver Modeling and Alignment for Worst-Case Delay Noise

Supamas Sirichotiyakul, David Blaauw, Chanhee Oh - *Motorola, Inc., Austin, TX*
Rafi Levy - *Motorola, Inc., Herzelia, Israel*
Vladimir Zolotov - *Motorola, Inc., Austin, TX*

43.3 False Coupling Interactions in Static Timing Analysis

Ravishankar Arunachalam, Ronald D. Blanton, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

43.4 Coupling Delay Optimization by Temporal Decorrelation using Dual Threshold Voltage Technique

Kiwook Kim, Seong Ook Jung - *Univ. of Illinois, Urbana, IL*
Prashant Saxena - *Intel Corp., Portland, OR,*
Chaung Laung Liu - *National Tsing-Hua Univ., Hsinchu, Taiwan, ROC*
Sung Mo Kang - *Univ. of Illinois, Urbana, IL*

Session 44

rm: N119-N120

LOW POWER DESIGN: SYSTEMS TO INTERCONNECT

CHAIR: *Vivek Tiwari - Intel Corp., Santa Clara, CA*

ORGANIZERS: *Ingrid Verbauwhede, Tadahiro Kuroda*

Low Power design needs to be addressed at all levels. At the system level, the first paper presents a generalized approach to the concept of partitioning the input space and applying specific optimizations to the partitions for overall energy reduction. The issue of energy consumption in DSM interconnects has gained attention recently. The next three papers present an introduction and different approaches to the problem. The final paper describes the circuit design of an adiabatic multiplier.

44.1 Input Space Adaptive Design: A High-Level Methodology for Energy and Performance Optimization

Weidong Wang - *Princeton Univ., Princeton, NJ*
Ganesh Lakshminarayana, Anand Raghunathan - *NEC USA, Princeton, NJ*
Niraj K. Jha - *Princeton Univ., Princeton, NJ*

44.2 A2BC: Adaptive Address Bus Coding for Low Power Deep Sub-Micron Designs

Joerg Henkel - *NEC USA, Princeton, NJ*

44.3S Coupling-Driven Bus Design for Low-Power Application-Specific Systems

Youngsoo Shin, Takayasu Sakurai - *Univ. of Tokyo, Tokyo, Japan*

44.4S Modeling and Minimization of Interconnect Energy Dissipation in Nanometer Technologies

Clark N. Taylor, Sujit Dey, Yi Zhao - *Univ. of California at San Diego, La Jolla, CA*

44.5 Student Design Contest: A True Single-Phase 8-bit Adiabatic Multiplier

Suhwan Kim, Conrad H. Ziesler, Marios C. Papaefthymious - *Univ. of Michigan, Ann Arbor, MI*

Session 45

rm: N107-N108

FLOORPLANNING REPRESENTATIONS AND PLACEMENT ALGORITHMS

CHAIR: *Ralph H.J.M. Otten - Delft Univ. of Technology, Delft, The Netherlands*

ORGANIZERS: *Louis Scheffer, Patrick Groeneveld*

The first two papers offer improved representations for floorplanning, offering faster incremental updates and capable of handling a wider variety of block shapes and constraints. The next two papers are improvements of partitioning based placement, providing better quality of results in wire length and timing. The final paper takes a novel approach, using system level power considerations to drive partitioning and placement.

45.1 TCG: A Transitive Closure Graph-Based Representation for Non-Slicing Floorplans

Jai Ming Lin, Yao Wen Chang - *National Chiao Tung Univ., Hsinchu, Taiwan, ROC*

45.2 Floor planning with Abutment Constraints and L-Shaped/T-Shaped Blocks Based on Corner Block List

Yuchun Ma, Xianlong Hong, Sheqin Dong, Yici Cai - *National Tsing-Hua Univ., Beijing, China*
Chung Kuan Cheng - *Univ. of California at San Diego, La Jolla, CA*
Jun Gu - *Science and Tech. Univ. of Hong Kong, Hong Kong, China*

45.3S Optimal Cut Sequences for Partitioning Based Placement

Patrick H. Madden, **Mehmet C. Yildiz** - *State Univ. of New York, Binghamton, NY*

45.4S Timing Driven Placement using Physical Net Constraints

Bill M. Halpin - *Intel Corp., Santa Clara, CA*
C. Y. Roger Chen - *Syracuse Univ., Syracuse , NY*
Naresh K. Sehgal - *Intel Corp., Santa Clara, CA*

45.5 From Architecture to Layout: Partitioned Memory Synthesis for Embedded Systems-on-Chip

Luca Benini - *Univ. di Bologna, Bologna, Italy*
Luca Macchiarulo, Alberto Macii, Enrico Macii, **Massimo Poncino** - *Politecnico di Torino, Torino, Italy*

Thursday
June 21

4:30
to
6:00

All speakers are denoted in **bold**

S – denotes short paper

Session 46

rm: N111-N114

PANEL: WHAT DRIVES EDA INNOVATION?

CHAIR: *Steve Schulz* - Texas Instruments, Dallas, TX
ORGANIZER: *Georgia Marszalek*

If EDA technology innovation drives return on investment, what drives innovation? Is it tied to the semiconductor retooling cycle? To productivity requirements? To Moore's Law? Or is there something more fundamental that we are missing? What driving forces could result in a $30 billion EDA industry, and what role will innovation play? Will the industry provide the needed breakthroughs for their customers, or seek instead the lowest common denominator user? Will designers "roll their own" tools or seek common solutions? How does EDA innovation track with the semiconductor business cycle? Does a slowdown accelerate or depress creation of new tools and new designs? Panelists will discuss the forces at work in the EDA industry of tomorrow.

PANELISTS:

John Darringer - IBM Corp., Yorktown Heights, NY
Greg Hinckley - Mentor Graphics Corp., Wilsonville, OR
George Janac - InTimeSoftware, Inc., Cupertino, CA
Handel Jones - International Business Strategies, Los Gatos, CA
Greg Spirakis - Intel Corp., Santa Clara, CA
Karen Vahtra - Magma Design Automation, Inc., Cupertino, CA

Session 47

rm: N109-N110

SIGNAL INTEGRITY: AVOIDANCE AND TEST TECHNIQUES

CHAIR: *Anirudh Devgan - IBM Corp., Austin, TX*
ORGANIZERS: *Chandu Visweswariah, Kenji Yoshida*

Inductive effects in interconnect are a major source of headaches for state-of-the-art digital designs. Inductive effects cause nasty timing and noise problems and threaten to be show-stoppers. This session features three innovative techniques to solve, avoid or test for these problems.

47.1 Built-In Self-Test for Signal Integrity

Mehrdad Nourani, Amir Attarha - *Univ. of Texas at Dallas, Richardson, TX*

47.2 Analysis of On-Chip Inductance Effects using a Novel Performance Optimization Methodology for Distributed RLC Interconnects

Kaustav Banerjee - *Stanford Univ., Stanford, CA*
Amit Mehrotra - *Univ. of Illinois, Urbana, IL*

47.3 Modeling and Analysis of Differential Signaling for Minimizing Inductive Cross-Talk

Yehia M. Massoud, Jamil Kawa, Don MacMillen - *Synopsys, Inc., Mountain View, CA*
Jacob K. White - *Massachusetts Institute of Tech., Cambridge, MA*

Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Session 48

rm: N115-N117

NOVEL APPROACHES TO MICROPROCESSOR DESIGN AND VERIFICATION

CHAIR: *Derek Beatty - Motorola, Inc., Austin, TX*
ORGANIZERS: *Carl Pixley, Shin-ichi Minato*

This session covers novel approaches to the correct design and verification of complex microprocessors, including automatic design of interlock and forwarding logic, generation of test programs to exercise complex corner cases, and verification techniques for the error logic.

48.1 Automated Pipeline Design

Daniel Kroening, Wolfgang Paul - *Univ. of Saarland, Saarbruecken, Germany*

48.2 A New Verification Methodology for Complex Pipeline Behavior

Kazuyoshi Kohno, Nobu Matsumoto - *Toshiba Corp., Kawasaki, Japan*

48.3 Pre-Silicon Verification of the [X] Microprocessor Error Handling System

Richard Lee, **Benjamin Tsien** - *Compaq Computer Corp., Palo Alto, CA*

Session 49

rm: N119-N120

SCHEDULING TECHNIQUES FOR POWER MANAGEMENT

CHAIR: *Donatella Sciuto - Politecnico di Milano, Milano, Italy*
ORGANIZERS: *Diederik Verkest, Luciano Lavagno*

Power constraints become increasingly important in embedded systems. This session presents new scheduling techniques for power management under different circumstances. The first paper presents a technique to determine voltage settings for a variable voltage processor. The second paper introduces a formal model of distributed multimedia systems that enables determining an optimal power management policy. The third paper looks at power aware scheduling in the context of mission critical systems.

49.1 Energy Efficient Fixed-Priority Scheduling for Real-Time Systems on Variable Voltage Processors

Gang Quan, Sharon Hu - *Univ. of Notre Dame, Notre Dame, IN*

49.2 Dynamic Power Management in a Mobile Multimedia System with Guaranteed Quality-of-Service

Qing Wu - *Univ. of Southern California, Los Angeles, CA*
Massoud Pedram - *Univ. of California, Los Angeles, CA*
Qinru Qiu - *Philips Research Lab., Irvine, CA*

49.3 Power-Aware Scheduling under Timing Constraint for Mission-Critical Embedded Systems

Jinfeng Liu - *Univ. of California, Irvine, CA*

Session 50

rm: N107-N108

NOVEL DEVICES AND YIELD OPTIMIZATION

CHAIR: *Chandu Visweswariah - IBM Corp., TJ Watson Research Ctr., Yorktown Heights, NY*
ORGANIZERS: *Chandu Visweswariah, Ralph Otten*

How soon will novel devices revolutionize integrated circuits? What can we do about falling yields due to mismatch and intra-chip variations? This session takes a shot at answering these questions. It begins with description of novel 3-dimensional SOI devices and then a novel MEMS accelerometer for mouse applications. Finally, yield optimization due to mismatch problems is addressed.

50.1 Exploring SOI Device Structures and Interconnect Architectures for 3-Dimensional Integration

Rongtian Zhang, Kaushik Roy, Cheng Kok Koh, David B. Janes - *Purdue Univ., West Lafayette, IN*

50.2 Student Design Contest: Two-Dimensional Position Detection System with MEMS Accelerometer for MOUSE Applications

Seungbae Lee, Gi-Joon Nam, **Junseok Chae**, Hanseup Kim, Alan J. Drake - *Univ. of Michigan, Ann Arbor, MI*

50.3 Mismatch Analysis and Direct Yield Optimization by Spec-Wise Linearization and Feasibility-Guided Search

Frank Schenkel, Michael Pronath - *Tech. Univ. of Munich, Munich, Germany*
Stephan Zizala, Robert Schwencker, Helmut Graeb - *Infineon Technologies, Munich, Germany*
Kurt Antreich - *Tech. Univ. of Munich, Munich, Germany*

Tutorial 1 — Friday, June 22

Tutorials will be held at the Las Vegas Convention Center.

8:00 AM - 1:00 PM Tutorial Registration Open
8:00 AM - Continental Breakfast
9:00 AM - 5:00 PM Tutorials
12:00 Noon - Lunch

DESIGN-FOR-TEST TECHNIQUES FOR SoC DESIGNS

ORGANIZER: *Janusz Rajski* - Mentor Graphics Corp., Willsonville, OR
PRESENTERS: *Janusz Rajski* - Mentor Graphics Corp., Willsonville, OR
Alfred Crouch - Motorola, Inc., Austin, TX
Geir Eide - Mentor Graphics Corp., Wilsonville, OR

Audience: Designers of complex systems-on-a-chip and ASICs, IP core providers, SoC integrators, system architects, and design managers interested in learning about state-of-the art DFT technology, practices and automation tools.

Description: Complex SoC designs contain millions of gates of logic and, in some cases, hundreds of embedded memories. In a complex SoC design process, Design-for-Test is one of the crucial components that determine the time to market, product quality, and its manufacturing cost. This tutorial aims to jump start the designer to new levels of practical test expertise by presenting DFT methodologies, solutions, and technological advancements for addressing today's toughest DFT issues. The tutorial briefly introduces basic DFT concepts and techniques, and focuses on practical issues such as: IP core design guidelines that enable test reuse, DFT for complex SoC designs, embedded memory test, at-speed test, and DFT integration into the design flow. More specifically the tutorial presents in detail structural Design-for-Test methodologies based on scan, i.e. scan cell design, scan operation, scan chain optimization, multiple clock domains, test logic, test points, basic concepts of Logic BIST, and boundary scan. Automatic test pattern generation (ATPG) creates high quality, compact test patterns in a fully automated manner. The highlights of the section addressing ATPG include: design rules checking, random and deterministic test pattern generation, pattern compression techniques, test pattern verification, combinational and sequential pattern types, at-speed test.

A special section of the tutorial is devoted to testing of embedded memories. It reviews: memory types, fault models, test algorithms, and test methods (Memory BIST and Vector translation).

The final section focuses on core test and SoC test integration. This chapter covers DFT in the design cycle, scan insertion flow, physical aspects of SoC DFT, test wrappers for IP cores, design guidelines and recommendations for test reuse, hierarchical test pattern generation, test access mechanisms, test scheduling, SoC test integration and verification. Important concepts and methodologies are illustrated by practical applications and case studies.

Tutorial 2 — Friday, June 22

INTERACTIVE TUTORIAL ON FUNDAMENTALS OF SIGNAL INTEGRITY FOR HIGH-SPEED/HIGH-DENSITY DESIGN

ORGANIZERS: *Andreas Cangellaris* - Univ. of Illinois, Urbana, IL
José Schutt-Ainé - Univ. of Illinois, Urbana, IL

PRESENTERS: *Andreas Cangellaris* - Univ. of Illinois, Urbana, IL
Alina Deutsch - Univ. of Illinois, Urbana, IL
Umberto Ravaioli - IBM Corp., Yorktown Heights, NY
José Schutt-Ainé - Univ. of Illinois, Urbana, IL

Audience: PCB and chip designers who want to gain familiarity with signal integrity issues at high-speeds and who want to develop a more practical approach for designing high-speed modules and high-density chips. Knowledge of basic transmission line theory will be helpful.

Description: With the advent of fast processors and high frequency communication networks, the demand for more accurate computer-aided design (CAD) tools has increased dramatically. Faster signals and higher packing density have exacerbated the noise issues in state-of-the-art IC and package designs. This course will offer an in-depth understanding of the fundamental mechanisms that govern broadband signal transmission in interconnect structures at the different levels of integration. Signal transmission attributes and proper interconnect modeling on-chip and off-chip will be explained and demonstrated through the use of JAVA applets that will be made available to the course participants.

Particular emphasis will be placed on the present-day on-chip wiring design practices and the unique properties of on-chip lossy transmission lines. The deficiencies of RC-circuit-representation-based designs and tools will be highlighted through relevant examples. The shortcomings of some of the RLC-based available tools will also be explained. It will be shown that frequency-dependent resistive and inductive effects (R(f)L(f)C-circuit-representation) are especially important for crosstalk, common-mode noise, and clock skew. Guidelines will be given for design, technology scaling, device sizes used, noise containment, length tradeoffs, clock distribution, operating temperature, and bandwidth improvement. The need for multi-variable performance-driven routers based on worst-case delay, propagated rise-time, and crosstalk will be explained in order to make adequate use of available technologies.

Tutorial 3 — Friday, June 22

CAD TOOLS FOR MIXED-SIGNAL AND RF ICs

ORGANIZER: *Georges Gielen* - Katholieke Univ., Leuven, Belgium
PRESENTERS: *Georges Gielen* - Katholieke Univ., Leuven, Belgium
Rob A. Rutenbar - Carnegie Mellon Univ., Pittsburgh, PA
Jaijeet Roychowdhury - CeLight, Inc., Sprinfield, NJ
Francois Clement - Simplex Solutions Inc., Grenoble, France

Audience: Practicing analog, RF and mixed-signal designers who want to learn about the new techniques and methodologies that could boost their design quality and productivity. CAD professionals responsible for implementing or maintaining analog, RF or mixed-signal tools or flows. Anyone with interests in practical RF or mixed-signal ICs.

Description: The growth of wireless services and other telecom applications increases the need for low-cost highly integrated solutions with very demanding performance specifications. This requires the development of intelligent front-end architectures that circumvent the physical limitations posed by the technology. In addition, with the evolution towards ultra deep submicro CMOS technologies, the design of complex systems on a chip (SoC) will emerge which are increasingly mixed-signal designs. The desire to do hand-crafted, one-transistor-at-a-time analog design is increasingly at odds with the current time-to-market constraints and hence the need for more analog design productivity, practical circuit and layout synthesis, and reliable verification at all levels of the mixed-signal hierarchy.

This tutorial will present the recent progress and current state of the art in design tools and methodologies for complex mixed-signal designs as well as for RF IC design. Different aspects will be covered by the different presenters, ranging from techniques and methodologies for analog synthesis both at architectural, circuit and layout level, as well as the recent progress in simulation and modeling for RF designs, as well as methods to analysis substrate noise couplings in mixed-signal ICs. The techniques will be addressed from a designer point of view, so that the attendees can assess how the techniques could be integrated to improve their current design practice.

The tutorial is divided in 4 parts. The first part will describe tools for designing analog building blocks. The second part will present tools for high-level design and simulation of mixed-signal systems. The third part will describe modeling and simulation techniques for RF circuits. The final part will describe methods for the analysis of substrate noise coupling problems in mixed-signal ICs.

Tutorial 4 — Friday, June 22

DESIGN-MANUFACTURING INTERFACE FOR UDSM ERA: DESIGNER AND CAD TOOL DEVELOPER PERSPECTIVES

ORGANIZER: *Andrzej J. Strojwas* - Carnegie Mellon Univ., Pittsburgh, PA
PRESENTERS: *Wojciech Maly* - Carnegie Mellon Univ., Pittsburgh, PA
Dennis Ciplickas - PDF Solutions Inc., San Jose, CA
Sani Nassif - IBM Austin Research Lab., Austin, TX
Andrzej J. Strojwas - Carnegie Mellon Univ., Pittsburgh, PA

Audience: The subtitle of this tutorial is: "What every designer and CAD tool developer should know about the implications of the Ultra Deep Submicron reality on the gigascale product design, verification and manufacturability". It is intended for all system and IC designers, CAD tool developers and university researchers. No IC technology/manufacturing background is required as a prerequisite.

Description: In this age of multi-billion dollar IC fablines and increased time-to-market pressures, achieving profitable production in the shortest possible time becomes an absolutely necessary condition for success. Increasing the initial yield and the rate of the yield ramp has the biggest impact on the product profitability. This task is especially challenging given the disaggregation of semiconductor industry, i.e., emergence of fabless companies and increasing role of foundries in manufacturing. This complex interface between "mother nature", represented by manufacturing process, and the design domain, focused more and more on higher levels of design abstraction, cannot be covered by a simple set of layout design rules and SPICE files to represent all essential relationships. The purpose of this tutorial is to depict a reality of the design-manufacturing interface in a manner useful to IC designers and CAD tool developers.

We will start by presenting an overview of trends in semiconductor industry focusing on the accelerated roadmap which leads to further miniaturization and the increasing role of manufacturing fluctuations. In the big picture, the most important link between design and manufacturing is quantified via manufacturing yield, which must be maximized during IC fabrication but is strongly determined by the design decisions made at all design abstraction levels. Therefore, manufacturing-aware design flow must rely on a spectrum of yield models. We will review in detail such models in the first part of the tutorial.

However, yield modeling cannot be useful if the models are not tuned to process reality and therefore cannot capture IC design sensitivity to process imperfections. To address this issue, the next part of our tutorial will be devoted to process/design characterization techniques/strategies via a comprehensive set of characterization vehicles to identify the key yield loss reasons (systematic, parametric, random defects). We will then discuss abstraction of manufacturability/reliability design rules including sub-wavelength lithography (OPC, PSM) and realistic worst-case SPICE files. These DFM interface capabilities will re-define the design flow and will pose new requirements on the EDA tools. They will enable much more predictive design synthesis and much more realistic verification of the system before its manufacturing. The bulk of our tutorial will propose such a design flow utilizing this DFM interface. We will focus on the following key tasks: technology choice (including monolithic vs. MCM, forecasting of performance, yield ramp-up and cost), high level design decisions using technology abstraction (choice of IP cores, IP migration vs. re-synthesis, etc.), estimation/optimization of timing, signal integrity and power, taking into account manufacturing fluctuations, circuit design optimization for SoC - including mixed-signal components (design centering, timing optimization) and layout optimization (including pre-tapeout optimization and post-tapeout transformations such as model-based OPC).

We will conclude the tutorial by discussing the technical and organizational challenges that must be overcome to successfully implement this new design-manufacturing interface.

Tutorial 5 — Friday, June 22

LOW POWER TOOLS AND METHODOLOGIES FOR THE ASIC INDUSTRY

ORGANIZER: *Rakesh Patel* - Intel Corp., Santa Clara, CA
PRESENTERS: *Enrico Macii* - Politecnico di Torino, Torino, Italy
Jerry Frankil- Sequence Design Inc., Acton, MA
Renu Mehra - Synopsys, Inc., Mountain View, CA
Mike Lee - Incentia Design Systems, Inc., Santa Clara, CA
Roberto Zafalon - ST Microelectronics, Agrate Bianza, Italy

Audience: This tutorial is primarily intended for ASIC designers, planners and project managers who are looking for practical solutions for reducing power in their designs. The focus is on power-aware design flows/methodology based on CAD solutions that are available today. It is hoped that attendees will come away with an understanding of the issues, tradeoffs and benefits of low power tools and will be able to effectively apply this knowledge to their designs and design flows.

Description: Power has been trending higher on the list of design constraints and today it is at or near the top across all computing platforms - whether this be laptops, cell-phones, hand-held PDAs, rack-mounted web-servers, routers, or big-iron servers in a backroom. Power is no longer a concern for only the thermally constrained high-performance (high-power) systems and energy-constrained low-power hand-held/portable systems. An ever-growing number of ASIC designs in all domains (chipsets, graphics, networking, media-processing, communication, etc.) are now faced with tight power budgets. Designers, many of whom are confronting this challenge for the first time, are looking for solutions they can use. There is large body of literature now on low power techniques, algorithms and tools, but this is not directly applicable to designers who do not have the luxury of creating or optimizing their own libraries, incorporating the latest modeling advance into their power estimation tools, or extending their synthesis tools with the latest algorithms. For these designers, what works are: a) best-known methods for optimizing their logic - RTL description, either manually or through automation b) ready-made estimation tools than can provide early feedback during the RTL-phase c) estimation tools that provide feedback during or after synthesis and that can be used to direct the synthesis tools d) optimization algorithms built into the synthesis solutions.

The tutorial is structured to provide information on the state of the art in all these domains. It will start by motivating the need of industrial design frameworks (i.e., combination of design techniques and CAD tools) that explicitly address power minimization. A possible design flow for low-power ASICs will be proposed next. A discussion on how the existing CAD technology is able to support the proposed flow will close the first part. The second part will focus on RT level and gate level power estimation and optimization techniques, commercially available power management solutions and future directions for industrial low power solutions. The third part will focus on recent power optimization techniques in logical and physical synthesis. The last part of the tutorial will provide an industrial design perspective. It will provide examples of applications of the above tools and techniques to real designs. Both power estimation and power optimization experiments and results will be presented and discussed in detail.

FIELD PROGRAMMABLE DEVICES: ARCHITECTURE AND CAD TOOLS

ORGANIZER: *Majid Sarrafzadeh* - Univ. of California, Los Angeles, CA
PRESENTERS: *Jason Cong* - Univ. of California, Los Angeles, CA
Alireza Kaviani - Xilinx, Inc., San Jose, CA
Eyal Odiz - Synplicity, Inc., Menlo Park, CA
Majid Sarrafzadeh - Univ. of California, Los Angeles, CA

Audience: Architects, CAD tool developer and users of Field Programmable Devices (FPDs). Researchers interested in learning fundamental problems associated with FPDs. Managers interested in learning more about these devices.

Description: Field Programmable Devices (FPDs) represent an exciting technology that is affecting the way digital circuitry is designed. By offering the advantages of faster time to market and ease of design changes, FPDs have become increasingly popular among the designers in both small and large companies. The purpose of this tutorial is to provide an overview of FPD architecture and related CAD techniques in order to provide a clear understanding of both their capabilities and shortcomings.

We start by presenting a short history, starting from the original simple PLAs to today's complex commercial FPDs. After understanding the basics of various FPD architectures we move on to explain more advanced features of recent FPGAs, such as special-purpose circuitry for arithmetic applications, memory blocks, clock management, and I/O features. We demonstrate examples of those features in VirtexII and APEX, which are the most recent products from two of the largest FPD vendors. Then we look into the near future of commercial products, which involves integrating a microprocessor on FPGAs. The integration of FPGAs and microprocessors on the same chip will potentially expand the current FPD market to embedded systems by creating new applications. In addition, this new product might provide a suitable platform for configurable computing, which requires a successful marriage between two established programmable technologies: reconfigurable hardware and microprocessors. Next, we conclude this part of the tutorial by providing the highlights of the recent academic research efforts dedicated to the architecture of programmable devices with the goal of improving their speed-performance and area-efficiency.

Finally, we review recent synthesis and physical design of FPDs. We review state-of-the-art logic synthesis, technology mapping, placement with wirelength, congestion, and timing optimization followed by routing methodologies. In particular we focus on CAD methodologies that are of interest in dealing with very large FPDs.

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Technical Program Committee

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Exhibitor List

Company	Booth #
@HDL, Inc.	48
0-In Design Automation	800
3DSP Corp.	652
ACE Associated Compiler Experts bv	111
Actel Corp.	2128
Adaptive Silicon, Inc.	622
Agilent Technologies	210
Alba Centre (The)	1017
ALDEC, Inc.	2428
Altera Corp.	2700
Alternative System Concepts, Inc.	3909
AMI Semiconductor, Inc.	821
AmmoCore Technology, Inc.	3742
Amphion	430
Analog Design Automation	3041
Ansoft Corp.	3225
Antrim Design Systems, Inc.	1742
APLAC Solutions Corp.	353
Applied Simulation Technology	1114
Aptix Corp.	3628
Arcadia Design Systems, Inc.	230
Archelon Inc.	724
Arexsys Inc.	1414
Aristo Technology, Inc.	3600
Artisan Components, Inc.	2911
Artwork Conversion Software Inc.	3308
Aspex Technology	348
ASSET InterTech, Inc.	2637
ATMOS Corp.	3913
Automata Design, Inc., Adiva Software	1116
Avant! Corp.	2706
Averant, Inc.	3441
Avery Design Systems Inc.	345
Axis Systems	500
AXYS Design Automation, Inc.	655
Barcelona Design	200
Beach Solutions	218
Beige Bag Software, Inc.	250
BindKey Technologies	552
BlueLabs Microelectronics AB	452
BOPS, Inc. Billions of Operations Per Second	627
Bridges2Silicon	125
BTA-Ultima	3215
C Level Design, Inc.	3400
Cadence Design Systems, Inc.	2615
Cahners Business Information	804
CARDtools Systems	105
CAST, Inc.	3932
Celoxica, Inc.	544
ChipData, Inc.	1030
Chipidea Microelectronica S.A.	107
Chronology Corp.	3611
Circuit Semantics, Inc.	3605
Cliosoft, Inc.	148
CMP	234
CMP Media Inc.	1724
Co-Design Automation, Inc.	844
ComCAD GmbH Analog Design Support	839
Comit Systems, Inc.	117
Concept Engineering GmbH	634
CoVerify Solutions Inc.	1308
CoWare, Inc.	833
CreOsys Inc.	1252
CynApps	1544
Cynergy System Design, Inc.	814
Cypress Semiconductor	3437
D2W Design-to-Wafer Services	101
Denali Software, Inc.	1400
Derivation Systems, Inc.	1209
Design & Reuse	1025
Design Workshop	120
DesignSoft, Inc.	1016
Dolphin Integration	3743
DSM Technologies, Inc.	3914
DSP Valley	427
Dynalith Systems, Inc.	852
e*ECAD	1454
eASIC	520
EDA Standards	2611
EDAptive Computing, Inc.	3901
EDAToolsCafe.com	1018
Electronic Tools Co.	2634
Electronics Workbench	1230
Endeavor Intertech Corp.	152
ESilicon	102
Esterel Technologies	424
Faraday Technology Corp.	618
Fintronic USA, Inc.	1322
Fluence Technology	3034
Foresight Systems, Inc.	1421
Frontier Design, Inc.	1021
FTL Systems, Inc.	2838
Future Design Automation Co., Ltd.	549
GDA Technologies, Inc.	418
Genesys Testware	1014
Ger2Chip.com, Inc.	1737
Gidel Ltd.	112
Global UniChip Corp.	522
Green Light, LLC	1239
Hewlett-Packard Co.	3000
IBM Microelectronics	318
IC Nexus Co., Ltd.	114
Icinergy, Inc.	3918
IDS-Insight Design Services	856
IKOS Systems Inc.	3028
IMEC	1133
IMEC/Europractice	1136
iMODL, Inc.	207
Improv Systems	322
Incentia Design Systems, Inc.	2841
InnoLogic Systems, Inc.	3204
Innoveda, Inc.	2621
Integrated Measurement Systems	644
Integrated Systems Engineering, Inc.	251
Intellitech Corp.	830
Intercept Technology Inc.	3211
InternetCAD.com, Inc.	3304
Interra, Inc.	1405
Interra Technologies, Inc.	836
Interweave Tech Corp.	3642
InTime Software, Inc.	3234
Intrinsix Corp.	2834
Intusoft	150

Exhibitor List (cont.)

Company	Booth #
IOTA Technology Inc.	841
iRoC Technologies	1241
John Wiley & Sons, Inc.	106
Kluwer Academic Publishers	3206
Lattice Semiconductor Corp.	1425
Leda Systems	116
Legend Design Technology, Inc.	3411
Lexra, Inc.	636
Library Technologies, Inc.	3920
Logic Express Systems Inc.	248
LogicVision, Inc.	3633
LPKF Laser & Electronics	548
Magma Design Automation, Inc.	807
MATRICuS Inc.	3736
MEMSCAP	1244
Mentor Graphics Corp.	718, 2115, 2415
Micro Magic, Inc.	825
Model Technology Inc.	2418
Monterey Design Systems	513
Morgan Kaufmann Publishers, Inc.	133
MOSIS	1333
Mosys, Inc.	3907
MyCAD, Inc.	1218
Nassda Corp.	1439
Neo Linear, Inc.	214
Nordic VLSI ASA	3637
Novas Software, Inc.	2107
Numerical Technologies, Inc.	1711
NurLogic Design, Inc.	1226
OEA International, Inc.	3404
OptEM Engineering Inc.	3927
Palmchip Corp.	327
PennWell Corp.	127
Penton Media, Inc.	510
picoTurbo, Inc.	119
Platform Computing Inc.	3407
PLATO Design Systems Inc.	456
Precience	1433
Prentice Hall-PTR	1434
Proceler, Inc.	527
Progate Group Corp.	3639
Prolific, Inc.	3237
Prover Technology Inc.	1451
Provis Corp.	1448
Pulsic Inc.	1052
QThink	3923
QuickLogic Corp.	722
Rambus Inc.	525
Random Logic Corp.	448
Real Intent	1044
RUBICAD Corp.	2411
Runtime Design Automation	1309
Sagantec	3021
sci-worx Corp.	1207
Sequence Design, Inc.	2134
Shearwater Group, Inc. (The)	630
Sigrity Inc.	3922
Silicon Design Solutions, Inc.	720
Silicon Graphics Computer Systems Inc.	648
Silicon Integration Initiative, Inc. (si2)	3321
Silicon Logic Engineering, Inc.	3636
Silicon Metrics Corp.	2540
Silicon Perspective Corp.	1429
Silicon Valley Research, Inc.	2121
SiliconCraft Inc.	126
Silvaco International	1410
Simplex Solutions, Inc.	3621
Simpod, Inc.	610
Simucad, Inc.	1418
Simutech, LLC	1733
Simutest, Inc.	1118
SliceX, Inc.	108
SmartSand Inc.	450
Sonics Inc.	1048
Sun Microsystems	3228
SynaptiCAD Inc.	1221
Synchronicity, Inc.	2102
Synopsys, Inc.	2400
Synplicity, Inc.	3615
SynTest Technologies, Inc.	818
Syntricity Inc.	550
Tanner EDA	3025
Target Compiler Technologies N.V.	533
Techmate Inc.	333
Tensilica, Inc.	3739
Tera Systems Inc.	1730
Teradyne, Inc.	3933
Tharas Systems Inc.	2340
TILAB S.p.A.	3900
TM Associates, Inc.	128
TOPS Systems Corp.	727
TransEDA Technology Ltd.	1707
Translogic USA Corp.	3925
Triscend Corp.	725
TSMC	848
UMC (USA) Group	3037
University Booth	3004
Valiosys SA	3737
VALOR Computerized Systems	2140
VaST Systems Technology Corp.	2437
Verisity Design, Inc.	1702
Veritable, Inc.	3934
Veritools, Inc.	2111
Verplex Systems, Inc.	1000
Virage Logic Corp.	506
Virtio	518
Virtual Component Exchange	1256
Virtual Prototypes, Inc.	422
Virtual Silicon Technology	1213
Viscid Design Technologies, Inc.	350
Vitalect Inc.	554
Warhol Design Systems, Inc.	434
Western Design Center	1223
Willamette HDL, Inc.	3306
Wolfram Research	449
X-Tek Corp.	2434
Xilinx, Inc.	1715
Xpedion Design Systems, Inc.	1248
XYALIS	351
Y Explorations, Inc.	204
Zaiq Technologies, Inc.	3911
Zeland Software, Inc.	553
Zuken USA	2628

Exhibitor Presentation Morning Schedule

These 15-minute presentations by DAC Exhibitors are intended to efficiently introduce you to new product and application information.
Badges are not required for admission to the Exhibitor Presentations, Monday, June 18.

Time	ROOM N102	ROOM N107-N108	ROOM N109-N112	ROOM N113-N114	ROOM N115-N117	ROOM N119-N120
9:00	Veritable, Inc.	AXYS Design Automation, Inc.	Zuken USA	Prolific, Inc.	Sun Microsystems	Xpedion Design Systems, Inc.
9:15	Faraday Technology Corp.	Simutest, Inc.	InTime Software, Inc.	Virtual Component Exchange	Translogic USA Corp.	iMODL, Inc.
9:30	SiliconCraft Inc.	IDS-Insight Design Services	Denali Software, Inc.	Silvaco International	Interra, Inc.	Provis Corp.
9:45	EDAptive Computing, Inc.	Triscend Corp.	Virage Logic Corp.	Simucad, Inc.	Model Technology Inc.	Dynalith Systems, Inc.
10:00	BOPS, Inc. Billions Of Operations Per Second	InternetCAD.com, Inc.	Antrim Design Systems, Inc.	Tensilica, Inc.	Real Intent	MyCad, Inc.
10:15	CARDtools Systems	Axis Systems	Innoveda, Inc.	Aristo Technology, Inc.	Synchronicity, Inc.	Verplex Systems, Inc.
10:30	Beach Solutions	Icinergy, Inc.	Verisity Design, Inc.	CoWare, Inc.	Silicon Perspective Corp.	Mosys, Inc.
10:45	DesignSoft, Inc.	CAST, Inc.	IKOS Systems Inc.	AMI Semiconductor, Inc.	Fluence Technology	Genesys Testware
11:00	Lattice Semiconductor Corp.	Nassda Corp.	Sequence Design, Inc.	Ger2Chip.com, Inc.	0-In Design Automation	RUBICAD Corp.
11:15	QThink	Frontier Design, Inc.	BTA-Ultima	Chronology Corp.	Xilinx, Inc.	Interweave Tech. Corp.
11:30	Global UniChip Corp.	Incentia Design Systems, Inc.	Ansoft Corp.	Veritools, Inc.	Aptix Corp.	iRoC Technologies
11:45	Tanner EDA	Valiosys SA	Cadence Design Systems, Inc.	SynaptiCAD Inc.	Silicon Integration Initiative, Inc. (Si2)	Progate Group Corp.

12:00 – 2:00 LUNCH BREAK

Exhibitor Presentation Afternoon Schedule

Time	ROOM N102	ROOM N107-N108	ROOM N109-N112	ROOM N113-N114	ROOM N115-N117	ROOM N119-N120
2:00	Warhol Design Systems, Inc.	Intercept Technology Inc.	Mentor Graphics Corp.	Tera Systems Inc.	Co-Design Automation, Inc.	DSM Technologies, Inc.
2:15	APLAC Solutions Corp.	IMEC	C Level Design, Inc.	X-Tek Corp.	Simutech, LLC	QuickLogic Corp.
2:30	MOSIS	CreOsys Inc.	Avant! Corp.	TM Associates, Inc.	Concept Engineering GmbH	Proceler, Inc.
2:45	Target Compiler Technologies N.V.	TransEDA Technology Ltd.	Synplicity, Inc.	Novas Software, Inc.	Altera Corp.	FTL Systems, Inc.
3:00	UMC (USA) Group	OptEM Engineering Inc.	Synopsys, Inc.	InnoLogic Systems, Inc.	Circuit Semantics, Inc.	Platform Computing Inc.
3:15	Averant, Inc.	Intrinsix Corp.	Numerical Technologies, Inc.	Agilent Technologies	Simplex Solutions, Inc.	3DSP Corp.
3:30	Design Workshop	Runtime Design Automation	Monterey Design Systems	Simpod, Inc.	Alternative System Concepts, Inc.	Zaiq Technologies, Inc.
3:45	TILAB S.p.A.	ComCAD GmbH Analog Design Support	Artisan Components, Inc.	Silicon Metrics Corp.	CynApps	Y Explorations, Inc.
4:00	ATMOS Corp.	Integrated Measurement Systems	Magma Design Automation, Inc.	MEMSCAP	Barcelona Design	Legend Design Technology, Inc.
4:15	Cliosoft, Inc.	Analog Design Automation	Arexsys Inc.	Neo Linear, Inc.	Cypress Semiconductor	Celoxica, Inc.
4:30	TOPS Systems Corp.	Techmate Inc.	Tharas Systems Inc.	Electronic Tools Co.	Virtio	CMP
4:45	Nordic VLSI ASA	Interra Technologies, Inc.	Silicon Valley Research, Inc.	TSMC	Prover Technology Inc.	SynTest Technologies, Inc.
5:00	Random Logic Corp.	Sagantec	EDAToolsCafe.com	sci-worx Corp.	Actel Corp.	ChipData, Inc.
5:15	Willamette HDL, Inc.	ACE Associated Compiler Experts bv	Sonics Inc.	eASIC	Fintronic USA, Inc.	Esterel Technologies
5:30	PLATO Design Systems Inc.	MATRiCuS Inc.	Library Technologies, Inc.	OEA International, Inc.	CoVerify Solutions Inc.	Avery Design Systems Inc.
5:45	Gidel Ltd.	Morgan Kaufmann Publishers, Inc.	Virtual Silicon Tech	Cynergy System Design, Inc.	Integrated Systems Engineering, Inc.	@HDL, Inc.

@HDL, Inc. 5:45 pm
Unique adaptive verification solution that detects tough design problems automatically using formal, model checking and simulation based algorithms.

0-In Design Automation 11:00 am
0-In's smart verification products bring a rich library of assertions and the power of formal verification to a simulation-based methodology.

3DSP Corp. 3:15 pm
3DSP is a leader in digital signal processing solutions for embedded systems offering the industry's only configurable DSP architecture.

ACE Associated Compiler Experts bv 5:15 pm
CoSy based C compiler generation for architecture exploration.

Actel Corp. 5:00 pm
Reviewing the VariCore embedded IP cores, enabling the integration of reprogrammable logic functions in ASICs or ASSPs on standard processes.

Agilent Technologies 3:15 pm
Agilent EEsof EDA presents its Advanced Design System family of software products for designing state-of-the-art wireless communication systems.

Altera Corp. 2:45 pm
Altera presents system-on-a-programmable-chip (SOPC) solutions: Quartus™ II, APEX® Mercury, Excalibur embedded processor solutions, MegaCore™ and AMPP(SM) functions.

Alternative System Concepts, Inc. 3:30 pm
ADVANCED HDL SOLUTIONS -- ASC researches new technologies like XML and low-power while delivering VHDL/Verilog translators and other proven tools.

AMI Semiconductor, Inc. 10:45 am
AMI Semiconductor offers the only ASIC solution for high-density Virtex and Apex FPGAs with its targeted XLArray family.

Analog Design Automation 4:15 pm
The AMS Genius analog/mixed-signal/RF synthesis system designs the structure and parameters of circuits with multiobjective worst-case yield optimization.

Ansoft Corp. 11:30 am
Ansoft provides high performance solutions for IC packaging, high speed printed circuit boards (PCBs), RFICs and EMI analysis.

Antrim Design Systems, Inc. 10:00 am
Antrim's spec-driven approach to process migration and foundry re-targeting of mixed-signal IP through analysis, behavioral model characterization/generation, and design synthesis.

APLAC Solutions Corp. 2:15 pm
APLAC Solutions Corp. provides APLAC-Circuit Simulation and Design Tool for analog, RF-IC, RF Board and RF System designs. http://www.aplac.com

Aptix Corp. 11:30 am
Aptix is the leader in reconfigurable systems prototyping technology, delivering products to rapidly verify and debug complex system-on-a-chip (SoC) designs.

Arexsys Inc. 4:15 pm
Designing complex systems? The answer is a language independent co-design and co-verification methodology using Arexsys' advanced ArchiMate and CosiMate technology.

Aristo Technology, Inc. 10:15 am
Large Designs, Fast - Aristo addresses the physical design challenges of multi-million gate ASICs and SOCs, such as network and wireless communications processors.

Artisan Components, Inc. 3:45 pm
Artisan Components, provider of the industry's leading physical IP products, will present new developments in their end user and partner programs as well as highlight new product solutions.

Exhibitor Presentation Abstracts — Monday, June 18

ATMOS Corp. — 4:00 pm
Designers are pressed to meet ever-increasing performance. Learn how processors are connected through wide GHz buses to large embedded memories.

Avant! Corp. — 2:30 pm
Avant! Corporation, the fastest growing company in EDA history, will present its industry-leading solutions for 0.1 micron System-on-a-Chip design.

Averant, Inc. — 3:15 pm
Averant's Solidify, the breakthrough verification product. No changes to your code or synthesis flow, no simulators, no test vectors.

Avery Design Systems Inc. — 5:30 pm
Avery Design Systems delivers innovative C/C++ and Verilog HDL testbench automation and distributed simulation to advance verification quality levels and productivity.

Axis Systems — 10:15 am
Axis Systems lets you go "way beyond fast" with a single platform based on ReConfigurable Computing technology providing simulation, acceleration, emulation, hw/sw co-verification.

AXYS Design Automation, Inc. — 9:00 am
AXYS provides solutions shortening the SoC design cycle by enabling early system integration and software development based on fast and accurate virtual prototypes.

Barcelona Design — 4:00 pm
Barcelona accelerates analog circuit design for creating mixed signal chips. We offer analog compilers, design services, and analog design flow development.

Beach Solutions — 10:30 am
EASI-Studio automatically generates bus interface hardware, driver software, product reference manuals and test software, all from one common data source.

BOPS, Inc. Billions of Operations Per Second — 10:00 am
VoIP SOC in a Box is a full pre-packaged solution that includes hardware/software design and implementation services for a carrier-class VoIP gateway SOC.

BTA-Ultima Inc. — 11:15 am
BTA-Ultima physical signoff and design closure solutions build on Silicon Signature™ timing, interconnect, device physics and services expertise.

C Level Design, Inc. — 2:15 pm
Learn how companies are leveraging the power of C++ to dramatically improve simulation performance and designer productivity for their multi-million gate designs.

Cadence Design Systems, Inc. — 11:45 am
Cadence will present synthesis/place-and-route, verification, emulation, rapid prototyping, system-level, and high-speed PCB design solutions.

CARDtools Systems — 10:15 am
NitroVP allows for a virtual prototype that features complete hardware and software/firmware co-design and simulation. Allowing a smooth transition from design to implementation.

CAST, Inc. — 10:45 am
IP CORES & SERVICES -- See our latest 8- and 16-bit processors, peripheral and bus controllers, UARTs, and related functions.

Celoxica, Inc. — 4:15 pm
Celoxica will discuss how its unique DK1 design suite, featuring Handel-C, cuts hardware design cycles to weeks and days.

ChipData, Inc. — 5:00 pm
ChipData's Design Chain Management™ is standards-based, CAD-Ready data and browser-based applications for B2B PCB design collaboration via the Internet.

Chronology Corp. — 11:15 am
Come see how the QuickBench® Verification Suite™ provides testbench automation capability to meet the most complex SOC verification challenges within ever-tightening design schedules.

Circuit Semantics, Inc. — 3:00 pm
Circuit Semantics provides characterization and static timing solutions for high speed SOC design. Our technology is utilized for cell libraries, functional blocks and full chip design.

Cliosoft, Inc. 4:15 pm
Cliosoft, focused on collaboration and team productivity, demonstrates SOS - Data and Project Management System, integrated with design tools from Cadence™.

CMP 4:30 pm
CMP is a manufacturing broker for ICs, MCMs, and MEMS for prototyping and low volume production. Since 1981 about 3,400 projects for Research, Education and Industry have been prototyped.

Co-Design Automation, Inc. 2:00 pm
Looking for 10X verification productivity improvement? See how SUPERLOG™ and SYSTEMSIM™ can evolve your Verilog design and verification methodology.

ComCAD GmbH Analog Design Support 3:45 pm
SIZE! Will enhance your analog design capacitance. ComCAD offers a new quality of design support by inventing analog synthesis.

Concept Engineering GmbH 2:30 pm
Concept Engineering provides innovative schematic generation and viewing technology for commercial EDA vendors, in-house CAD departments and IC and FPGA designers.

CoVerify Solutions Inc. 5:30 pm
CoVerify Solutions provide tools that allow ASIC verification and embedded software engineers to develop software running on host with HDL simulators.

CoWare, Inc. 10:30 am
CoWare, the leader in system-level design, cuts SoC design time in half with a proven hardware/software co-design methodology and tools.

CreOsys Inc. 2:30 pm
Through innovative networking technologies, CreOsys delivers the software to connect and communicate independent of distance and time zone.

CynApps 3:45 pm
CynApps will present our technology for high-level design and verification at all levels of abstraction using our Open Platform solution.

Cynergy System Design, Inc. 5:45 pm
Bridging RTL and C standards - creation, integration, and distribution of fast, accurate Application Specific Virtual Prototypes (ASVPs) for SoC system verification.

Cypress Semiconductor 4:15 pm
Cypress's advanced CPLD solutions are truly "Driving the Communications Revolution". Warp™ development tools, the Delta39K, Quantum38K, and Programmable Serial Interface (PSI) families will be highlighted.

Denali Software, Inc. 9:30 am
Denali is the world-leading provider of memory solutions, from modeling, simulation, and verification, to high-performance memory subsystem IP.

Design Workshop 3:30 pm
Design Workshop offers a suite of highly customizable, multi-platform physical layout and verification tools. Stop by Booth #120 for demonstrations.

DesignSoft, Inc. 10:45 am
TINAPro is a powerful, easy-to-use analyzer and simulator software package for designing analog, digital, mixed, RF and VHDL electronic circuits.

DSM Technologies, Inc. 2:00 pm
Innovative Solutions for: Graphical Design Rule Entry - Automatic Physical Runset Generation - Foundation Libraries - Process Technology Deployment - Mixed Signal Design Environment.

Dynalith Systems, Inc. 9:45 am
Dynalith Systems markets an advanced emulation system for complex semiconductor integrated circuits, ASIC SoCs, which is called iSAVE (In-System Algorithm Verification Engine).

eASIC 5:15 pm
eASIC® offers a universal fabric configurable as logic, PLD or RAM, allowing flexibility, easy debugging and rapid, low-cost derivatives for SoC.

EDAptive Computing, Inc. 9:45 am
EDAptive will present an overview of its: HDL Based Design Tools, Test & Measurement Tools, Web Based Collaboration Tools, Training & Consulting.

Exhibitor Presentation Abstracts — Monday, June 18

EDAToolsCafe.com — 5:00 pm
EDAToolsCafe.com is the world's #1 EDA portal. More than 125,000 EDA professionals visit the portal each month for news, jobs and EDA resources.

Electronic Tools Co. — 4:30 pm
Come get your free copy of E-Studio that translates and visualizes design data. Use XML, EDIF, or native EDA databases.

Esterel Technologies — 5:15 pm
Esterel Studio, the ultimate development suite for trusted electronic devices and safe embedded softwares.

Faraday Technology Corp. — 9:15 am
Faraday Technology Corp. will present the total solutions including Faraday's leading edge IPs, libraries, DSM design flows and full turn key services.

Fintronic USA, Inc. — 5:15 pm
A new breakthrough in design verification will be presented.

Fluence Technology — 10:45 am
Join the test revolution with Fluence Technology's integrated suite of DFT and D2T tools including the industry's most comprehensive suite of BIST solutions.

Frontier Design, Inc. — 11:15 am
Automated C-based FPGA design flow offers highly parallelized implementations of complex DSP algorithms, while optimizing FPGA memory and register utilization.

FTL Systems, Inc. — 2:45 pm
System-level verification becomes reality with FTL Systems' Billion Gate Design Solution™ enabling analog and digital design using mainstream hardware.

Genesys Testware — 10:45 am
Genesys will present its Memory BistCore product that has a unique dynamic self-repair feature for improving embedded memory yield. It also provides BIST for CAMs.

Get2Chip.com, Inc. — 11:00 am
Get2Chip.com will demonstrate Volare, the world's first fully integrated front-end for SoC design in one common multi-level synthesis engine.

Gidel Ltd. — 5:45 pm
GIDEL will present an innovative and cost-effective solution for system development & verification involving, software and IP/SOIC. The solution is for systems with or without dedicated user's hardware.

Global UniChip Corp. — 11:30 am
Global UniChip speeds up your SOC design to market with three kind of business models: High valued silicon-proven IPs, SOC design service, and SOC turnkey solutions.

Icinergy, Inc. — 10:30 am
Icinergy Software develops and markets architectural floorplanning tools used in the early planning stages for System-on-Chip designs.

IDS-Insight Design Services — 9:30 am
Insight Design Services is a design consulting services for programmable logic and LSI Logic ASICs. Expertise in CPLD and FPGA, designers support the Xilinx product family.

IKOS Systems Inc. — 10:45 am
IKOS will show its new VStation 15M emulator capable of up to 15 million gates with full visibility.

IMEC — 2:15 pm
Designing Reconfigurable Networked Appliances using C++ Speaker: Paul Six, Associate Director DESICS Division, IMEC.

iMODL, Inc. — 9:15 am
iMODL provides automated functional verification tools, BFMs and protocol monitors for leading processors and I/O standards, including PCI-X and InfiniBand.

Incentia Design Systems, Inc. — 11:30 am
Abstract not available

InnoLogic Systems, Inc. 3:00 pm
By blending formal and existing approaches, InnoLogic's ESP-V products improve coverage, reduce simulation time and are easy to use.

Innoveda, Inc. 10:15 am
A broad range of tools that bridge gaps in the design process - system-level, PCB, enterprise integration and electro-mechanical.

Integrated Measurement Systems 4:00 pm
Integrated Measurement Systems (IMS) is a recognized leader in IC validation and virtual test engineering solutions for optimizing IC development.

Integrated Systems Engineering, Inc. 5:45 pm
ISE develops and supports TCAD, or Technology CAD, simulation software for predictive simulation of semiconductor processes and devices.

Intercept Technology Inc. 2:00 pm
Come see a demonstration of CONNEX, Intercept's new shape-based autorouter. Combined with Pantheon, CONNEX features robust and intuitive routing capabilities in a single, integrated application.

InternetCAD.com, Inc. 10:00 am
See what's new with Itools, InternetCAD.com's placement and routing package. We are the high quality, low cost solution for all of your IC designs.

Interra, Inc. 9:30 am
SpyGlass offers a new approach to RTL verification using structural analysis to spot problems not easily detected by other methods.

Interra Technologies, Inc. 4:45 pm
Interra Technologies, Inc. provides EDA building blocks (analyzers, RTL-synthesis, memory tools) and consulting services to EDA, semiconductor and SOC companies.

Interweave Tech. Corp. 11:15 am
Proliferate design methodology & power-user knowledge, Re-use design process solutions and collaborate with your global teams.

InTime Software, Inc. 9:15 am
DesignWarrior, an integrated RTL design environment with built-in performance prediction, eliminates the need for front-end designers to be physical experts.

Intrinsix Corp. 3:15 pm
The largest independent ASIC and System (SoC) product design company. Our highly experienced engineering teams architect, design and verify complex electronic systems.

IRoC Technologies 11:30 am
iRoC Technologies, leading Robust IP Provider, brings self-correcting intelligence to integrated circuits, protecting them from transient errors. Contact: info@irocтech.com.

Lattice Semiconductor Corp. 11:00 am
Lattice Semiconductor is the ISP performance and density leader with it's and SuperBIG™, SuperFAST™, SuperWIDE™ CPLDs, programmable Analog devices, and software.

Legend Design Technology, Inc. 4:00 pm
MemChar™ and BlockChar™ provide the complete solution for Memory and SOC Block Characterization. Their benefits are accuracy, performance and automation.

Library Technologies, Inc. 5:30 pm
We'll present our solutions for timing closure, clock skew, noise management, power and timing optimization, library generation and modeling tools.

Magma Design Automation, Inc. 4:00 pm
Visit the Magma Design Automation booth and see how our integrated synthesis, placement and routing solutions can help you meet your performance and time-to-market goals.

MATRICuS Inc. 5:30 pm
MATRICuS will demonstrate the newest features in LAYTOOLS including parameterized cells. The first EDA tool available in LINUX, see how LAYTOOLS creates a successful design environment.

Exhibitor Presentation Abstracts — Monday, June 18

MEMSCAP — 4:00 pm
MEMSCAP is a provider of innovative MEMS-based solutions for the design, development and manufacture of telecommunications products.

Mentor Graphics Corp. — 2:00 pm
Mentor Graphics will present its new tools and leading technology in HDL and FPGA design, system design, DSM and SoC Verification, and Embedded Software.

Model Technology Inc. — 9:45 am
Model Technology's ModelSim product line provides ASIC and FPGA designers with the latest in HDL simulation technology regardless of the language.

Monterey Design Systems — 3:30 pm
Monterey Design Systems™ demonstrates the most productive, fully open, highly integrated physical design solutions for high yielding DSM SoCs - Sonar™ & Dolphin™.

Morgan Kaufmann Publishers, Inc. — 5:45 pm
The new Morgan Kaufmann Series in Systems on Silicon offers state-of-the-art books by leading experts in design languages, design methodology, design automation, manufacture and test.

MOSIS — 2:30 pm
MOSIS presents a complete design flow (with a variety of options) for prototyping production compatible designs for TSMC, AMI, etc.

Mosys, Inc. — 10:30 am
MoSys' 1T-SRAM™ memory technology - already in volume production - enables semiconductor and system applications to embed ultra-dense memory using standard pure logic processes.

MyCAD, Inc. — 10:00 am
MyCAD provides complete solutions for IC design: IC Layout/Verification, VHDL, Synthesis, FPGA Prototyper at affordable cost on PC platforms.

Nassda Corp. — 11:00 am
Discover why over 70 companies have adopted HSIM™ for full-chip circuit simulation of their analog, mixed-signal, and SOC designs.

Neo Linear, Inc. — 4:15 pm
NeoCircuit and NeoCell automate custom analog cell synthesis and layout, while capturing the design constraints necessary for mixed-signal IP reuse.

Nordic VLSI ASA — 4:45 pm
Fabless SoC company, providing complex digital design, high speed data converters and 2,4GHz wireless modules. Your idea is the challenge - we provide solutions!

Novas Software, Inc. — 2:45 pm
Novas, the debug leader, presents our latest products to help you locate, isolate, and understand the causes of design bugs.

Numerical Technologies, Inc. — 3:15 pm
The First 70 people to bring this program to our exhibitor presentation will get a free 007 DVD.

OEA International, Inc. — 5:30 pm
Providing high accuracy 3D extraction and design planning software solutions for chip level critical power, signal, bus and clock nets.

OptEM Engineering Inc. — 3:00 pm
OptEM presents interconnect analysis and device extraction tools for digital designers concerned with inductive, frequency dependent and lossy transmission line effects.

Platform Computing Inc. — 3:00 pm
Designing to the multimillion-gate level presents tremendous challenges. LSF-enabled EDA tools allow these challenges to be addressed directly.

PLATO Design Systems Inc. — 5:30 pm
Routing Multi-million Gate SoC Designs: Plato brings new physical design solution with concurrent routing, extraction, analysis and interconnect optimization.

Proceler, Inc. — 2:30 pm
Proceler will demonstrate technology that creates high-performance, application-specific soft processors directly from high-level application source code written in standard C/C++.

Progate Group Corp. 11:45 am
RTL to chip design service company - Progate Group Corporation.

Prolific, Inc. 9:00 am
Dynamic Cell Creation is the beginning of a technology that will dramatically change the way standard cell libraries are developed and deployed.

Prover Technology Inc. 4:45 pm
Prover Technology will show how proof engines turbo-charge EDA tools - dramatically improving design time for circuits and systems.

Provis Corp. 9:30 am
Simulation for the power user! Z01X! is the only simulator using clustering technology for faster simulations, higher capacity and scalability.

QThink 11:15 am
It's your IP. Find out how QThink's unique approach to IP ownership is revolutionizing the design services market.

QuickLogic Corp. 2:15 pm
QuickLogic's new QuickSD™ ESP Family integrates up to eight 1 Gb/s Bus LVDS SERDES transceivers with embedded memory and customizable logic to create single-chip communications solutions.

Random Logic Corp. 5:00 pm
Random Logic Corporation presents QuickCAP® v. 4.0, gdsIISeries™ RC and RLC products, and Auxiliary Tools™, for interconnect circuit characteristics extraction.

Real Intent 10:00 am
Real Intent will present Verix, its easy-to-use Intent-Driven formal verification system for VHDL/Verilog functional verification.

RUBICAD Corp. 11:00 am
RUBICAD will present innovative solutions for physical design to achieve design closure in next generation nanometer-scale chips and silicon systems.

Runtime Design Automation 3:30 pm
Runtime Design Automation develops and markets design management tools that address the challenges of SOC, DSM, and IP reuse. The Flow Tracer family of products automates flow creation, management, and execution.

Sagantec 5:00 pm
Proven design acceleration solutions for full-custom layout implementation of high-performance cores, memories and analog designs in latest technology.

sci-worx Corp. 5:00 pm
sci-worx will present its leading-edge HW/SW DesignObjects® and its SoC platform solutions for communications & secure applications.

Sequence Design, Inc. 11:00 am
Sequence Design, Inc. presents timing, power and signal integrity solutions essential for next generation system-on-chip design closure beyond 180 nanometers.

Silicon Integration Initiative, Inc. (Si2) 11:45 am
Silicon Integration Initiative, Inc. (Si2) provides engineering consultation and services to industry-leading silicon, electronic systems and EDAcompanies. (www.Si2.org)

Silicon Metrics Corp. 3:45 pm
Silicon Metrics, the Timing Sign-off Company, will be presenting ASIC and Fabless nanometer design timing sign-off advancements utilizing its SiliconSmart family of products.

Silicon Perspective Corp. 10:30 am
Creating a physical prototype that establishes the feasibility of the netlist shortens the design cycle of large SoCs.

Silicon Valley Research, Inc. 4:45 pm
SVR presents QIC/APR 2.0 a fast, high capacity (over 1 million gates) place and route system for cell-based designs using deep submicron technology.

Exhibitor Presentation Abstracts — Monday, June 18

SiliconCraft Inc. — 9:30 am
SiliconCraft demonstrates NeoTime STA and circuit optimizer, NeoPower. By SiliconCraft's Fab-proven technology, your timing and power can be optimized concurrently in most efficient way.

Silvaco International — 9:30 am
Silvaco CEO, Ivan Pesic will discuss Silvaco's involvement in the first multi-vendor tool flow available online on e*ECAD's pay-per-use portal.

Simplex Solutions, Inc. — 3:15 pm
Simplex presents design technologies, methodologies, and silicon engineering expertise for the design and verification of advanced SoC designs.

Simpod, Inc. — 3:30 pm
Simpod's modeling technology speeds design and verification of embedded systems. DeskPOD™ models, all-in-one solution, are absolutely accurate and faster than full-function software models.

Simucad, Inc. — 9:45 am
NEW! The SILOS® III Verilog HDL Logic Simulator now includes a Finite State Machine module and a Code-Coverage tool.

Simutech, LLC — 2:15 pm
Simutech's enables IP reuse, e-commerce, and rapid SoC development. Its products enable web based technical evaluation, HW/SW development, and SoC verification.

Simutest, Inc. — 9:15 am
Test Problems? Simutest has full range of engineering productivity improvement solutions for design to test including Verifier and Release Wizard software New!

Sonics Inc. — 5:15 pm
Sonics provides highly configurable, on-chip MicroNetworks for integrating multiple IP cores into high performance SOCs with demanding complex data flows.

Sun Microsystems — 9:00 am
Sun's presentation will outline a high-performance, distributed computing architecture targeted to DSM IC design.

SynaptiCAD Inc. — 11:45 am
Vera, SystemC, VHDL, and Verilog Graphical Testbench Generation! Automatically generate bus-functional models, sequence recognition code, protocol checkers, and split-phase transactions.

Synchronicity, Inc. — 10:15 am
Learn how Synchronicity's popular internet-based solutions for design management, team collaboration and design reuse will raise your development productivity.

Synopsys, Inc. — 3:00 pm
Synopsys, the leading EDA design tool provider, will showcase its latest product and service offerings covering key design flow areas.

Synplicity, Inc. — 2:45 pm
Synplicity supplies logic and physical synthesis technologies which enable ASIC and FPGA designers to achieve simply better results.

SynTest Technologies, Inc. — 4:45 pm
SynTest offers DFT Tools, Services and Consultancy for IC/SoCs from Chip Design to Tape-out, including BIST, Scan Synthesis, ATPG, Fault Simulation etc.

Tanner EDA — 11:45 am
Tanner EDA delivers powerful custom IC design solutions for PCs to address the challenges of analog, RF, and mixed-signal IC design.

Target Compiler Technologies N.V. — 2:45 pm
Discover Chess/Checkers v2, Target's retargetable compilation environment for application-specific processors with extended support for deep pipelining and automatic HDL generation.

Techmate Inc. — 4:30 pm
Techmate presents a Design Management Environment, Physical Hardware, Modeler and Contractor Services for ASIC/FPGA development.

Tensilica, Inc. — 10:00 am
Tensilica is the leading provider of configurable RISC and DSP cores and associated software development tools for single-chip embedded systems.

Tera Systems Inc. 2:00 pm
Discover how the TeraForm RTL design planner enables interactive front end design exploration, RTL signoff, and back - end timing convergence for high - performance ASICs.

Tharas Systems Inc. 4:30 pm
Tharas Systems offers hardware accelerated HDL simulation with fast compile times, tremendous speed, in the context of your existing simulation environment.

TILAB S.p.A. 3:45 pm
CSELT introduces you to IPs, platforms and solutions for next generation mobile equipment, access and networking appliances, advanced optical architectures.

TM Associates, Inc. 2:30 pm
TM Associates offers a complete complement of Verilog & VHDL training courses taught by independent, industry-leading consultants.

TOPS Systems Corp. 4:30 pm
TOPS Systems present the solution to the complex SoC Verification need with Virtual Prototyping, already proven with heterogeneous multiprocessor, MISC.

TransEDA Technology Ltd. 2:45 pm
Highlighting Verification Navigator, an integrated design verification environment with Configurable HDL Checking, Coverage Analysis, FSM Analysis, Test Suite Analysis.

Translogic USA Corp. 9:15 am
Ease5.0 TeamEdition fully supports SoC-projects. Enabling design-teams to work concurrently in a Graphical design-environment, specifying Asics or FGPAs in Verilog/VHDL.

Triscend Corp. 9:45 am
Triscend will present its Configurable System-on-Chip, combining a processor sub-system with embedded programmable logic to offer a flexible off-the-shelf system-on-chip solution for fast time-to-market.

TSMC 4:45 pm
A designer's foundry industry perspective including 300mm and 0.10µm insights and the latest web-based design and engineering collaboration capabilities.

UMC (USA) Group 3:00 pm
UMC provides designers with choices in logic and mixed-signal transistors, RF and mixed-mode high-performance passives, eSRAM, eDRAM, and silicon-proven libraries and IP cores.

Valiosys SA 11:45 am
Verification bottleneck? Valiosys' imPROVE model checking tool and TLL transistor abstraction tool can help!

Verisity Design, Inc. 10:30 am
Functional verification automation to verify your most complex designs faster and more efficiently than ever before. Verification in Motion.

Veritable, Inc. 9:00 am
Veritable Inc. provides formal validation solutions that combine the usability of traditional checking tools with the power of formal verification.

Veritools, Inc. 11:30 am
From C++ to transistors, Undertow Suite source code debugging now includes SystemC, Verilog, VHDL, combination VHDL/Verilog and mixed mode digital/analog.

Verplex Systems, Inc. 10:15 am
Verplex provides the highest performance and easiest to use formal verification products, yielding full-chip functional closure from RTL to GDSII.

Virage Logic Corp. 9:45 am
Virage Logic, the leader in embedded memory, will showcase compilers and software that enable the development and reuse of memories.

Virtio 4:30 pm
INNOVATE SOFTWARE ON SOFTWARE. Experience the no-hardware solution to software development now at booth 518.

Virtual Component Exchange 9:15 am
To solve the problems hindering trading of third party SIP, the VCX has developed www.thevcx.com , find out how it works.

Exhibitor Presentation Abstracts — Monday, June 18

Virtual Silicon Technology — 5:45 pm
Virtual Silicon - IP Buildiing Blocks for SOC Design.

Warhol Design Systems, Inc. — 2:00 pm
Warhol's physical solutions for SoC including hierarchical placement, dynamic gridless routing, and logic restructuring guarantee circuit efficiency as well as 100% routing completion rates.

Willamette HDL, Inc. — 5:15 pm
Willamette HDL, Inc. demonstrates AccurateC™, a language rule checker for C/C++-based electronic design and the system-level design modeling platform, SystemC.

X-Tek Corp. — 2:15 pm
X-CDE utilizes high-level sets of properties to determine that your design functions as specified without unnecessary simulation.

Xilinx, Inc. — 11:15 am
The Xilinx vision of integrated, internet enabled software for ultra high density FPGAs and low power CPLDs will be presented by Bill Gregorak.

Xpedion Design Systems, Inc. — 9:00 am
Xpedion presents the GoldenGate product family, delivering the next generation of RF / 3G Wireless / Broadband simulation and modeling, from circuits to systems.

Y Explorations, Inc. — 3:45 pm
YXI presents high-level synthesis and automatic reuse taking you from behavioral "C"-based, VHDL or Verilog to synthesizable RTL.

Zaiq Technologies, Inc. — 3:30 pm
Zaiq is presenting Design Solutions in Wireless, Broadband and Optical domains, as well as the development of Intellectual Property Solutions.

Zuken USA — 9:00 am
Zuken provides proven world-class design solutions, including the very latest HDI and 3D technologies that help you Be First™- every time.

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The 38th Design Automation Conference is sponsored by the **ACM/SIGDA** (Association for Computing Machinery/Special Interest Group on Design Automation), **IEEE/CAS** (Institute of Electrical and Electronics Engineers/Circuits and Systems Society), and the **EDA Consortium** (Electronic Design Automation Consortium). Membership information is available on pages 60 - 63 or at the conference at the ACM and IEEE booths. **Join before registering and save**.

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SIGDA/DAC University Booth

Each year SIGDA organizes the University Booth. The booth is an opportunity for university researchers to display their results and to interact with visitors from industry. Priority is given to presentations that complement the conference technical program. Demos that highlight benchmark results are also encouraged. The Design Contest winners will give demonstrations presenting their designs at the University Booth, Tuesday, 12:00PM - 2:00PM. The schedule of presentations will be published at the conference and will also be available on the SIGDA website. We thank the Design Automation Conference for its continued support of this project.

EDA Consortium

Formed in 1989 the EDA Consortium is an international association of companies engaged in the development, manufacture, and sale of design tools and services to the electronic engineering community.

The Consortium Enhances the EDA Industry's Efficiency and Perceived Value by:

- Leading forums to discuss industry issues
- Maintaining a centralized web site
- Sponsoring the DAC and DATE (Europe) conferences
- Reporting revenue data on the EDA market
- Recognizing excellence through:
  · Phil Kaufman Award · Design Achievement Awards
- Supporting emerging EDA companies

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- Invitations to Consortium events
- Member discounts on:
  - DAC & DATE exhibit spaces
  - Market Statistics Service - the only source for quarterly EDA revenue data

For more information, contact EDA Consortium, 111 West Saint John Street, Suite 220, San Jose, CA 95113, Phone: (408) 287-3322, Fax: (408) 283-5283, E-mail: info@edac.org, Web site: www.edac.org.

ACM/SIGDA Membership Application

SIGDA focuses on all aspects of computer-aided design of electronic systems, including simulation, synthesis, verification, graphics, test benchmarking, layout design for manufacturing and packaging, documentation, and frameworks. Its goals are to provide information, organize conferences and workshops, and enhance the Design Automation conferences and workshops.

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For more information on both SIGDA & ACM contact ACM directly at: 1 (800) 342-6626 (U.S.A & Canada) or 1 (212) 626-0500 (global), by fax at: 1 (212) 944-1318, e-mail: acmhelp@acm.org, or by writing to ACM Member Services Department, P.O. Box 11315, New York, NY 10286-1315.

SIGDA Member Benefits include:

- The Annual CD-ROM Conference Proceedings Compendium and Multimedia
- Subscription to the SIGDA newsletter
- Discounted rate for SIGDA journal on Design Automation
- Discounts at SIGDA Sponsored Conferences
- Travel grant eligibility

Your Contact Information

Name _____

Address _____

City/State/Province _____

Country/ZIP/Postal Code _____

Email _____

Phone _____

Fax _____

ACM Member # _____

Payment Information

❑ check/money order (payable to ACM) Credit Card: ❑ AMEX ❑ VISA ❑ MC

Card # _____ Exp. Date _____

Signature _____

Please send completed application to the address mentioned above. **Thank you!**

Professional Membership

❑ **ACM and SIGDA**	**$110**
❑ Add Expedited Air (outside N.America)	**$43**
❑ Add ACM Digital Library	**$90**
❑ **ACM only**	**$95**
❑ Add Digital Library	**$90**
❑ **SIGDA only**	**$15**

I certify that I have met one of following criteria:
• Bachelor's Degree (in any area) or • Equivalent Level of Education or
• Two years full-time employment in the IT field

Signature: _____

Student Membership

❑ **ACM and SIGDA (includes DL)**	**$53**
❑ Add Expedited Air	**$43**
❑ **ACM only (includes the DL)**	**$38**
❑ **SIGDA only**	**$15**

You MUST complete the following to qualify:

College or High School: _____

❑ Fresh ❑ Soph. ❑ Jr. ❑ Sr. **Major:** _____

Expected date of Graduation: _____

Student Design Contest/Additional Meetings

Student Design Contest

The purpose of the Student Design Contest is to promote excellence in the design of electronic systems by providing competition between graduate and undergraduate students at universities and colleges. This year we received submissions in two categories: 'Conceptual' and 'Operational.' Operational designs are those which have been implemented and tested. Conceptual designs have not yet been fabricated and tested but must have been thoroughly simulated.

Students compete for cash prizes donated by a number of industrial sponsors and by DAC itself. This year the total prize money is $23,500. Prizes will be awarded at a special luncheon during the conference. Prize winners will be listed in the final program and have been invited to show their work at the SIGDA/DAC University Booth on the show floor. In addition, three of the submissions have been included in this year's technical program (see pages 17, 33, 35).

Birds-Of-a-Feather (BOF) Meetings

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather". All BOF meetings are held at the Las Vegas Hilton, Wednesday, June 20, 2001, 6:00PM - 7:30PM. DAC will facilitate common interest group meetings to discuss DA related topics. To arrange a BOF meeting contact the DAC office at mpa@dac.com or sign up at the Information Desk at-conference. A room will only be assigned if ten or more people sign up. A viewgraph projector and screen will be provided on request. Check DACnet and the Birds-of-a-Feather board at the Information Desk.

ACM/SIGDA Ph.D Forum

ACM/SIGDA will hold a semi-annual meeting after the cocktail party on Tuesday evening, June 19, 2001, from 7:00PM to 9:00PM in room N250. A light dinner will be served. The primary focus of the meeting will be the fourth annual Ph.D. Forum. The meeting is open to all members of the DA community.

The Ph.D. Forum, hosted by SIGDA, aims to strengthen the ties between academic research and industry. During the SIGDA meeting, students will use posters to discuss their Ph.D. thesis work with interested attendees. This session will provide the students an opportunity to receive feedback on their work. It also previews academic work-in-progress to the DA community. For more information about the Forum, please visit http://www.sigda.acm.org/Programs/PHDForum. SIGDA members and non-members are invited.

Proceedings

ACM/SIGDA (Association for Computing Machinery/Special Interest Group on Design Automation) and the Design Automation Conference will jointly publish the proceedings of DAC'01 on CD-ROM. Papers can be accessed using Adobe Reader 4.0 (included on the CD-ROM). DAC Proceedings will also be available on the World Wide Web after the conference.

A compendium CD-ROM containing the conference proceedings from the previous year is published annually, beginning with the Compendium'94 (containing DAC, EURO-DAC, and ICCAD). Compendium'99 contains ASP-DAC'99, DAC'99, DATE'99, ICCAD'99 and proceedings from four symposia (FPGA'99, ISLPED'99, ISPD'99, and ISSS'99). Compendium'00 will include ASP-DAC'00, DATE'00, DAC'00, ICCAD'00, FPGA'00, ISPD'00, ISLPED'00, CODES'00, and ISSS'00. SIGDA conference proceedings on CD-ROM and Compendium CD-ROMs are available from ACM. Stop by the ACM Booth for further information.

TODAES

Transactions on Design Automation of Electronic Systems (TODAES)

TODAES will be your pulse in the rapidly changing field of design technology of electronic systems. TODAES will keep you current in the areas of system design, high level synthesis, physical layout, design verification, system reliability, and high performance circuits. TODAES subscriptions are available in three formats: print (includes an annual CD-ROM), online, or both.

	ACM member	ACM/SIGDA member	ACM student member	ACM/SIGDA student member	SIGDA only	Non-Member
print...	$34	$24	$29	$19	$165	$175
electronic...	$27	$17	$23	$13	$130	$140
print & electronic...	$41	$31	$35	$25	$200	$210

38th DAC Proceedings

The 38th DAC proceedings will contain 160 papers, panels, and special invited presentations. DAC is offering each conference and student registrant the proceedings in both the hardbound edition and the CD-ROM edition. Should you wish to purchase any additional copies you may do so at the ACM booth for $50.00. After the conference, mail orders should be sent to ACM; approximate cost after conference is $70 for members, and $140 for non-members ACM should be contacted before placing your order to determine cost and availability of the proceedings. The address is:

ACM Order Department
P.O. Box 11315
New York, NY 10286-1315

1 (800) 342-6626 (U.S. and Canada)
1 (212) 626-0500 (all other countries)

Fax: 1 (212) 944-1318
e-mail: orders@acm.org

Las Vegas Attractions

Las Vegas Attractions

Las Vegas is the entertainment capital of the world! Plush resort hotels, lavish shows, and non-stop casino action attract people worldwide. Venture down the neon lit "Strip" to visit "New York" or "Venice", the Lion Habitat at the MGM Hotel, or witness a fight between two pirate ships in front of the Treasure Island Hotel. The city has many casinos, restaurants, golf courses, nightclubs and lounges. Four recommended shows are The Blue Man Group, Cirque du Soleil ('Mystere' and 'O' shows), and Siegfrid and Roy. There are many other near-by attractions which are easily accessible by tour or car. To mention just a few: Lake Mead and Hoover Dam, Red Rock Canyon and Old Nevada, a replica of an old western fort. These are within a thirty minute drive from the city. For those wishing to wander a bit farther, there is the Grand Canyon. Each hotel provides a tour reservation desk for your convenience. Tickets for shows in the area can be purchased there as well.

Viva Las Vegas Party - Wednesday, June 20, 2001, 7:30-10:30pm

Hilton Center at the Las Vegas Hilton *(next door to the Convention Center.)*

"The King" returns to Las Vegas: "Elvis" and the band Night Shift will entertain attendees while they enjoy great food. There will be carving and pasta stations, hors d'oeuvres, canapes, espresso and desserts. Enter the DAC party through the giant casino chips and down the red carpet into the Hilton Center.

Guest/Family Program

A $45 registration fee will admit each guest or family member to the following:

1. Tuesday night Cocktail Party at the Las Vegas Convention Center
2. Wednesday night 38th DAC "Viva Las Vegas" Party in the Las Vegas Hilton
3. Use of the complimentary shuttle bus services between all DAC participating hotels and the Las Vegas Convention Center
4. Admission to the exhibit hall when accompanied by an attendee.

Registration for the Guest/Family Program will be at the Conference Registration desk on Sunday, June 17 through Wednesday, June 20, 2001. A badge will be provided for each registered guest or family member. This badge must be worn to participate in the above activities. Look for the Guest Registration sign in the registration area. Children under the age of 14 are not allowed in the exhibit hall or demo suite area.

Weather

Las Vegas has an average daytime temperature reaching from 90 to over 100 degrees with very low humidity. Summer clothing is appropriate with a light jacket or sweater for evenings in the air-conditioned night spots. Casual attire is recommended for the Conference itself and is acceptable in most restaurants.

Air Transportation / Rental Cars / Busing

Conference Shuttle Bus Service

Complimentary shuttle bus service is provided for all DAC registered conference attendees, exhibitors, and guest program participants. Day and Evening Route busing will be provided to and from the Las Vegas Convention Center and all participating DAC hotels, except the Las Vegas Hilton. Hours will be extended to accommodate the DAC Demo Suite attendees. At 7:00 PM Wednesday night the buses will run from all DAC hotels to the Las Vegas Hilton until 1:00 AM.

Day Route Schedule (service every 10–15 minutes)

Sunday, June 17	2:00 PM - 6:30 PM
Monday, June 18	7:00 AM - 11:00 PM
Tuesday, June 19	7:00 AM - 11:00 PM
Wednesday, June 20	7:00 AM - 1:00 AM
Thursday, June 21	7:00 AM - 7:00 PM

Busing Routes and Designated Stops

ROUTE 1 Riviera	PICK-UP LOCATION Convention Entrance
ROUTE 2 Bally's	PICK-UP LOCATION Tour Bus Ramp
ROUTE 3 Paris	PICK-UP LOCATION Tour Bus Plaza

Rental Cars

This year DAC has arranged discounted rates with Dollar Car Rental. To receive this rate mention the DAC reference number CON22 when making your reservation. Dollar Car Rental 1-800-800-4000. Cars may be picked up at the airport or the Las Vegas Hilton.

Car Class	Daily	Weekly
Compact	$25	$130
Full Size 4-Door	$35	$180
Luxury	$55	$280

DAC Airlines

United Airlines United Airlines is one of two official DAC airlines. Receive either 5% discount off any United, United Express or Shuttle by United published fares for scheduled service in the U.S. and Canada or 10% discount off applicable BUA fares in effect with no advance purchase. United offers an additional 5% discount towards the purchase of tickets at least 60 days in advance of travel. Travel dates to/from Las Vegas include June 13-24, 2001. Meeting ID Code: **560EP**. Please reference this ID when you or your travel agent call United Meetings desk at **1-800-521-4041**.

Continental Airlines Continental Airlines is also offering discounts to DAC participants. Travel dates are June 13-27, 2001. Call **1-800-468-7022** and reference the following codes: **I0S31P + Z Code: ZGMK.** Receive either a 5% or 10% discount within the U.S. and Canada, depending on class of service. Continental offers an additional 5% discount towards the purchase of tickets at least 60 days in advance of travel.

Getting from the Airport

Proceed to the shuttle departure area, outside baggage claim. Prices range from $4 to $6 per person to "the Strip" or downtown hotels. Taxis are also available from the airport outside baggage claim.

Housing

Handicapped Access/Special Needs

The Conference policy has always been to fully cooperate with any attendee who has a special need or requirement. If you have a special need, we ask that you contact the DAC office at (303) 530-4333 so that we may personally handle this matter for you. If you require special hotel accommodations, please indicate that on your hotel reservation form.

Housing

The DAC Office will NOT handle room reservations.
ALL room reservations MUST be made DIRECTLY with
The Las Vegas Convention/Visitors Authority.

Las Vegas Convention Center/Visitors Authority
3150 Paradise Rd.
Las Vegas, NV 89109-9096
phone: (888) 892-5822
fax: (702) 386-7818

Four hotels in Las Vegas are participating with discounted room rates for the 38th DAC. A hotel reservation form is on page 70. Make your reservations now.

Available Housing Fills Quickly! Make Your Reservations Early!

Reservation requests will be handled on a first-come first-serve basis by the Las Vegas Convention Center/Visitors Authority. A first night's room and tax deposit is required. Confirmations will be made by Las Vegas Convention Center/Visitors Authority. The special DAC rates will be honored on all reservations made by May 17, 2001, pending availability.

Las Vegas Convention Center/Visitors Authority will attempt to make your reservations as indicated by the choice of hotels you specify. If the hotels you choose are not available, Las Vegas Convention Center/Visitors Authority will make your reservation at an available Conference hotel.

Before sending hotel reservations, check availability on the web at www.dac.com.

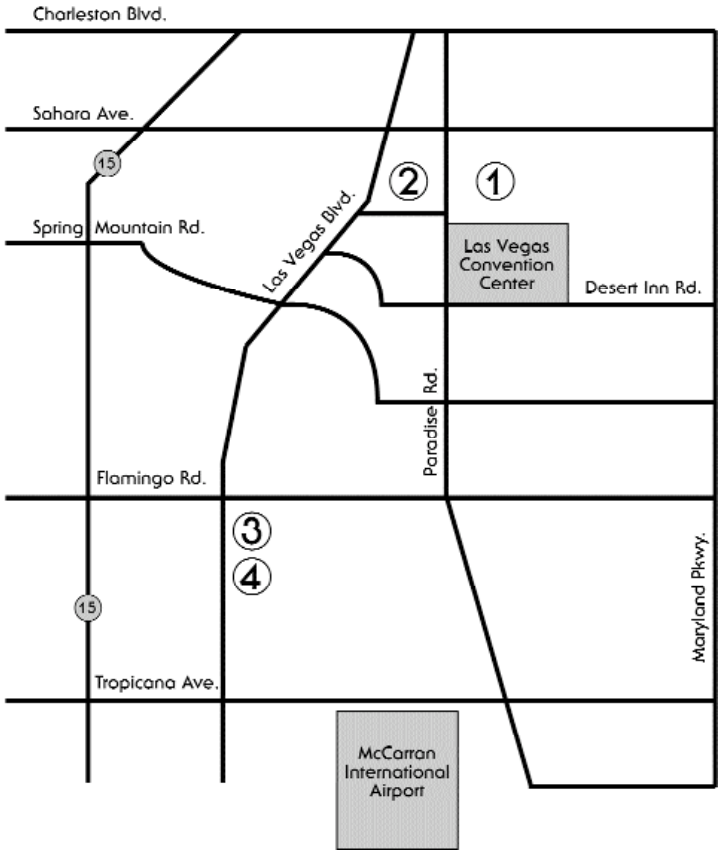
See page 69 for a map of the Las Vegas hotels.

NOTE: All meetings and exhibits will be at the Las Vegas Convention Center with the exception of the Tuesday Opening Session and Keynote, which will be held at the Las Vegas Hilton Pavilion. All full-day tutorials will be held at the Las Vegas Convention Center.

Las Vegas City Map

Hotel Key

1) Las Vegas Hilton
2) Riviera Hotel & Casino
3) Bally's Las Vegas
4) Paris Las Vegas



Hotel Registration Form

registration is also available at www.dac.com

Hotel reservations, changes, and cancellations are handled by the Las Vegas Convention/Visitors Authority prior to **May 17, 2001**. All reservations are made on a first-come-firstserved basis. Before sending hotel reservations, check availability on the web at www.dac.com, or call 1 (888) 892-5822. The following hotels are available:

HOTEL (prioritize your choices)	RATE (choose one) single	double	HOTEL (prioritize your choices)	RATE (choose one) single	double
_____ **Las Vegas Hilton**	$120	$120	_____ **Paris Las Vegas**	$124	$124
_____ **Bally's Las Vegas**	$104	$104	_____ **Riviera Hotel & Casino**	$ 81	$ 81

Above rates honored only if your reservation is made by **May 17, 2001**. The Las Vegas Convention/Visitors Authority will attempt to make your reservations as indicated by the choice of hotel(s) you specify. If the hotel(s) you choose are not available, the Las Vegas Convention/Visitors Authority will make your reservation at an available Conference hotel.

RESERVATIONS SENT TO THE DAC OFFICE WILL BE DISCARDED!

Send deposit check or credit card information with completed form to: Las Vegas Convention Center/Visitors Authority, 3150 Paradise Rd., Las Vegas, NV 89109-9096 — phone: (888) 892-5822, fax: (702) 386-7818

All reservations will be processed by mail, toll-free phone, internet and fax. Hours of operation are 7:00AM - 5:00PM PST.

Name _____Company _____

Phone _____Fax: _____

Mailing Address _____

City _____State _____Zip _____E-mail Address_____

Arrival Date _____ Departure Date _____ Sharing with_____

Room Type: ❑ single 1 bed ❑ double 1 bed ❑double 2 beds ❑ triple ❑ quad ❑ ADA accessible room requested

Special Request (ie smoking) _____Reservations will be confirmed by the Las Vegas Convention/Visitors Authority.

CREDIT CARD INFORMATION AMEX_____Visa_____MC_____Discover_____Diners_____Cardholder Name _____

Number _____Exp. Date _____Cardholder Signature _____

Your credit card will be billed for the first night's room and tax deposit. If you prefer to guarantee by check, **make check payable to the hotel** after you receive your acknowledgement from the Las Vegas Convention/Visitors Authority. Check must be in U.S. dollars drawn from a U.S. bank, wire transfers will not be accepted. All changes should be processed by phone or fax with the Las Vegas Convention/Visitors Authority until May 17, 2001. Cancellations occurring after May 17, 2001 and prior to 14 days of arrival date are to go directly to the hotel for a full refund. Cancellations made less than 14 days of arrival date will lose the complete deposit.

Index

Registration Instructions

7 Easy Steps

1. Complete Attendee Information
2. Complete Membership Status
3. Complete Tutorial/Workshop Selection
4. Complete Registration Options
5. Complete Payment Information
6. Complete Attendee Survey
7. Submit via fax, mail or on-line along with payment:

38th Design Automation Conference
Attn: Registration Desk
5305 Spine Rd., Ste. A
Boulder, CO 80301
TEL # (303) 530-4333
FAX # (303) 530-4334

FOR INFORMATION ONLY, CALL (800) 321-4573.

A. Payment MUST be included with the registration form or it WILL be discarded.
B. Registration may be charged to Visa, Mastercard or American Express. For credit card payment include the complete credit card number, expiration date, and name on the card.
C. If payment is received from a non-U.S. bank, the attendee will be charged a collection fee of $30.00.
D. **May 21, 2001** is the **DEADLINE** to qualify for the advanced registration rate. Payment transactions must be completed on or before May 21, 2001 in order to receive the early registration rate. After May 21, 2001, early registrants with incomplete payment information will be required to pay the higher conference rate.
E. The DAC office will continue to accept registrations until May 29, 2001, at the at-conference rate. After May 29, 2001, all registration must be done at conference.
F. Register ONE person per form (copy form as needed).
G. Refund Policy: Written requests for cancellations must be received in the DAC office by May 21, 2001, and are subject to a $25.00 processing fee. Cancellations received after May 21, 2001 will NOT be honored and all registration fees will be forfeited.
H. Membership number must be included at time of submission to receive the membership rate. No refunds will be made for change in membership status. If you would like information on becoming an IEEE or ACM member, refer to pages 60-63.

DAC Social Events include: coffee breaks, Tuesday Cocktail Party and the Wednesday Night Party.

Registration Hours

Sunday, June 17, 2001 .....8:00 AM to 4:00 PM
Monday, June 18, 2001 .....8:00 AM to 6:00 PM
Tuesday, June 19, 2001 .....7:30 AM to 5:00 PM
Wednesday, June 20, 2001 .....7:30 AM to 5:00 PM
Thursday, June 21, 2001 .....7:30 AM to 3:00 PM

Students

A special student rate applies to individuals who are members of IEEE or ACM and are currently enrolled in school. Students who advance register must include a valid IEEE or ACM student membership number and a valid student ID. Students registering at conference must present a valid IEEE or ACM membership card and a Student ID. Student registration includes a copy of the proceedings and all social events.

One/Two Day Registration

One/Two day only registration includes: the day(s) you select for the Technical Conference, all three days of the Exhibits, and the proceedings in both the hard edition and CD-ROM. One/Two Day only registration does not include Wednesday Night Party.

Tutorials

Full-day tutorials are offered on Friday, June 22, 2001. You must register for at least one day of the Technical Conference to attend a tutorial. Tutorial registration fee includes: continental breakfast, lunch, breaks, and tutorial notes. See pages 36-41 for tutorial descriptions. Space is limited to the first 125 persons. If your tutorial selection is filled and you do not indicate a second choice on the registration form, we will refund the tutorial registration fee. For tutorial availability, check the DAC website.