About the Conference

The 39th Design Automation Conference is a high quality professional forum for technology interchange among design automation researchers and developers, the engineers who use DA systems to design, test and manufacture circuits and systems, and the vendors who provide both electronic design automation (EDA) systems and silicon. Five full days of activities are planned, including a rich technical program of research and case study papers, panels and tutorials, and an exhibition of the latest in EDA products and services. The conference this year will again highlight the convergence of embedded systems software design tools and EDA hardware design tools in support of large complex systems on a chip. This is reflected in the "Embedded Systems Showcase" on the exhibit floor, a panel session on "Unified Tools for SoC Embedded Systems", the Thursday keynote address by Jerry Fiddler, Chairman and Founder of Wind River, and a number of technical sessions sprinkled throughout the program.

The Technical Program consists of panel discussions, special (invited paper) sessions, and technical paper sessions. The Tuesday morning keynote will be presented by Dr. Hajime Sasaki, Chairman of the NEC Corporation, speaking on new challenges likely to be faced by the CAD industry. From there, the technical program is organized around two tracks. The Design Tools track focuses on new techniques for enhancing the performance and capabilities of EDA tools. The Design Methods track focuses on the results and insights gained by applying EDA tools to actual system designs. There are eight panel discussions covering topics that range from the relationship between Wall Street and the EDA industry, to "What is the next EDA Driver" to "Tools or Users: Which is the Bigger Bottleneck?" The technical program also features 15 invited presentations by experts in their field, covering exciting topics such as "How do You Design a 10M Gate ASIC" to EDA tools for opto-electronics.

More than 225 companies are exhibiting the latest commercially available products Monday through Wednesday. Demo suites provide an opportunity to more closely examine the offerings of particular vendors. For the first time this year, we are featuring "Hands-on" Tutorials, Monday through Thursday, where vendors will have the opportunity to instruct small groups in the capabilities and use of their tools. The theme for these tutorials this year is "Verification of Embedded Systems".

On Monday, prior to the technical program, we are featuring a tutorial for EDA professionals wanting to learn more about the world of embedded system software. Also on Monday, there is an opportunity for non-technical attendees (teachers, financial community, spouses, etc.) to get a basic introduction to the world of EDA. On Friday, the conference concludes as usual, with five full-day specialized tutorials.

We invite you to join us in New Orleans and take full advantage of this rich and varied program.

Important Information At-A-Glance

	Exhibit Hours:	Demo Suite Hours:
Monday, June 10	10:00 AM to 6:00 PM	8:00 AM to 9:00 PM
Tuesday, June 11	10:00 AM to 6:00 PM	8:00 AM to 9:00 PM
Wednesday, June 12	10:00 AM to 6:00 PM	8:00 AM to 9:00 PM
Thursday, June 13	-	8:00 AM to 5:00 PM

At-Conference Registration Hours

The registration desk will be located in the lobby of Halls H & I of the Ernest N. Morial Convention Center and will be open at the following times:

Sunday, June 9, 2002	12:00 PM to 4:00 PM
Monday, June 10, 2002	8:00 AM to 6:00 PM
Tuesday, June 11, 2002	7:30 AM to 5:00 PM
Wednesday, June 12, 2002	7:30 AM to 5:00 PM
Thursday, June 13, 2002	7:30 AM to 3:00 PM
Tutorial Registration	Friday, June 14, 8:00 AM to 1:00 PM

Virtual DAC (www.dac.com)

Virtual DAC offers two powerful on-line tools for attendees to make the most of their time at DAC. The *DAC Floor* is designed to allow attendees to plan which exhibitors they want to visit. The *DAC Planner* is designed for attendees to plan which technical sessions and other important DAC events they want to attend. Together, the two services allow attendees to organize, in advance, how they want to utilize their time at DAC.

DACnet-2002

DACnet stations are located outside Hall H on the first level and outside the Auditorium on the second level of the Ernest N. Morial Convention Center. Wireless access is also available on the second level.

The 39th Design Automation Conference Week in Review					
Sunday, June 9	**Monday, June 10**	**Tuesday, June 11**	**Wednesday, June 12**	**Thursday, June 13**	**Friday, June 14**
• Verification Workshop	• Full Day Tutorial • Hands-On Tutorials • Workshops • Exhibits • Demo Suites	• Keynote Address • Opening Session • Technical Sessions • Hands-On Tutorial • Exhibits • Demo Suites	• Technical Sessions • Hands-On Tutorials • Exhibits • Demo Suites • DAC Party	• Keynote Address • Technical Sessions • Hands-On Tutorials • Demo Suites	• Full Day Tutorials

New @ DAC

DAC Pavilion

DAC brings its technical program to the exhibit floor through live panel discussions and broadcasts of highlighted technical sessions in the DAC Pavilion. DAC attendees and exhibitors are invited to visit the DAC Pavilion to participate in these engaging technical presentations or take a few minutes to relax in our lounge space.

A Whole NEW Monday at DAC

Monday at DAC has a whole new look this year. Exhibitor Presentations can now be found on each exhibitor's virtual DAC booth at www.dac.com. This has opened up Monday for workshops on Interoperability, Women in DA and an introductory session on EDA for non-engineers. If tutorials are more your flavor, check out the two Hands-On Tutorials, or the Full-Day Tutorial featuring issues with embedded systems for EDA developers. In addition, the free Monday exhibit passes are still available. Monday at DAC is not to be missed!

Tutorials

DAC offers several new tutorial programs this year. Starting on Monday, June 10, there is a full-day introductory tutorial on *An Introduction to Embedded Software: Issues, Tools and Methods - For HW and EDA Designers*. This tutorial is designed to prepare attendees for the many embedded systems technical sessions offered in the technical program. The other new tutorial program at DAC this year is the Hands-on Tutorials.

Workshops

Be sure to check out DAC's workshops, Sunday and Monday. (See pages 42 - 45.)

Hands-On Tutorials

Hands-on Tutorials are half-day sessions offered by exhibitors demonstrating solutions to verifying embedded systems. These highly interactive sessions give attendees the opportunity to do in-depth software demonstrations on Sun workstations.

Monday 9:00 AM - 12:00 PM, rm-293

Developing Bus-Functional Models for Embedded ATM Switch Verification • SynaptiCAD Inc., Synopsys, Inc.

Monday 2:00 PM - 5:00 PM, rm-293

Creating and Using a Virtual Prototype for Embedded System Verification • Mentor Graphics Corp., Denali Software, Inc., AXYS Design Automation, Inc., Verisity Design, Inc.

Tuesday 2:00 PM - 5:00 PM, rm-293

Assertion-Based Validation with HW/SW for Comprehensive Embedded System Verification

• Co-Design Automation, Inc., Real Intent, ARM

Wednesday 9:00 AM - 12:00 PM, rm-293

Hardware-Software Integration on the ARM Wireless PrimeXsys Platform using the CoWare N2C Design System • CoWare, Inc., ARM

Wednesday 2:00 PM - 5:00 PM, rm-293

Verification of Embedded Communication Systems

• Cadence Design Systems, Inc., Xilinx, Inc., Synplicity, Inc.

Thursday 9:00 AM - 12:00 PM, rm-294

Hardware and Software Debug Methods for a Programmable System • Xilinx, Inc., Wind River

Thursday 2:00 PM - 5:00 PM, rm-293

Top-Level Validation of Complex SoCs • Esterel Technologies

Program Highlights

Technical Program - details on pgs. 10 - 35

The technical program offers over 160 papers, panels and special sessions in five parallel tracks covering system level design, synthesis, physical design, verification, interconnect, power and AMS issues. Highlights include a focus on embedded systems (see right) as well as a number of special sessions with invited paper presentations on the implications of optics for EDA, the future of CMOS scaling, and designing 10M Gate ASICs.

TUESDAY KEYNOTE
Hajime Sasaki
Chairman of the Board
NEC Corp., Tokyo, Japan
Tuesday, June 11 - 9:00 AM
Room: Conference Auditorium

THURSDAY KEYNOTE
Jerry Fiddler
Chairman and Founder
Wind River, Alameda, CA
Thursday, June 13 - 1:00 PM
Room: Auditorium B

Best Paper Awards - details on pg. 53

Best Paper Awards of $1000 each will be announced at the Tuesday morning General Session. Papers eligible for awards in this category are nominated by the Program Committee and selected by a referee process. **(see sessions: 3.1, 4.3 and 29.2)**

On-Site Information Desk

The information desk is located in the lobby of Hall I of the Ernest N. Morial Convention Center. (504) 670-4500.

Embedded Systems -

Sessions: 3, 15, 19, 20, 23, 31, 34, 40, 41, 45, 49, 54

Recognizing the increasing role of embedded software and IP in complex SoC designs, we have provided a special focus on embedded systems topics. Over 35 papers and panels will cover topics such as embedded compilation, hardware/software co-design, system modeling and power optimization. In addition, special invited sessions will discuss design automation for electronic textiles, designing SoCs for yield improvement, and energy efficiency in mobile computing.

5th SIGDA Ph.D Forum - details on pg. 50

Tuesday, June 11 6:00PM - 8:30PM: Room 284

A chance for Ph.D students and industry representatives to get together. Students get feedback on their research proposals; industry gets a chance to meet students and preview their work.

Tutorials - details on pgs. 36 - 41

Monday, June 10, 2002 • 9:00 AM - 5:00 PM

1) An Introduction to Embedded Software: Issues, Tools and Methods - for HW and EDA Designers

Friday, June 14, 2002 • 9:00 AM - 5:00 PM

2) Intellectual Property Design and Integration for SoCs
3) Modeling Technology for High Frequency Design
4) Using SystemC for System Level Modeling and Design
5) Physical Chip Implementation: Hot Spots and Best Practices
6) New Computing Platforms for Embedded Systems

Exhibit Highlights

Exhibit Floor

Monday - Wednesday, June 10-12, 2002 10:00 AM - 6:00 PM

Over 225 EDA, Silicon, IP and Embedded Systems companies participate in the DAC exhibition and demo suites. All exhibits and suites are located in Halls F-J of the Ernest N. Morial Convention Center. **Children under the age of 14 will NOT be allowed in the exhibit hall or demo suite area.**

The Embedded Systems Showcase offers exhibitors and attendees a highly focused area to display and view tools for the design of embedded systems-on-chip.

The latest innovations are at your fingertips with exhibitors highlighting their latest products.

Demo Suites

Monday - Wednesday, June 10-12, 2002 .....8:00 AM - 9:00 PM
Thursday, June 13, 2002 .....8:00 AM - 5:00 PM

- Demo Suites are located in Halls F & G of the Ernest N. Morial Convention Center.
- Exhibiting companies offer their customers private product demos within the Convention Center.
- Demo Suites are available by invitation only.

Exhibit-Only Registration

- **Free Monday Exhibit-Only Passes** - Attend the exhibition free of charge Monday, June 10.
- $40 exhibit-only registration will allow you to attend exhibits Monday through Wednesday.

DAC Pavilion

DAC is introducing the DAC Pavilion in booth 1035. The Pavilion offers live panel discussions with industry experts, broadcasts of selected technical sessions and a lounge area to relax. Join us as we bring DAC's world-class technical program to the exhibit floor! Please check the DAC web site for details on the Pavilion presentations.

New Exhibitors at DAC

DAC has always been the best place to see the industry's newest companies, and this year is no exception. With over 30 new exhibitors this year, DAC is the place to be to find out what the hot start-ups are up to. Among the companies participating in DAC for the first time are: (as of May 13, 2002)

AccelChip, Inc.
Acreo
Annapolis Micro Systems, Inc.
Apex Design Systems, Inc.
Astek Corp.
Cimmetry Systems, Inc.
Dataram Corp.
DATE 03
eInfochips Inc.
Emulation and Verification Engineering
EverCAD Navigator Corp.
Freehand DSP
Golden Gate Technology
HPL
IEEE Media
Korea Electronics Technology Institute
LISATek, Inc.
MathWorks (The)
Multigig Ltd.
Nature Worldwide Technology Corp.
NEWS Design System
Novilit, Inc.
Open Core Protocol International Partnership
Prosilog SA
PTC
Q Design Automation
Sandwork Design Inc.
Sarnoff Corp.
Signal Integrity Software
Silicon Canvas, Inc.
StarNet Communications
Tempus Fugit, Inc.
UbiTech, Inc.
UP Media, Inc.
Zambeel, Inc.
Zenasis Technologies, Inc.

Tuesday Keynote - Paradigm Shift in Semiconductor Design: Challenges on the CAD System

Hajime Sasaki
Chairman of the Board
NEC Corp., Tokyo, Japan
Tuesday, June 11, 2002, 9:00 AM - 10:00 AM
Room: Conference Auditorium

Abstract: Last year, the Semiconductor industry suffered the severest recession in its history, withering by 32%. There had been no case where the final market of electronic products itself shrank. Concurrently, there have been some symbolic events in the industry. First, Moore's Law has become uncertain. In order to maintain the law, we must come up with novel processes for each new generation. Secondly, vendors have begun to shift from mass-production oriented business schemes to the system LSI business. This shift to application specific devices requires a drastic review of the value chain.

Semiconductor design in the new era can be divided into three areas. Area 1 deals with the traditional design hierarchy, such as function design, logic design and layout design. In this area, a revolution in function design is especially required that is represented by C language-based design. Area 2 deals with the new challenges of pursuing shrinking technology. We should be prepared for problems resulting from the application of new materials, represented by electric current leakage through the gate insulator. Also, interconnect structure is another challenging problem. The merger of design and process is the key. Area 3 deals with comprehensive issues such as IP management and mass production know-how.

The industry will become much more dependent on design. The challenge is how we should cultivate competitive designers both in quantity and quality. The "design project leader" must cover all three areas above. The corporate structure of IDM does not carry a competitive advantage, as long as design and process is divided into further sub-segments. When the industry can provide a solution that best meets its customer's needs and niceties from every angle, the industry will take off again and reach a new prosperous stage.

Biography: After receiving a master's degree of engineering in the field of electrical engineering from the graduate school of the University of Tokyo in 1961, he joined NEC Corporation. He served as General Manager of the VLSI Development Division and General Manager of the Microcomputer Products Division before being elected to the Board of Directors in 1988. He was appointed Senior Executive Vice President in 1996 in charge of semiconductors operations, and in 1999 elected to his current position of Chairman of the Board. Mr. Sasaki received the commendation from the Minister of State for Science and Technology, as a person of scientific and technological merits in 1995. In 2000, he received the Third Millennium Medal from IEEE. Also he was elected as a member of NAE (National Academy of Engineering). In 2001, he received the Robert N. Noyce Medal from IEEE and was elected as an IEEE Life Fellow.

Thursday Keynote - Software and Silicon - Where's the Equilibrium?

Jerry Fiddler
Chairman and Founder
Wind River, Alameda, CA
Thursday, June 13, 2002, 1:00 PM - 1:45 PM
Room: Auditorium B

Abstract: Silicon, EDA, and embedded software companies have largely lived in different universes. Despite repeated predictions that they would move closer together, and some real attempts to do so, those predictions have mostly proved false. Now, however, technology and economic trends are making it necessary and inevitable that suppliers find new ways to solve our customers problems. The complexity of the devices being built require solutions that cross the comfortable boundaries of the past. This talk will examine the trends and problems driving this.

Biography: Fiddler co-founded Wind River in 1981 with David Wilner, a colleague from Fiddler´s tenure at the University of California's Lawrence Berkeley Laboratory. Since establishing Wind River, Fiddler has taken on whatever role was necessary, from chief and only programmer to president and chairman of the board. Today Wind River, with operations worldwide, is the market share leader in embedded technology and continues to innovate and define the market.

Beginning with his tenure at the University of California's Lawrence Berkeley Laboratory, Fiddler has earned a reputation as an expert in the design and implementation of real-time systems. His work at Berkeley Lab gave him the ability to approach problems from a broader perspective and also taught him how to determine the pieces needed to build a system to solve a problem, skills that are key in developing embedded technology. He has published and presented numerous papers and articles on embedded technology and the rise of hidden, or embedded, computers in everyday life.

Fiddler graduated from the University of Illinois with a double baccalaureate in music and photography, and he received an M.S. in computer science from the same institution. Fiddler continues to follow his love of music with a home music studio and his band, XAZ, for which he writes songs and plays acoustic, electric, and classical guitars, as well as guitar synthesizer.

DAC Pavilion - Exhibit Floor Booth # 1035

Monday, 11:00AM-12:00PM

Knowing Your Exit Strategy: Acquisition vs. IPO

Organizers: **Michelle Clancy**, *Cayenne Communication*
Deirdre Hanford, *Synopsys, Inc.*
Moderator: **Erach Desai**, *Principal, Desaisive Technology Research*
Panelists:
Penny Herscher, *Simplex Solutions, Inc.*
Mike Tsai, *Axis Systems, Inc.*

Is an IPO a myth for most startups? How does a company position itself for acquisition or IPO? This panel will explore the strategies behind an emerging technology company's battles to position itself on the way to a successful IPO. Panelists will discuss what drives a company's direction toward an IPO or an acquisition. Questions will be discussed regarding different approaches used when structuring a company for a particular exit strategy.

Monday, 1:00PM-2:00PM

Panel 6 TBA

Check DACNet or the DAC Pavilion booth for details.

Monday, 3:00PM-4:00PM

Software Patents In EDA: Helping Progress or Impeding Innovation?

Organizer: **Dennis Fernandez**, *Fernandez and Associates, LLP*
Moderator: **Andrew Beckerman-Rodau**, *Suffolk Law School*
Panelists:
Dennis Fernandez, *Fernandez and Associates, LLP*
Joe Hustein, *InSilicon*

As the EDA industry continues to grow and mature, there is an ongoing debate on the constructive or obstructive role of Intellectual Property Rights. In support of the commercially valuable and strategic role of offensive blocking patents, Dennis Fernandez argues the legal case for aggressive exploitation of exclusive software patents against competitors, and even against possible Industry Standards. On the other hand, advocating company interests in building win-win customer relationships to deliver valuable goods and services, Joe Hustein, presents the business case for more effective cross-licensing and partnering efforts to foster new product concepts and processes.

Tuesday, 1:30PM-2:00PM

Focus Centers: Your Tax Dollars at Work

Organizer: **William H. Joyner**, *Semiconductor Research Corp.*
Moderator: **William H. Joyner**, *Semiconductor Research Corp.*
Panelists:
Jan Rabaey, *UC Berkeley, Gigascale Silicon Research Ctr.*
Rob Rutenbar, *CMU, Center for Circuits, Systems, and Software.*

Two Focus Center Research Programs, directly affect the EDA industry and the design automation research agenda: the Gigascale Silicon Research Center and the Center for Circuits, Systems, and Software. What are the US taxpayers and industry sponsors getting for this investment in research? Are they addressing areas where "evolutionary research and development have failed to find solutions to anticipated problems"? Are they generating "new concepts and radical alternatives to current methodologies"? How will these advances be translated into industry growth? Attend this panel to see how your tax dollars are hard at work.

DAC Pavilion - Exhibit Floor Booth # 1035

Tuesday, 4:00PM-5:00PM

Hybrid FPGAs: FPGA within ASIC or ASIC within FPGA

Organizer: Herman Schmit - *Carnegie Mellon Univ.*

Moderator: Herman Schmit, *Carnegie Mellon Univ.*

Panelists:
Chris Phillips, *Leopard Logic*
Sinan Kaptanoglu, *Altera*

The newest FPGAs from major vendors all include some "hard" components, such as microprocessor cores or fast multipliers. Simultaneously, a number of companies are creating embedded FPGA-like cores that can be incorporated into an ASIC design. Which is the right solution for next generation systems? Can you really get ASIC-level performance using these hard components within an FPGA, and can you really get FPGA-like flexibility and reprogrammability from an embedded FPGA? This panel will contrast these two alternatives for system implementation.

Wednesday, 1:30PM-2:00PM

Can IP Build Successful Semiconductor Businesses?

Organizer: Brandie Still, *Synchronicity, Inc.*

Moderator: Dennis Harmon, *Synchronicity, Inc.*

Panelists:
Alistair Greenhill, *ARM*
Colin Harris, *PMC-Sierra Inc.*

Much has been written about, and indeed invested in, emerging semiconductor Intellectual Property (IP) business models. Gartner estimates that the market will quadruple by 2004 and that over 150 firms have entered this space. Companies like ARM, MIPS and Rambus have garnered the spotlight for this recent phenomenon in the IC design chain, yet the reality is that few companies have been able to turn IP into viable, ongoing businesses - why is that? This panel will explore how various IP participants can facilitate implementation and overcome market obstacles.

Monday	Tuesday	Wednesday	
			10:00 –
Panel 1: Knowing Your Exit Strategy: Acquisition vs. IPO	Session 1: How Wall St. Evaluates EDA	Session 16: Optics: Lighting the Way to EDA Riches	11:00 –
			12:00 –
	Tape Delayed: Broadcast of Keynote		
Panel 6: TBA Check DACNet for updates.			1:00 –
	Panel 3: Focus Centers	Panel 5: Can IP Build Semiconductor	
Panel 2: Software Patents in EDA: Helping Progress or Impeding Innovation?	Session 6: Tools or Users: Which is the Bigger Bottleneck?	Session 26: How Do You Design a 10M Gate ASIC	2:00 – 3:00 –
	Panel 4: Hybrid FPGAs: FPGA within ASICs or ASICs within FPGAs		4:00 – 5:00

Monday, June 10, 2002

	Room 294	Room 293	Room 285	Room 286	Room 288
9:00	**Tutorial 1**	**Hands-On Tutorial**			
10:00	An Introduction to Embedded Software: Issues, Tools and Methods - for HW and EDA Designers	Developing Bus-Functional Models for Embedded ATM Switch Verification • *SynaptiCAD Inc., Synopsys, Inc.*			Introduction to Chips and EDA for a General Audience 10:00 AM - 12:00 PM
12:00					
1:00	Lunch in Room 296		Interoperability Workshop 12:00 PM - 5:00 PM		
2:00	**Tutorial 1 (cont.)** An Introduction to Embedded Software: Issues, Tools and Methods - for HW and EDA Designers	**Hands-On Tutorial** Creating and Using a Virtual Prototype for Embedded System Verification • *Mentor Graphics Corp., Denali Software, Inc., AXYS Design Automation, Inc., Verisity Design, Inc.*		Workshop for Women in Design Automation: Silk Purses and Sow's Ears: Turning Obstacles into Opportunity 1:15 PM - 4:00 PM	
5:00					

Exhibit Hours 10:00 AM - 6:00 PM / **Demo Suite Hours** 8:00 AM - 9:00 PM

Hands-On Tutorials (Rooms 293 & 294)

	Monday	Tuesday	Wednesday	Thursday
9:00 - 12:00	*Developing Bus-Functional Models for Embedded ATM Switch Verification* • SynaptiCAD Inc., Synopsys, Inc.		*Hardware-Software Integration on the ARM Wireless PrimeXsys Platform using the CoWare N2C Design System* • CoWare, Inc., ARM	*Hardware and Software Debug Methods for a Programmable System* • Xilinx, Inc., Wind River
2:00 - 5:00	*Creating and Using a Virtual Prototype for Embedded System Verification* • Mentor Graphics Corp., Denali Software, Inc., AXYS Design Automation, Inc., Verisity Design, Inc.	*Assertion-Based Validation with HW/SW for Comprehensive Embedded System Verification* • Co-Design Automation, Inc., Real Intent, ARM	*Verification of Embedded Communication Systems* • Cadence Design Systems, Inc., Xilinx, Inc., Synplicity, Inc.	*Top-Level Validation of Complex SoCs* • Esterel Technologies

Tuesday, June 11, 2002

8:30 to 10:00 — **Opening Session and Keynote Speaker** Location: Conference Auditorium

Paradigm Shift in Semiconductor Design: Challenges on the CAD System

Hajime Sasaki - Chairman of the Board, NEC Corp., Tokyo, Japan

BREAK 10:00 - 10:30

	Auditorium B	Room 292	Room 288	Room 287	Room 285
	Session 1 📽	**Session 2**	**Session 3**	**Session 4**	**Session 5**
10:30 to 12:00	**PANEL:** Wall Street Evaluates EDA	Web and IP Based Design	Design Innovations for Embedded Processors	Passive Model Order Reduction	New Perspectives in Physical Design
	LUNCH 12:00 - 2:00				
	Auditorium B			Room 287	
	Session 6 📽			**Session 10**	
2:00 to 4:00	**PANEL:** Tools or Users: Which is the Bigger Bottleneck?	**SPECIAL SESSION:** Life After CMOS: Imminent or Irrelevant?	Formal Verification	High Level Specification and Design	Timing Abstraction
	BREAK 4:00 - 4:30				
	Session 11 📽	**Session 12**	**Session 13**	**Session 14**	**Session 15**
4:30 to 6:00	**SPECIAL SESSION:** E-Textiles	**PANEL:** Analog Intellectual Property: Now? Or Never?	Low-Power System Design	Fabric-Driven Logic Synthesis	Memory Management and Address Optimization in Embedded Systems

use other file- p11-12 foldout

5th SIGDA Ph.D Forum in Room 285 of the Convention Center 6:00 PM - 8:30 PM

Exhibit Hours 10:00 AM - 6:00 PM / **Demo Suite Hours** 8:00 AM - 9:00 PM

📽 - **Videoed Sessions**

All Design Methods Sessions are shaded purple. Embedded Systems Sessions are shaded grey.
Presenters will be available in room 283 for additional 20-minute question and answer periods after the session.

Wednesday, June 12, 2002

	Auditorium B	Auditorium A	Room 292	Room 288	Room 287
	Session 16 📽	**Session 17**	**Session 18**	**Session 19**	**Session 20**
8:30 to 10:00	**SPECIAL SESSION:** Optics: Lighting the Way to EDA Riches?	**PANEL:** Nanometer Design: What Hurts Next?	Novel DFT, BIST and Diagnosis Techniques	Case Studies In Embedded System Design	Theoretical Foundations of Embedded System Design
	BREAK 10:00 - 10:30				
	Session 21 📽	**Session 22**	**Session 23**	**Session 24**	**Session 25**
10:30 to 12:00	Equivalence Verification	**PANEL:** Whither (or Wither) ASIC Handoff?	Embedded Software Automation: From Specification to Binary	Applications of Reconfigurable Computing	New Test Methods Targeting Non-Classical Faults
	Session 26 📽				**Session 30**
2:00 to 4:00	**SPECIAL SESSION:** How Do You Design a 10M Gate ASIC?	Power Distribution Issues	Advances In Synthesis	Analog Synthesis & Design Methodology	Low-Power Physical Design
	BREAK 4:00 - 4:30				
	Session 31 📽	**Session 32**	**Session 33**	**Session 34**	**Session 35**
4:30 to 6:00	**PANEL:** Unified Tools for SoC Embedded Systems: Mission Critical, Mission Impossible or Mission Irrelevant?	Multi-Voltage, Multi-Threshold Design	Advanced Simulation Techniques	Design Methodologies Meet Network Applications	Advances in Analog Modeling

use other file- p11-12 foldout

39th DAC Wednesday Night Carnival Krewe Party • 7:30 PM - 10:30 PM • Hilton New Orleans Riverside

AM - 9:00 PM

Exhibit Hours 10:00 AM - 6:00 PM / **Demo Suite Hours** 8:00 AM - 9:00 PM

📽 - **Videoed Sessions**

All Design Methods Sessions are shaded purple. Embedded Systems Sessions are shaded grey.

Presenters will be available in room 283 for additional 20-minute question and answer periods after the session.

CUT OFF
CUT OFF
CUT OFF
CUT OFF
CUT OFF
CUT OFF
CUT OFF
CUT OFF

CUT OFF
CUT OFF
CUT OFF
CUT OFF
CUT OFF
CUT OFF
CUT OFF
CUT OFF

Thursday, June 13, 2002

	Auditorium B	Auditorium A	Room 292	Room 288	Room 287
	Session 36	**Session 37**	**Session 38**	**Session 39**	**Session 40**
8:30 to 10:00	Advances in Timing and Simulation	**PANEL:** Formal Verification Methods: Getting Around the Brick Wall	Routing and Buffering	System on Chip Design	Timing Analysis and Memory Optimization for Embedded Systems
	BREAK 10:00 - 10:30				
	Session 41	**Session 42**	**Session 43**	**Session 44**	**Session 45**
10:30 to 12:00	Processors and Accelerators For Embedded Applications	**PANEL:** What is the Next EDA Driver?	Cross-Talk Noise Analysis and Management	Test Cost Reduction for SoCs	Scheduling Techniques for Embedded Systems
	Keynote - *Software and Silicon - Where's the Equilibrium?* • 1:00 - 1:45 • Room: Auditorium B ***Jerry Fiddler*** - Chairman and Founder, Wind River				
	Session 46	**Session 47**	**Session 48**	**Session 49**	**Session 50**
2:00 to 4:00	**SPECIAL SESSION:** Designing SoCs for Yield Improvement	Advances in SAT	Inductance and	Development of Processors	Moving Towards More ective Validation
			BREAK 4:00 - 4:30		
	Session 51	**Session 52**	**Session 53**	**Session 54**	**Session 55**
4:30 to 6:00	**SPECIAL SESSION:** Energy Efficient Mobile Computing	Floorplanning and Placement	Circuit Effects in Static Timing	Design Space Exploration for Embedded Systems	Behavioral Synthesis

use other file- p11-12 foldout

Demo Suite Hours 8:00 AM - 5:00 PM

Ukleoed Sessions

All Design Methods Sessions are shaded purple. Embedded Systems Sessions are shaded grey.
Presenters will be available in room 283 for additional 20-minute question and answer periods after the session.

Friday, June 14, 2002

Tutorials are held at the Ernest N. Morial Convention Center.

8:00 AM - 1:00 PM .....Tutorial Registration Open
9:00 AM - 5:00 PM .....Tutorials
8:00 AM .....Continental Breakfast
12:00 Noon.....Lunch (in room 393)

Tutorial 2 – Intellectual Property Design and Integration for SoCs rm-291

Organizers: Ralf Seepold - *FZI, Karlsruhe, Germany*
Natividad Martínez Madrid - *FZI, Karlsruhe, Germany*

Tutorial 3 – Modeling Technology for High Frequency Design rm-293

Organizer: Joel R. Phillips - *Cadence Berkeley Labs., San Jose, CA*

Tutorial 4 – Using SystemC for System Level Modeling and Design rm-294

Organizers: Kevin Kranen - *Synopsys, Inc., Mountain View, CA*
Mike [illegible]

Tutorial 5 – [illegible]

Organizer: Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*

Tutorial 6 – New Computing Platforms for Embedded Systems rm-296

Organizers: Frank Vahid - *Univ. of California, Riverside & Center for Embedded Computer Systems, UC Irvine, Irvine, CA*
Walid Najjar - *Univ. of California, Riverside, CA*

use other file- p11-12 foldout

Topics and Related Sessions

If you are interested in the following topics, please see the related sessions below.

Embedded Systems:
Sessions: 3, 15, 19, 20, 23, 40, 41, 45, 49, 54

Logic & High Level Synthesis & Optimization:
Sessions: 9, 14, 28, 55

Logic & Functional Verification & Simulation:
Sessions: 8, 21, 33, 37, 47, 50

Timing Verification and Simulation:
Sessions: 10, 36, 53

Electrical, Device & Interconnect Modeling & Simulation:
Sessions: 4, 33, 43, 48

Physical Design:
Sessions: 5, 27, 38, 52

[illegible]
46

[illegible]nology:
7

Analog and Mixed Signal Design:
Sessions: 12, 29, 35

Low Power Design:
Sessions: 13, 30, 32, 51

Design Re-use, IP and SoC Issues:
Sessions: 2, 24, 31, 39

EDA Methodologies and Industry Issues:
Sessions: 6, 22, 26, 34, 42

Opening Session

rm: Conference Auditorium

Opening Remarks: Bryan Ackland - *General Chair, 39th DAC*

Awards Presented By: Robert Walker
ACM/SIGDA Representative

Giovanni De Micheli
IEEE/CASS Representative

Opening Keynote Address:

Paradigm Shift in Semiconductor Design: Challenges on the CAD System

Hajime Sasaki - *Chairman of the Board, NEC Corp., Tokyo, Japan*

Awards/Scholarships

- P.O. Pistilli Undergraduate Scholarships (ACSEE)
- Marie R. Pistilli Women in EDA Achievement Award
- Graduate Scholarships
- Student Design Contest Awards
- 2002 IEEE CASS Fellows
- ACM/SIGDA Distinguished Service Award
- ACM/SIGDA Outstanding New Faculty Award
- Phil Kaufman Award
- Best Paper Awards

Tuesday
June 11

8:30
to
10:00

Tuesday June 11

10:30 to 12:00

All speakers are denoted in bold

S – denotes short paper

§ – denotes best paper

Session 1 – Videoed

rm: Auditorium B

PANEL: WALL STREET EVALUATES EDA

CHAIR: Aart de Geus - *Synopsys, Inc., Mountain View, CA*
ORGANIZERS: Sharon Turnoy, Deirdre Hanford

The EDA sector is capturing unprecedented attention on Wall Street. With seven IPOs in 2001 alone and strong performance by the EDA "blue chips," the industry has gained new prominence with the capital markets. In this panel, Aart de Geus will moderate a discussion between representatives of the various constituencies who play a role in shaping Wall Street's opinion of EDA: financial analysts, portfolio managers, venture capitalists, CEOs, and the press.

Questions discussed will include: How do investors and analysts currently view EDA? What contributes to that perception? What factors drive EDA's current favor with Wall Street, and why is the sector "hot" compared to two to three years ago? How do we sustain that favor? Given the highly complex nature of our industry, how do investors decipher the strength of a particular EDA firm? Is EDA tied to the semiconductor industry's performance? What role does the press play in shaping the view?

1.1 Wall Street Evaluates EDA

Moshe Gavrielov - *Verisity Design, Inc., Mountain View, CA*
Richard Goering - *EE Times, Felton, CA*
Lucio Lanza- *Lanza TechVentures, Palo Alto, CA*
Vishal Saluja - *J. & W. Seligman & Co., Inc., Palo Alto, CA*
Jay Vleeschhouwer - *Merrill Lynch & Co. Inc., New York, NY*

Session 2

rm: 292

WEB AND IP BASED DESIGN

CHAIR: Gang Qu - *Univ. of Maryland, College Park, MD*
ORGANIZERS: Ahmed A. Jerraya, Krzysztof Kuchcinski

Web created new opportunities for geographically distributed design process but at the same time it introduced a number of challenges. The first paper presents techniques for IP delivery using Java applets. The second paper proposes generic techniques for watermarking-based IP protection that is essentially applicable to an arbitrary optimization and design problem. The third paper enables simulation of a design in the web environment. The final paper makes design process more flexible by leveraging on engineering change methodology.

2.1 IP Delivery for FPGAs Using Applets and JHDL

Michael J. Wirthlin, Brian McMurtrey - *Brigham Young Univ., Provo, UT*

2.2 Watermarking Integer Linear Programming Solutions

Seapahn Megerian, Milenko Drinic, Miodrag Potkonjak - *Univ. of California, Los Angeles, CA*

2.3S Model Design using Hierarchical Web-Based Libraries

Fabrice Bernardi, Jean F. Santucci - *Univ. of Corsica, Corte, France*

2.4S Behavioral Synthesis via Engineering Change

Milenko Drinic - *Univ. of California, Los Angeles, CA*
Darko Kirovski - *Microsoft Research, Redmond, WA*

Design Methods Sessions are shaded purple. Embedded Systems Sessions are shaded grey.

Session 3

rm: 288

DESIGN INNOVATIONS FOR EMBEDDED PROCESSORS

CHAIR: Vojin Zivojnovic - *AXYS Design Automation, Inc., Irvine, CA*

ORGANIZERS: Grant E. Martin, Majid Sarrafzadeh

This session presents a number of interesting innovations in design techniques for embedded processors. The first paper reveals a novel technique for mixing compiled-code and interpreted-code approaches to instruction-set simulation. The second paper introduces the idea of incorporating optimized hardware for profiling memory. The final paper reduces instruction memory size using decompression hardware.

§ 3.1 A Universal Technique for Fast and Flexible Instruction-Set Architecture Simulation

Achim Nohl - LISATek Inc., Menlo Park, CA
Gunnar Braun - *Aachen Univ. of Tech., Aachen, Germany*
Andreas Hoffmann - LISATek Inc., Menlo Park, CA
Oliver Schliebusch, Rainer Leupers, Heinrich Meyr - *Aachen Univ. of Tech., Aachen, Germany*

3.2 A Fast On-Chip Profiler Memory

Roman Lysecky, Susan Cotterell, Frank Vahid - *Univ. of California, Riverside, CA*

3.3 Design of a One-Cycle Decompression Hardware for Performance Increase in Embedded Systems

Haris Lekatsas, Joerg Henkel, Venkata Jakkula - *NEC Corp., Princeton, NJ*

Session 4

rm: 287

PASSIVE MODEL ORDER REDUCTION

CHAIR: Jacob White - *Massachusetts Institute of Tech., Cambridge, MA*

ORGANIZERS: Jaijeet Roychowdhury, Mustafa Celik

Three excellent papers are presented in this session, with the theme of rigorous approaches to linear passive MOR addressing important theoretical and practical issues. The first paper presents a framework for MOR based on generalized factors that includes popular methods like PRIMA as special cases. The second paper presents a convincing argument that causality is key to effective passive MOR of distributed systems. The final demonstrates that attentiveness to positive real properties ensures passivity in truncated balanced realizations.

4.1 A Factorization-Based Framework for Passivity-Preserving Model Reduction of RLC Systems

Qing Su, Venkataramanan Balakrishnan, Cheng-Kok Koh - *Purdue Univ., West Lafayette, IN*

4.2 Model Order Reduction for Strictly Passive and Causal Distributed Systems

Luca Daniel - *Univ. of California, Berkeley, CA*
Joel R. Phillips - *Cadence Design Systems, Inc., San Jose, CA*

§ 4.3 Guaranteed Passive Balancing Transformations for Model Order Reduction

Joel R. Phillips - *Cadence Berkeley Labs., San Jose, CA*
Luca Daniel - *Univ. of California, Berkeley, CA*
Miguel Silveira - *INESC, Lisboa, Portugal*

Session 5

rm: Auditorium A

NEW PERSPECTIVES IN PHYSICAL DESIGN

CHAIR: Steven Teig - *Simplex Solutions, Inc., Sunnyvale, CA*

ORGANIZERS: Ralph Otten, Timothy Kam

This session presents early, innovative examples of what promise to be some of the next trends in physical design.

5.1 Uncertainty-Aware Circuit Optimization

Xiaoliang Bai - *Univ. of California at San Diego, La Jolla, CA*
Chandu Visweswariah, Philip N. Strenski - *IBM Corp., Yorktown Heights, NY*
David J. Hathaway - *IBM Corp., Essex Junction, VT*

5.2 Congestion-Driven Codesign of Power and Signal Networks

Haihua Su, Jiang Hu - *IBM Corp., Austin, TX*
Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*
Sani R. Nassif - *IBM Corp., Austin, TX*

5.3 On Metrics for Comparing Routability Estimation Methods for FPGAs

Parivallal Kannan, Shankar Balachandaran, Dinesh Bhatia - *Univ. of Texas, Dallas, TX*

Tuesday June 11

2:00 to 4:00

All speakers are denoted in bold

S – denotes short paper

ß – denotes best paper

Session 6 – Videoed

rm: Auditorium B

PANEL: TOOLS OR USERS: WHICH IS THE BIGGER BOTTLENECK?

CHAIR: Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*

ORGANIZER: Bob Dahlberg

As chip design becomes ever more complex, fewer design teams are succeeding. Who's to blame? On one hand, tools are hard to use, buggy, not interoperable, and have missing functionality. On the other hand, there is a wide range of engineering skills, and tools can be abused within flawed methodologies. This panel will quantify and prioritize the key gaps that must be addressed on both sides.

6.1 Tools or Users: Which Is the Bigger Bottleneck?

Ron Collett - *Numetrics Management Systems, Inc., Santa Clara, CA*
Patrick Groeneveld, - *Magma Design Automation, Inc., Cupertino, CA*
Lavi Lev- *Cadence Design Systems, Inc., San Jose, CA*
Nancy Nettleton - *Sun Microsystems, Palo Alto, CA*
Paul Rodman - *ReShape, Inc., Mountain View, CA*
Lambert Van den Hoven - *Philips Research Labs., Eindhoven, The Netherlands*

Session 7

rm: Auditorium A

SPECIAL SESSION: LIFE AFTER CMOS: IMMINENT OR IRRELEVANT?

CHAIRS: Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*
Kaustav Banerjee - *Stanford Univ., Stanford, CA*

ORGANIZERS: Dennis Sylvester, Kaustav Banerjee

With the introduction of 90nm CMOS processes as early as the fourth quarter of this year, we are finally entering the heralded nanometer CMOS regime. In nanoscale CMOS, many fundamental questions now become more pressing: how far can we scale the traditional planar CMOS paradigm, what device technologies are in development that can potentially replace CMOS and when? This session addresses both evolutionary and revolutionary approaches to continuing along Moore's Law. We start with industrial perspectives on how to best extend the lifespan of CMOS as we know it with the latter half of the session devoted to more radical departures from today's devices.

7.1 Life Is CMOS: Why Chase the "Life-After"?

George Sery - *Intel Corp., Santa Clara, CA*
Shekhar Borkar, Vivek De - *Intel Corp., Hillsboro, OR*

7.2 The Next Chip Challenge: Effective Methods for Viable Mixed Technology SoCs

H. Bernhard Pogge - *IBM Microelectronics, Hopewell Junction, NY*

7.3 Few Electron Devices: Towards Hybrid CMOS-SET Integrated Circuits

Adrian Ionescu, Michel J. Derclercq, Santanu Mahapatra - *Swiss Federal Institute of Tech., Lausanne, Switzerland*
Kaustav Banerjee - *Stanford Univ., Stanford, CA*
Jacques Gautier - *CAE-DRT-LEVI/DTS, Grenoble, France*

7.4 Carbon Nanotube Field-Effect Transistors for Logic Applications

Richard Martel, V. Dercyke, J. Appenzeller, S. Wind, Ph. Avouris - *IBM Corp., Yorktown Heights, NY*

Design Methods Sessions are shaded purple. Embedded Systems Sessions are shaded grey.

Session 8

rm: 292

FORMAL VERIFICATION

CHAIR: Yaron Wolfsthal - *IBM Corp., Haifa, Israel*
ORGANIZERS: Carl Pixley, Karem Sakallah

The need and benefits of formal verification (FV) have been accepted for some time. The capacity of FV-based tools is still limited and in this session new technologies and methodologies are presented that enable larger designs to be formally verified. In particular, novel ideas to enhance symbolic simulation, hybrid approach that uses symbolic simulation and model checking and SAT and BDD bounded model-checking.

8.1 Efficient State Representation for Symbolic Simulation

Valeria Bertacco, Kunle Olukotun - *Stanford Univ., Stanford, CA*

8.2 Handling Special Constructs in Symbolic Simulation

Alfred Koelbl - *Tech. Univ. of Munich, Munich, Germany*
James Kukula - *Synopsys, Inc., Beaverton, OR*
Kurt Antreich - *Tech. Univ. of Munich, Munich, Germany*
Robert Damiano - *Synopsys, Inc., Beaverton, OR*

8.3 A Hybrid Verification Approach: Getting Deep into the Design

Scott Hazelhurst - *Univ. of the Witwatersrand, Johannesburg, S. Africa*
Osnat Weissberg, Gila Kamhi, Limor Fix - *Intel Corp., Haifa, Israel*

8.4 Can BDDs Compete with SAT Solvers on Bounded Model Checking?

Gianpiero Cabodi, Paolo E. Camurati, Stefano Quer - *Politecnico di Torino, Turin, Italy*

Session 9

rm: 288

HIGH LEVEL SPECIFICATION AND DESIGN

CHAIR: Andreas Kanstein - *Motorola, Inc., Austin, TX*
ORGANIZERS: Limor Fix, Shin-ichi Minato

With increasing design complexity, different technologies have been developed to bridge the gap between the amount of logic that can be put on a chip and the design and verification effort necessary to build such a chip. In this session, C-based design methodology is presented. High level specification is used for generation of IP monitors, for designing pipeline control and for constraining the design environment.

9.1 RTL C-Based Methodology for Designing and Verifying a Multi-Threaded Processor

Luc Semeria - *Synopsys, Inc., Mountain View, CA*
Andrew Seawright - *0-In Design Automation, San Jose, CA*
Renu Mehra- *Synopsys, Inc., Mountain View, CA*
Daniel Ng- *Broadcom, Inc., San Jose, CA*
Arjuna Ekanayake, Barry Pangrle - *Synopsys, Inc., Mountain View, CA*

9.2 High-Level Specification and Automatic Generation of IP Interface Monitors

Marcio T. Oliveira, Alan J. Hu - *Univ. of British Columbia, Vancouver, British Columbia*

9.3 Achieving Maximum Performance: A Method for the Verification of Interlocked Pipeline Control Logic

Kerstin I. Eder - *Univ. of Bristol, Bristol, Great Britain*
Geoff Barrett - *Broadcom Corp., Bristol, Great Britain*

9.4 Formal Verification of Module Interfaces Against Real Time Specifications

Arindam Chakrabarti - *Univ. of California, Berkeley, CA*
Pallab Dasgupta, Partha P. Chakrabarti, Ansuman Banerjee - *Indian Institute of Tech., Kharagpur, India*

Session 10

rm: 287

TIMING ABSTRACTION

CHAIR: Mark Hahn - *Cadence Design Systems, Inc., San Jose, CA*
ORGANIZERS: Chandu Visweswariah, Narendra V. Shenoy

Hierarchical timing verification and re-use of IP blocks require accurate timing abstraction. The first three papers of this session present various approaches to efficient generation of timing abstractions. The last paper applies ATPG and implication techniques to automatically detect multi-cycle paths in sequential circuits.

10.1 Automated Timing Model Generation

Ajay J. Daga, Loa Mize, Subramanyam Sripada, Chris Wolff, Qiuyang Wu - *Synopsys, Inc., Hillsboro, OR*

10.2 Timing Model Extraction of Hierarchical Blocks by Graph Reduction

Cho Moon - *Cadence Design Systems, Inc., San Diego, CA*
Harish Kriplani, Krishna P. Belkhale - *Cadence Design Systems, Inc., San Jose, CA*

10.3 Efficient Stimulus Independent Timing Abstraction Model Based on a New Concept of Circuit Block Transparency

Martin Foltin, Brian Foutz, Sean C. Tyler - *Hewlett-Packard Co., Fort Collins, CO*

10.4 An Implication-Based Method to Detect Multi-Cycle Paths in Large Sequential Circuits

Hiroyuki Higuchi - *Fujitsu Labs. Ltd., Kawasaki, Japan*

Tuesday June 11

4:30 to 6:00

All speakers are denoted in bold

S – denotes short paper

§ – denotes best paper

Session 11 📽 – Videoed

rm: Auditorium B

SPECIAL SESSION: E-TEXTILES

CHAIR: Majid Sarrafzadeh - *Univ. of California, Los Angeles, CA*
ORGANIZER: Majid Sarrafzadeh

Topics: Enabling technologies and fabrication techniques for the economical manufacture of large-area, flexible, conformable e-textiles applications. E-textiles represents a revolutionary step by bringing together textiles and electronics in a common effort to integrate many elementary sensors, actuators, logic, and power sources sparsely distributed application, with highly unreliable behavior, but with stringent constraints on operational longevity. On-the-fly reconfigurability and adaptability with low computational overhead. Device and technology challenges imposed by embedding simple computational elements into fabric, by building yarns with computational capabilities, or by the need of unconventional power sources.

11.1 Reconfiguarable Fabric

Deborah Estrin, Glenn Reinmann, Mani Srivatsava, Majid Sarrafzadeh - *Univ. of California, Los Angeles, CA*

11.2 The Wearable Motherboard: A Framework for Personalized Mobile Information Processing (PMIP)

Sungmee Park, **Sundaresan Jayaraman**, Ken Mackenzie - *Georgia Institute of Tech., Atlanta, GA*

11.3 Opportunities and Challenges in E-textile Modeling, Analysis and Optimization

Diana Marculescu, Radu Marculescu, Pradeep Khosla - *Carnegie Mellon Univ., Pittsburgh, PA*

Session 12

rm: Auditorium A

PANEL: ANALOG INTELLECTUAL PROPERTY: NOW? OR NEVER?

CHAIR: Stephen Ohr - *EET/CMP Media, San Francisco, CA*
ORGANIZERS: Linda Marchant, Philippe Magarshack

With more and more Systems-on-chip makers hoping to include analog functional blocks as a means of differentiating their designs, it is therefore tempting to believe that analog intellectual properties (IP) can be created, traded and integrated with the same tools and methodologies with which digital IP are moved about. But is analog IP a viable business? Can analog IPs be traded — given that design tuning is needed for every new chip variant, and every new process generation? Certainly, silicon foundries need to rely on a wide set of external IP offerings, in order to allow their users to build complete systems. Are they seeing enough activity in Analog IP designs to justify specialized fab runs, or the kind of process tuning that would allow analog and digital IPs to coexist on the same chip? What is the future of analog designs at the very low voltage-swings coming with sub-100nm CMOS? What CAD tools are needed to help analog designers? Are newly emerging EDA technologies, designed to enhance analog design productivity, maturing rapidly enough to be accepted by designers? Certainly many Analog IP providers and Analog EDA tool vendors would argue that the answer is yes. However, how many 'traditional' analog designers would admit they are still using kit parts and breadboards — maybe Spice and manual IC layout techniques — today in their every-day job? This panel of experts — representing analog designers, analog EDA tool providers, silicon foundries and analog IP vendors — will address these issues, and provide a likely context for analog IP development and trade.

12.1 Analog Intellectual Property: Now? or Never?

Mike Brunolli - *NurLogic Design, Inc., San Diego, CA*
Masao Hotta - *Hitachi Ltd., Gunma-ken, Japan*
Felicia James - *Cadence Design Systems, Inc., San Jose, CA*
Rudolf Koch - *Infineon Technologies AG, Munich, Germany*
Roy McGuffin - *Antrim Design Systems, Inc., Scotts Valley, CA*
Andrew Moore - *TSMC, San Jose, CA*

Session 13

rm: 292

LOW-POWER SYSTEM DESIGN

CHAIR: Giovanni De Micheli - *Stanford Univ., Stanford, CA*

ORGANIZERS: Renu Mehra, Enrico Macii

This session deals with system level power minimization using dynamic voltage scaling. The first paper describes task scheduling algorithms that minimize energy in a multiprocessor environment. The second paper describes task scheduling algorithms that maximize battery life. The third paper minimizes energy in a multiprocessor environment by allowing each loop nest to be executed with multiple process and shutting off unused processors.

13.1 Task Scheduling and Voltage Selection for Energy Minimization

Yumin Zhang - *Synopsys, Inc., Mountain View, CA*
Xiaobo (Sharon) Hu, Danny Z. Chen - *Univ. of Notre Dame, Notre Dame, IN*

13.2 Battery-Conscious Task Sequencing for Portable Devices Including Voltage/Clock Scaling

Daler Rakhmatov, Sarma Vrudhula - *Univ. of Arizona, Tucson, AZ*
Chaitali Chakrabarti - *Arizona State Univ., Tempe, AZ*

13.3 An Energy Saving Strategy Based on Adaptive Loop Parallelization

Ismail Kadayif, Mahmut T. Kandemir - *Penn State Univ., University Park, PA*
Mustafa Karakoy - *Imperial College, London, Great Britain*

Session 14

rm: 288

FABRIC-DRIVEN LOGIC SYNTHESIS

CHAIR: Tiziano Villa - *Parades, Roma, Italy*

ORGANIZERS: Malgorzata Marek-Sadowska, Steven Nowick

Papers in this section discuss synthesis approaches which target specific fabrics. The first paper proposes a new regular layout structure and discusses logic synthesis for it. The second paper describes a modified Bellman-Ford algorithm for cycle stealing in FPGAs. The third paper shows how layout information can improve carry-save adder designs.

14.1 River PLAs: A Regular Circuit Structure

Fan Mo, Robert K. Brayton - *Univ. of California, Berkeley, CA*

14.2 Withdrawn

14.3 Layout-Aware Synthesis of Arithmetic Circuits

Junhyung Um, Taewhan Kim - *KAIST, Taejon, Korea*

Session 15

rm: 287

MEMORY MANAGEMENT AND ADDRESS OPTIMIZATION IN EMBEDDED SYSTEMS

CHAIR: Nikil Dutt - *Univ. of California, Irvine, CA*

ORGANIZERS: Diederik Verkest, Luca Benini

Memory access and addressing is often a critical issue in embedded system design. The papers in this session describe approaches to reduce/eliminate memory bottlenecks.

15.1 Automatic Data Migration for Reducing Energy Consumption in Multi-Bank Memory Systems

Victor M. De La Luz, Mahmut T. Kandemir - *Penn State Univ., University Park, PA*
Ibrahim Kelev - *UMIST, Manchester, UK*

15.2 Exploiting Shared Scratch Pad Memory Space in Embedded Multiprocessor Systems

Mahmut T. Kandemir - *Penn State Univ., University Park, PA*
J. Ramanujam - *Louisiana State Univ., Baton Rouge, LA*
Alok Choudhary - *Northwestern Univ., Evanston, IL*

15.3 Address Assignment Combined with Scheduling in DSP Code Generation

Yoonseo Choi, Taewhan Kim - *KAIST, Taejon, Korea*

Wednesday June 12

8:30 to 10:00

All speakers are denoted in bold

S – denotes short paper

ß – denotes best paper

Session 16 – Videoed

rm: Auditorium B

SPECIAL SESSION: OPTICS: LIGHTING THE WAY TO EDA RICHES?

CHAIR: Jaijeet Roychowdhury - *Univ. of Minnesota, Minneapolis, MN*

ORGANIZERS: Jaijeet Roychowdhury, Joel R. Phillips

Optical communication has been a key enabler in the development of the Internet. Now it is being considered for on-chip signalling and communication as well. What implications does optics hold for the future of chip design and of EDA? Have EDA and optical CAD anything in common? Can they benefit each other? We look into these questions in this special session, consisting of two invited lectures and a contributed paper. The first talk is an overview of optical systems and their use in communications. The second focuses on computer-aided design techniques in optical communications. The final presentation describes a fast technique for computing optical fields propagating in free space.

16.1 The Optical Internet and the Drive Towards Multifunctional Hybrid Optoelectronic Integration

Edward H. Sargent - *Univ. of Toronto, Toronto, ON, Canada*

16.2 Computer Aided Design of Long-Haul Optical Fiber Transmission Systems

J. F. Maloney - *PhotonEx Corp., Maynard, MA*
C. R. Menyuk - *Univ. of Maryland, Baltimore, MD*

16.3 A Fast Optical Propagation Technique for Modeling Micro-Optical Systems

Timothy P. Kurzweg, Steven P. Levitan, Jose A. Martinez, Mark Kahrs, Donald M. Chiarulli - *Univ. of Pittsburgh, Pittsburgh, PA*

Session 17

rm: Auditorium A

PANEL: NANOMETER DESIGN: WHAT HURTS NEXT?

CHAIR: Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

ORGANIZERS: Rob A. Rutenbar, Andrew B. Kahng

Every year, the design and EDA communities are besieged by dire warnings about the impending doom of "design as we know it". Every year, another unpleasant physical effect from the evil depths of deep submicron physics surfaces, compromising our designs in new and vile ways. Every year, the same story: more nanometer woes. Rather than endorse a new winner in this year's race for the "next worst thing" from the nanometer arena, this panel gathers a set of world-class technology experts to debate what effects are hiding just around the next corner, waiting to pounce on the unwary tool or chip designer. Which among these is really the most important, when will it happen, and why?

17.1 Nanometer Design: What Hurts Next?

Bob Brodersen - *Univ. of California, Berkeley, CA*
Anthony Hill - *Texas Instruments, Inc., Dallas, TX*
John Kibarian - *PDF Solutions, San Jose, CA*
Desmond A. Kirkpatrick - *Intel Corp., Hillsboro, OR*
Mitsumasa Koyanagi - *Tohoku Univ., Sendai, Japan*
Mark Lavin - *IBM Corp., Yorktown Heights, NY*

Design Methods Sessions are shaded purple. Embedded Systems Sessions are shaded grey.

Session 18

rm: 292

NOVEL DFT, BIST AND DIAGNOSIS TECHNIQUES

CHAIR: Rathish Jayabharathi - *Intel Corp., Folsom, CA*

ORGANIZERS: Kwang-Ting (Tim) Cheng, T.M. Mak

This session presents several novel ideas on DFT, BIST and diagnosis. The first paper discusses a DFT technique that utilizes clock control to simplify ATPG. The second paper tackles diagnosis problems with the conventional MISR signatures. The third paper presents a DFT technique to accommodate unknown output values in a BIST scheme. The last paper explores the diagnosis capability of software-based self-test.

18.1 Low-Cost Sequential ATPG with Clock-Control DFT

Miron Abramovici - *Agere Systems, Inc., Murray Hill, NJ*
Xiaoming Yu, Liz Rudnick - *Univ. of Illinois, Urbana, IL*

18.2 Effective Diagnostics Through Interval Unloads In a BIST Environment

Peter Wohl - *Synopsys, Inc., Williston, VT*
Greg Maston, John Waicukauski, Sanjay Patel - *Synopsys, Inc., Beaverton, OR*

18.3S On Output Response Compression In the Presence of Unknown Output Values

Irith Pomeranz - *Purdue Univ., West Lafayette, IN*
Sandip Kundu - *Intel Corp., Austin, TX*
Sudhakar M. Reddy - *Univ. of Iowa, Iowa City, IA*

18.4S Software-Based Diagnosis for Processors

Li Chen, Sujit Dey - *Univ. of California at San Diego, La Jolla, CA*

Session 19

rm: 288

CASE STUDIES IN EMBEDDED SYSTEM DESIGN

CHAIR: Wayne Wolf - *Princeton Univ., Princeton, NJ*

ORGANIZERS: Anand Raghunathan, Xiaobo (Sharon) Hu

This session showcases case studies and experiences using application specific design methodologies in the design of embedded systems. The presentations include the design of a Viterbi decoder for wireless handsets, the use of a cost model for Hardware/Software co-design in the design of a digital camera, and the generation of efficient software for H.263 image compression.

19.1 Design of a High-Throughput Low-Power IS95 Viterbi Decoder

Xun Liu, Marios C. Papaefthymiou - *Univ. of Michigan, Ann Arbor, MI*

19.2 A Detailed Cost Model for Concurrent Use With Hardware/Software Co-Design

Daniel Ragan, Peter Sandborn - *Univ. of Maryland, College Park, MD*
Paul Stoaks - *Foresight-Systems, Inc., Austin, TX*

19.3 Efficient Code Synthesis from Extended Dataflow Graphs for Multimedia Applications

Hyunok Oh, Soonhoi Ha - *Seoul National Univ., Seoul, Korea*

Session 20

rm: 287

THEORETICAL FOUNDATIONS OF EMBEDDED SYSTEM DESIGN

CHAIR: Rajesh Gupta - *Univ. of California, Irvine, CA*

ORGANIZERS: Annette Reutter, Donatella Sciuto

This session presents three formal approaches dealing with performance analysis and refinement transformations in embedded systems design. The first paper introduces formal transformation methods for the refinement of an abstract model into an implementation model. The second paper presents a compositional approach to analyze the timing behavior of complex systems under different scheduling strategies. The final paper shows a new timing generation method for the performance analysis of embedded software.

20.1 Transformation Based Communication and Clock Domain Refinement for System Design

Ingo Sander, Axel Jantsch - *Royal Institute of Tech., Kista, Sweden*

20.2 Model Composition for Scheduling Analysis In Platform Design

Kai R. Richter, Dirk Ziegenbein, Marek Jersak, Rolf Ernst - *Tech. Univ. of Braunschweig, Braunschweig, Germany*

20.3 Timed Compiled-Code Simulation of Embedded Software for Performance Analysis of SOC Design

Jong-Yeol Lee, In-Cheol Park - *KAIST, Taejon, Korea*

Wednesday June 12

10:30 to 12:00

All speakers are denoted in bold

$ – denotes short paper

ß – denotes best paper

Session 21 – Videoed

rm: Auditorium B

EQUIVALENCE VERIFICATION

CHAIR: Ziyad Hanna - *Intel Corp., Haifa, Israel*
ORGANIZER: Shin-ichi Minato

Using an equivalence checker to prove the functional equivalence of two designs is a common and practical verification approach. In this session, new technologies are presented that enable extraction of complex circuits, allow sequential equivalence checking and handle hard-to-verify arithmetic operators.

21.1 Automated Equivalence Checking of Switch Level Circuits

Atanas N. Parashkevov - *Motorola, Inc., Mawson Lakes, Australia*
Simon Jolly - *Foursticks Pty. Ltd., Frewville, Australia*
Tim McDougall - *Motorola, Inc., Mawson Lakes, Australia*

21.2 A Practical and Efficient Method for Compare-Point Matching

Demos Anastasakis, **Robert Damiano** - *Synopsys, Inc., Hillsboro, OR*
Hi-Keung T. Ma - *Synopsys, Inc., Mountain View, CA*
Ted Stanion - *Synopsys, Inc., Hillsboro, OR*

21.3 Self-Referential Verification of Gate-Level Implementations of Arithmetic Circuits

Ying-Tsai Chang, Kwang-Ting (Tim) Cheng - *Univ. of California, Santa Barbara, CA*

Session 22

rm: Auditorium A

PANEL: WHITHER (OR WITHER?) ASIC HANDOFF

CHAIR: Michael Santarini - *EE Times, San Mateo, CA*
ORGANIZERS: Mark Miller, Sudhakar Jilla

The traditional ASIC netlist handoff is changing - but to what? Is RTL handoff finally a reality? Or, will a placement-based handoff model emerge? Are differences among underlying tool technologies and methodologies only cosmetic? Or, are there fundamental business and IP distinctions? These and other questions will be discussed as the panel examines the future of the designer - ASIC vendor relationship.

22.1 Whither (or Wither) ASIC Handoff?

Tommy Eng - *Tera Systems, Inc., Campbell, CA*
Sandeep Khanna - *Synopsys, Inc., Mountain View, CA*
Kamalesh Ruparel - *Cisco Systems, Inc., Sarratoga, CA*
Tom Russell - *IBM Microelectronics, Essex Junction, VT*
Kazu Yamada - *NEC Corp., Santa Clara, CA*

Design Methods Sessions are shaded purple. Embedded Systems Sessions are shaded grey.

Session 23

rm: 292

EMBEDDED SOFTWARE AUTOMATION: FROM SPECIFICATION TO BINARY

CHAIR: Joerg Henkel - *NEC Corp., Princeton, NJ*
ORGANIZERS: Marco Di Natale, Xiaobo (Sharon) Hu

The increasing embedded software content of electronic systems makes it important to automate various aspects of the software design flow. This session presents papers that represent advances in embedded software automation, including synthesis from synchronous specifications, automatic library mapping for complex functions using symbolic algebra, and re-targetability of binary utilities.

23.1 Software Synthesis from Synchronous Specifications Using Logic Simulation Techniques

Yunjian Jiang, Robert K. Brayton - *Univ. of California, Berkeley, CA*

23.2 Complex Library Mapping for Embedded Software using Symbolic Algebra

Armita Peymandoust - *Stanford Univ., Stanford, CA*
Tajana Simunic - *Hewlett-Packard Labs., Palo Alto, CA*
Giovanni De Micheli - *Stanford Univ., Stanford, CA*

23.3 Retargetable Binary Utilities

Maghsoud Abbaspour, Jianwen Zhu - *Univ. of Toronto, Toronto, ON, Canada*

Session 24

rm: 288

APPLICATIONS OF RECONFIGURABLE COMPUTING

CHAIR: Ivo Bolsens - *Xilinx, Inc., San Jose, CA*
ORGANIZERS: Grant E. Martin, Kurt Keutzer

This session demonstrates that Reconfigurable Computing has come of age. The first paper looks at how multimedia applications will benefit through dynamic reconfiguration of operation level parallelism. The second one builds a case for partial runtime reconfiguration, demonstrated on a networking application. The final paper is a case study in which what might normally be a software testbench for disk drive design is instead built as reconfigurable hardware, giving much higher performance.

24.1 Exploiting Operation Level Parallelism through Dynamically Reconfigurable Datapaths

Zhining Huang, Sharad Malik - *Princeton Univ., Princeton, NJ*

24.2 Dynamic Hardware Plugins for FPGAs with Partial Run-Time Reconfiguration

Edson L. Horta - *LSI-EPUSP-USP, Sao Paulo, Brazil*
John W. Lockwood - *Washington Univ., St. Louis, MO*
Dave Parlour - *Xilinx, Inc., San Jose, CA*
David Taylor - *Washington Univ., St. Louis, MO*

24.3 A Reconfigurable FPGA-Based Readback Signal Generator For Hard-Drive Read Channel Simulator

Jinghuan Chen, Jaekyun Moon, Kia Bazargan - *Univ. of Minnesota, Minneapolis, MN*

Session 25

rm: 287

NEW TEST METHODS TARGETING NON-CLASSICAL FAULTS

CHAIR: Rob Aitken - *Agilent Technologies, Santa Clara, CA*
ORGANIZERS: Miron Abramovici, T.M. Mak

Complexity of VLSI testing requires targeting new types of faults in addition to the classical stuck-at fault model. The session illustrates different aspects of this struggle.

25.1 Embedded Tutorial: Embedded Software-Based Self-Testing for SoC Design

Angela Krstic, Wei Cheng Lai, Li Chen, Kwang-Ting (Tim) Cheng - *Univ. of California, Santa Barbara, CA*
Sujit Dey - *Univ. of California at San Diego, La Jolla, CA*

25.2 A Novel Wavelet Transform Based Transient Current Analysis for Fault Detection and Localization

Swarup K. Bhunia, Kaushik Roy - *Purdue Univ., West Lafayette, IN*
Jaume Segura - *Balearic Islands Univ., Mallorca, Spain*

25.3S Signal Integrity Fault Analysis Using Reduced-Order Modeling

Amir Attarha, Mehrdad Nourani - *Univ. of Texas, Richardson, TX*

25.4S Enhancing Test Efficiency for Delay Fault Testing Using Multiple-Clocked Schemes

Jing Jia Liou, Li C. Wang, Kwang-Ting (Tim) Cheng - *Univ. of California, Santa Barbara, CA*
Jennifer Dworak, Ray Mercer - *Texas A&M Univ., College Station, TX*
Tom Williams - *Synopsys, Inc., Boulder, CO*

Wednesday June 12

2:00 to 4:00

All speakers are denoted in bold

S – denotes short paper

ß – denotes best paper

Session 26 – Videoed

rm: Auditorium B

SPECIAL SESSION: HOW DO YOU DESIGN A 10M GATE ASIC?

CHAIR: Ahmed A. Jerraya - *TIMA Lab., Grenoble Cedex, France*

ORGANIZERS: Ahmed A. Jerraya, Kurt Keutzer

ASIC design has always been challenging but an increasing number of design groups are unsuccessful at designs in excess of 4M logic gates. A leading industry analyst states that first-silicon success is only a tenth as likely at 10M gates as at lower complexity levels. Some designers have even claimed that design above the 4M logic gate complexity is simply impossible with the current generation of design tools. Nevertheless, a number of designers are successfully approaching the 10M gate complexity level. How are they doing it? In this session designers from three segments of the integrated-circuit design industry will describe key aspects of their design methodology that enable them to achieve silicon success on high complexity designs.

26.1 Going Mobile: The Next Horizon for Multi-Million Gate Designs in the Semiconductor Industry

Christian Berthet - *STMicroelectronics, Grenoble Cedex, France*

26.2 When 10M Gates Just Isn't Enough: The GPU Challenge

Chris Malakowsky - *NVidea, Santa Clara, CA*

26.3 Challenges in Achieving First-Silicon Success for 10M-Gate SoCs: A Silicon Engineering Perspective

Aurangzeb Khan - *Simplex Solutions, Inc., Sunnyvale, CA*

26.4 Panel Discussion: Is 10 M Gate ASIC Design Really as Easy as They Say?

Christian Berthet - *STMicroelectronics, Grenoble Cedex, France*
Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*
Kurt Keutzer - *Univ. of California, Berkeley, CA*
Aurangzeb Khan - *Simplex Solutions, Inc., Sunnyvale, CA*
Chris Malakowsky - *NVidea, Santa Clara, CA*
Ron Wilson - *ISD Magazine, San Mateo, CA*

Session 27

rm: Auditorium A

POWER DISTRIBUTION ISSUES

CHAIR: Sachin Sapatnekar - *Univ of Minnesota, Minneapolis, MN*

ORGANIZERS: Abhijit Dharchoudhury, Tadahiro Kuroda

Power distribution issues are becoming extremely important as levels of integration increase. The first paper describes a model-order reduction method for hierarchical power grid analysis. The second paper describes a frequency-domain macromodel for block current signatures. The third paper describes circuit models for the chip interface, and the fourth paper describes a method for analyzing symmetrical P/G networks. The final paper describes a method to optimize clock distribution networks using supply current folding.

27.1 HIPRIME: Hierarchical and Passivity Reserved Interconnect Macromodeling Engine for RLKC Power Delivery

Yahong Cao, YuMin Lee, Tsunghao Chen, Chung Ping Chen - *Univ. of Wisconsin, Madison, WI*

27.2 High-Level Current Macro-Model For Power-Grid Analysis

Srinivas Bodapati - *Univ. of Illinois, Urbana, IL*
Farid N. Najm - *Univ. of Toronto, Toronto, ON, Canada*

27.3S Macro-Modeling Concepts For The Chip Electrical Interface

Brian W. Amick - *Sun Microsystems, Austin, TX*
Claude R. Gauthier, Dean Liu - *Sun Microsystems, Sunnyvale, CA*

27.4S Modeling and Analysis of Regular Symmetrically Structured Power/Ground Distribution Networks

Hui Zheng, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

27.5 Clock Tree Optimization in Synchronous CMOS Digital Circuits for Substrate Noise Reduction Using Folding of Supply Current Transients

Mustafa Badaroglu, Kris Tiri, Stephane Donnay, Piet Wambacq - *IMEC, Leuven, Belgium*
Ingrid Verbauwhede - *Univ. of California, Los Angeles, CA*
Georges G. Gielen - *Katholieke Univ., Leuven, Belgium*
Hugo De Man - *IMEC, Leuven, Belgium*

Session 28

rm: 292

ADVANCES IN SYNTHESIS

CHAIR: Marek Perkowski - *Portland State Univ., Portland, OR*

ORGANIZERS: Soha M. Hassoun, Yusuke Matsunaga

This section presents advances to the state-of-the-art in three non-mainstream areas which show promise for the future. The first paper presents a powerful back-end optimizer for a leading asynchronous CAD tool which can be applied to large design examples (e.g. microprocessors). The second and third papers focus on the integration of asynchronous design with a commercial CAD tool flow. The fourth paper contributes a novel set of optimizing transformations for quantum Boolean circuits. The fifth paper significantly improves runtimes in SPP (sum of pseudo-products) minimization.

28.1 Resynthesis and Peephole Transformations for the Optimization of Large-Scale Asynchronous Systems

Tiberiu Chelcea, Steven M. Nowick - *Columbia Univ., New York, NY*

28.2S Design of Asynchronous Circuits by Synchronous CAD Tools

Alex Kondratyev - *Cadence Design Systems, Inc., Berkeley, CA*

Kelwin Lwin - *ReShape Inc., Mountain View, CA*

28.3S Implementing Asynchronous Circuits using a Conventional EDA Tool-Flow

Christos Sotiriou - *FORTH, Heraklion, Crete, Greece*

28.4 Transformation Rules for Designing CNOT-Based Quantum Circuits

Shigeru Yamashita - *NTT Communication Science Lab., Soraku-gun, Japan*

Kazuo Iwama, Yahiko Kamabayashi - *Kyoto Univ., Kyoto, Japan*

28.5 Fast Three-Level Logic Minimization Based on Autosymmetry

Anna Bernasconi, Valentina Ciriani, Fabrizio Luccio, Linda Pagli - *Univ. of Pisa, Pisa, Italy*

Session 29

rm: 288

ANALOG SYNTHESIS & DESIGN METHODOLOGY

CHAIR: C.-J. Richard Shi - *Univ. of Washington, Seattle, WA*

ORGANIZERS: Joel R. Phillips, Kartikeya Mayaram

This session presents new developments in algorithms and methodology for synthesis and systematic design of analog and mixed-signal circuits. Two papers present progress in automatic model generation for synthesis. The third paper presents exploration methods for high-level design of delta-sigma modulators, and the final paper presents an A/D converter design case study.

29.1 An Efficient Optimization-Based Technique to Generate Posynomial Performance Models for Analog Integrated Circuits

Walter P. Daems, Georges G. Gielen, Willy M. Sansen - *Katholieke Univ., Leuven, Belgium*

§ 29.2 Remembrance of Circuits Past: Macromodeling by Data Mining in Large Analog Design Spaces

Hongzhou Liu, Amit Singhee, Rob A. Rutenbar, L. Richard Carley - *Carnegie Mellon Univ., Pittsburgh, PA*

29.3 Optimal Design of Delta-Sigma ADCs by Design Space Exploration

Ovidiu Bajdechi, Johan H. Huijsing - *Delft Univ. of Tech., Delft, The Netherlands*

29.4 STUDENT DESIGN CONTEST: Systematic Design of a 200 Ms/s 8-bit Interpolating/Averaging A/D Converter

Jan Vandenbussche - *Katholieke Univ., Heverlee, Belgium*

Session 30

rm: 287

LOW-POWER PHYSICAL DESIGN

CHAIR: Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

ORGANIZERS: Chaitali Chakrabarti, Sarma Vrudhula

This session includes papers that address power optimization at the physical level. The first two papers focus on interconnect power estimation and optimization. The first paper describes a fast accurate method for power estimation using hierarchical Petri nets. The second paper presents a method for power-delay optimal repeater insertion along interconnects. The last two papers deal with novel circuit architectures. The third paper describes a novel method for power reduction in the clock distribution network for domino logic. The last paper shows how a gate virtual ground can be introduced to achieve a significant reduction in the leakage power of SRAMs.

30.1 Petri Net Modeling of Gate and Interconnect Delays for Power Estimation

Ashok K. Murugavel, Nagarajan Ranganathan - *Univ. of South Florida, Tampa, FL*

30.2 Power Estimation in Global Interconnects and Its Reduction Using a Novel Repeater Optimization Methodology

Pawan Kapur, Gaurav Chandra, Krishna C. Saraswat - *Stanford Univ., Stanford, CA*

30.3S Low-Swing Clock Domino Logic Incorporating Dual Supply and Dual Threshold Voltages

Seong-Ook Jung - *Univ. of Illinois, Urbana, IL*

Kiwook Kim - *Pluris Inc., Cupertino, CA*

Sung-Mo Steve Kang - *Univ. of California, Santa Cruz, CA*

30.4S DRG-Cache: A Data Retention Gated-Ground Cache for Low Power

Amit Agarwal, Hai Li, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

Wednesday June 12

4:30 to 6:00

All speakers are denoted in bold

S – denotes short paper

ß – denotes best paper

Session 31 📽 – Videoed

rm: Auditorium B

PANEL: UNIFIED TOOLS FOR SOC EMBEDDED SYSTEMS: MISSION CRITICAL, MISSION IMPOSSIBLE OR MISSION IRRELEVANT

CHAIR: Gary Smith - *Dataquest, San Jose, CA*
ORGANIZERS: Daya Nadamuni, Sharad Malik

As designers struggle with developing application solutions consisting of complex systems-on-a-chip with a significant software component, they must deal with a diversity of tools with very different philosophies and assumptions, to help manage this task. On one hand are tools which assume a clean separation between the hardware and software parts of the design with an abstraction of the hardware available for software development. On the other hand are tools that try to handle the hardware and software parts of the design concurrently. What drives these different philosophies? Which of these is critical for emerging system designs? Which of these is viable going forward? Our panel of experts consisting of designers, embedded software tool providers, system design tool providers and an academic will answer these challenging questions.

31.1 Unified Tools for SoC Embedded Systems: Mission Critical, Mission Impossible or Mission Irrelevant

Brian Bailey - *Mentor Graphics Corp., Wilsonville, OR*
Rick Chapman - *SuperH, Inc., Bristol, UK*
John Fogelin - *Wind River, Alameda, CA*
Kurt Keutzer - *Univ. of California, Berkeley, CA*
Grant Martin - *Cadence Design Systems, Inc., San Jose, CA*

Session 32

rm: Auditorium A

MULTI-VOLTAGE, MULTI-THRESHOLD DESIGN

CHAIR: Rajendran Panda - *Motorola, Inc., Austin, TX*
ORGANIZERS: Renu Mehra, Sarma Vrudhula

The availability of multiple supply voltages and dual threshold voltage offers new opportunities for making trade-offs between energy consumption and performance. The first paper presents a method to optimally assign high Vt transistors to cluster of low Vt gates for reducing the leakage power. The second paper describes a practical methodology for dual Vt assignment and gate sizing. The third paper presents a novel application for optimal use of multiple supply voltages.

32.1 Dynamic and Leakage Power Reduction in MTCMOS Circuits Using an Automated Efficient Gate Clustering Technique

Mohab H. Anis - *Univ. of Waterloo, Waterloo, ON, Canada*
Shawki M. Areibi - *Univ. of Guelph, Guelph, ON, Canada*
Mohamed K. Mahmoud, Mohamed Elmasry - *Univ. of Waterloo, Waterloo, ON, Canada*

32.2 Total Power Optimization By Simultaneous Dual-Vt Allocation and Device Sizing In High Performance Microprocessors

Tanay Karnik, Yibin Ye, James Tschanz, Liqiong Wei, Steven M. Burns - *Intel Corp., Hillsboro, OR*
Venkatesh Govindarajulu - *Intel Corp., Austin, TX*
Vivek K. De, Shekhar Y. Borkar - *Intel Corp., Hillsboro, OR*

32.3 An Optimal Voltage Synthesis Technique for a Power-Efficient Satellite Application

Dong-In Kang, Jinwoo Suh, Stephen P. Crago - *USC/ISI, Arlington, VA*

Design Methods Sessions are shaded purple. Embedded Systems Sessions are shaded grey.

Session 33

rm: 292

ADVANCED SIMULATION TECHNIQUES

CHAIR: L. Miguel Silveira - *Univ. of Lisbon, Lisboa, Portugal*

ORGANIZERS: Georges G. Gielen, Kartikeya Mayaram

This session presents progress in simulation techniques for analog systems. First, techniques are presented for simulating optical systems and then for fractional-N frequency synthesizers. Next we feature two papers on RF simulation: one to include frequency-domain models in time-domain simulation, one demonstrating purely time-domain techniques for close-spaced carriers. The final paper presents a novel approach to noise analysis for nonlinear circuits in the frequency domain.

33.1 Fast and Accurate Behavioral Simulation of Fractional-N Frequency Synthesizers and other PLL/DLL Circuits

Michael H. Perrott - *Massachusetts Institute of Tech., Cambridge, MA*

33.2 Time-Domain Steady-State Simulation of Frequency-Dependent Components using Multi-Interval Chebyshev Method

Baolin Yang, Joel R. Phillips - *Cadence Design Systems, Inc., San Jose, CA*

33.3S A Time-Domain RF Steady-State Method for Closely Spaced Tones

Jaijeet Roychowdhury - *Univ. of Minnesota, Minneapolis, MN*

33.4S An Algorithm for Frequency-Domain Noise Analysis in Nonlinear Systems

Giorgio Casinovi - *Georgia Institute of Tech., Atlanta, GA*

Session 34

rm: 288

DESIGN METHODOLOGIES MEET NETWORK APPLICATIONS

CHAIR: Anand Raghunathan - *NEC Corp., Princeton, NJ*

ORGANIZERS: Anand Raghunathan, Marco Di Natale

Networking chips represent a challenging class of applications for EDA tools and methodologies. This session contains presentations that showcase novel design methodologies developed to address performance and power issues in network processors and switch fabrics. The first paper presents an advanced memory management methodology for high-performance network processors. The second presentation addresses power analysis of switch fabrics used in network routers, while the final presentation discusses memory optimizations for single chip switch fabrics.

34.1 System-Level Performance Optimization of the Data Queuing Memory Management in High-Speed Network Processors

Chantal Ykman, Jurgen Lambrecht, Diederik Verkest, Francky Catthoor - *IMEC, Heverlee, Belgium*
Aris Nikologiannis - *Ellemedia, Athens, Greece*
George Konstantoulakis - *Inaccess Networks, Athens, Greece*

34.2 Analysis of Power Consumption on Switch Fabrics in Network Routers

Terry Tao Ye - *Stanford Univ., Stanford, CA*
Luca Benini - *Univ. di Bologna, Bologna, Italy*
Giovanni De Micheli - *Stanford Univ., Stanford, CA*

34.3 Memory Optimization in Single Chip Network Switch Fabrics

David J. Whelihan, Herman Schmit - *Carnegie Mellon Univ., Pittsburgh, PA*

Session 35

rm: 287

ADVANCES IN ANALOG MODELING

CHAIR: Alan Mantooth - *Univ. of Arkansas, Fayetteville, AR*

ORGANIZERS: Joel R. Phillips, Kartikeya Mayaram

This session features topics related to modeling of analog systems. The first paper presents a high-level behavioral model for coupled oscillators. The next paper seeks to apply formal methods to analog verification problems. The third paper discusses a technique for analyzing unsolvable systems that are possible to construct in the VHDL-AMS language. The final paper presents novel quadrature schemes for computing inductance in the presence of magnetically permeable materials.

35.1 Behavioral Modeling of (Coupled) Harmonic Oscillators

Piet Vanassche, Georges G. Gielen, Willy Sansen - *Katholieke Univ., Leuven, Belgium*

35.2 Model Checking Algorithms for Analog Verification

Walter Hartong, Lars Hedrich, Erich Barke - *Univ. of Hannover, Hannover, Germany*

35.3S Regularization of Hierarchical VHDL-AMS Models using Bipartite Graphs

Jochen Mades - *Infineon Tech., Munich, Germany*
Manfred Glesner - *Darmstadt Univ. of Tech., Darmstadt, Germany*

35.4S Improving the Generality of the Ficticious Magnetic Charge Approach to Computing Inductances in the Presence of Permeable Materials

Yehia M. Massoud - *Synopsys, Inc., Mountain View, CA*
Jacob K. White - *Massachusetts Institute of Tech., Cambridge, MA*

Thursday June 13

8:30 to 10:00

All speakers are denoted in bold

S – denotes short paper

ß – denotes best paper

Session 36 – Ukleoed

rm: Auditorium B

ADVANCES IN TIMING AND SIMULATION

CHAIR: David J. Hathaway - *IBM Corp., Essex Junction, VT*
ORGANIZERS: Louis Scheffer, Narendra V. Shenoy

This session addresses extensions to static timing to take into account statistical manufacturing variations, false paths and both. In addition to timing verification, the final paper focuses on inexpensive acceleration of functional verification by using FPGAs and a special compiler.

36.1 A General Probabilistic Framework for Worst Case Timing Analysis

Michael Orshansky, Kurt Keutzer - *Univ. of California, Berkeley, CA*

36.2S False Timing Path Identification using ATPG Technique and Delay-Based Information

Jing Zeng, Magdy Abadir - *Motorola, Inc., Austin, TX*
Jacob Abraham - *Univ. of Texas, Austin, TX*

36.3S False-Path-Aware Statistical Timing Analysis and Efficient Path Selection for Delay Testing and Timing Validation

Jing Jia Liou, Angela Krstic, Li C. Wang, Kwang-Ting (Tim) Cheng - *Univ. of California, Santa Barbara, CA*

36.4 A Fast, Inexpensive and Scalable Hardware Acceleration Technique for Functional Simulation

Srihari Cadambi, Chandra S. Mulpuri, Pranav N. Ashar - *NEC Corp., Princeton, NJ*

Session 37

rm: Auditorium A

PANEL: FORMAL VERIFICATION METHODS: GETTING AROUND THE BRICK WALL

CHAIR: David Dill - *Stanford Univ., Stanford, CA*
ORGANIZERS: Nate James, Shishpal Rawat

Do formal verification tools and methodologies require a drastic overhaul to move beyond equivalence checking? Equivalence checking catches errors in synthesis and local hand-modifications to designs. However, the really big problems are with "behavioral" errors and the real power of formal tools can be realized if we can address these errors. Some of our panelists feel that the designer can utilize and benefit from FV technology by making incremental changes to the design methodology. Others however argue that major changes are required to reap the "real" benefit of these new technologies. Just how much change is enough, what is the capacity of our current tools and what is limiting the full deployment of FV technology?

Our panel of experts, consisting of users, tool providers, and core engine builders, will answer these challenging questions. The panel will debate these issues while discussing real live examples from the users base. They will provide a perspective of how the progression of technology will bring to their user base "the real promise" of formal verification.

37.1 Formal Verification Methods: Getting Around the Brick Wall

Gérard Berry - *Esterel Tech., Villeneuve-Loubet, France*
Limor Fix - *Intel Semiconductors Ltd., Haifa, Israel*
Harry Foster- *Verplex Systems, Inc., Milpitas, CA*
Rajeev Ranjan - *Real Intent, Santa Clara, CA*
Gunnar Stalmarck - *Prover Tech., Inc., Stockholm, Sweden*
Curt Widdoes - *0-In Design Automation, San Jose, CA*

Session 38

rm: 292

ROUTING AND BUFFERING

CHAIR: Noel Menezes - *Intel Corp., Hillsboro, OR*

ORGANIZERS: Charles J. Alpert, Steven Teig

Buffering is a key aspect of interconnect design. It is crucial to meld routing and timing into a consistent framework for timing closure. This session covers a range of interconnect performance issues such as efficient interconnect synthesis, buffer planning with pin assignment, and implementation issues in global routing data structures.

38.1 S-Tree: A Technique for Buffered Routing Tree Synthesis

Milos Hrkic, John Lillis - *Univ. of Illinois, Chicago, IL*

38.2 An Algorithm for Integrated Pin Assignment and Buffer Planning

Hua Xiang, Xiaoping Tang, D. F. Wong - *Univ. of Texas, Austin, TX*

38.3 An Efficient Routing Database

Narendra V. Shenoy - *Synopsys, Inc., Bangalore, India*
William Nicholls - *Synopsys, Inc., Mountain View, CA*

Session 39

rm: 288

SYSTEM ON CHIP DESIGN

CHAIR: Rolf Ernst - *Tech. Univ. of Braunschweig, Braunschweig, Germany*

ORGANIZERS: Krzysztof Kuchcinski, Miodrag Potkonjak

SoC is the enabling technology that will close the gap between exponentially growing silicon potential and designers productivity. In modern design, memory most often dominates transistor budget. The first paper proposes solutions to smoothly integrate embedded memories in complex SoCs. The second paper introduces a revolutionary protocol design technique which enables exceptional improvements on industrial design. The final two papers address focused but important problems in System design: efficient use of background memory and design of multiprecision circuit.

39.1 Automatic Generation of Embedded Memory Wrapper for Multiprocessor SoC

Ferid Gharsalli, Samy Meftali, Frederic Rousseau, Ahmed A. Jerraya - *TIMA Lab., Grenoble, France*

39.2 A Novel Synthesis Technique for Communication Controller Hardware from Declarative Data Communication Protocol Specifications

Robert Siegmund, Dietmar Müller - *Tech. Univ. of Chemnitz, Chemnitz, Germany*

39.3S An Integrated Algorithm for Memory Allocation and Assignment in High-level Synthesis

Jaewon Seo, Taewhan Kim - *KAIST, Taejon, Korea*
P ræti R. Panda - *Synopsys, Inc., Mountain View, CA*

39.4S High-Level Synthesis of Multiple-Precision Circuits Independent of Data-Objects Length

Maria C. Molina, José M. Mendias, Román Hermida - *Complutense Univ., Madrid, Spain*

Session 40

rm: 287

TIMING ANALYSIS AND MEMORY OPTIMIZATION FOR EMBEDDED SYSTEMS

CHAIR: Giuseppe Lipari - *Scuola S. Anna, Pisa, Italy*

ORGANIZERS: Marco Di Natale, Xiaobo (Sharon) Hu

High performance embedded systems present many design challenges, e.g., timing analysis and memory management. Papers in this session introduce new techniques to tackle some of these challenges. The first paper presents a schedulability analysis algorithm for real-time systems. The second paper describes a technique to estimate execution time bounds with full consideration of cache effects. The last paper discusses optimization of scratch-pad memory.

40.1 Schedulability of Event-Driven Code Blocks in Real-Time Embedded Systems

Samarjit Chakraborty, Thomas Erlebach, Simon Kuenzli, Lothar Thiele - *ETH Zurich, Zurich, Switzerland*

40.2 Associative Caches in Formal Software Timing Analysis

Fabian Wolf - *Volkswagon AG, Wolfsburg, Germany*
Jan Staschulat, Rolf Ernst - *Tech. Univ. of Braunschweig, Braunschweig, Germany*

40.3 Compiler-Directed Scratch Pad Memory Hierarchy Design and Management

Mahmut T. Kandemir - *Penn State Univ., University Park, PA*
Alok Choudhary - *Northwestern Univ., Evanston, IL*

Thursday June 13

10:30 to 12:00

All speakers are denoted in bold

S – denotes short paper

ß – denotes best paper

Session 41 📽 – Videoed

rm: Auditorium B

PROCESSORS AND ACCELERATORS FOR EMBEDDED APPLICATIONS

CHAIR: Chris Rowen - *Tensilica, Santa Clara, CA*
ORGANIZERS: Kurt Keutzer, Majid Sarrafzadeh

The papers in this session explore the design challenges associated with taking an embedded application all the way to silicon. The first paper explores the design of a Rijndael processor. The second looks at a contemporary embedded processor design. Each of these two designs probes the state-of-the-art in performance. The third paper reviews architectural and micro-architectural issues in the development of an accelerator for network applications.

41.1 STUDENT DESIGN CONTEST: Unlocking the Design Secrets of a 2.29 Gb/s Rijndael Processor

Patrick R. Schaumont, Henry Kuo, Ingrid M. Verbauwhede - *Univ. of California, Los Angeles, CA*

41.2 The ICORE™ 520 MHz Synthesizable CPU Core

Naresh Soni - *STMicroelectronics, San Diego, CA*

41.3 A Flexible Accelerator for Layer 7 Networking Applications

Gokhan Memik, Bill Mangione-Smith - *Univ. of California, Los Angeles, CA*

Session 42

rm: Auditorium A

PANEL: WHAT IS THE NEXT EDA DRIVER?

CHAIR: Jan Rabaey - *Univ. of California, Berkeley, CA*
ORGANIZERS: Joachim Kunkel, Dennis Brophy

The PC industry was the major consumer of silicon in the 80's and 90's. It defined the requirements for EDA. In a world dominated by PC's, clock frequency was the ultimate measure of performance. Times have changed. Today wireless communications has replaced the PC as the primary driver. How we measure 'cutting edge' has also changed. From 'MHz' to weight, functions, hours of talk time and standby time. This change has created a significant impact on EDA, its innovation and product cycle, particularly in areas like low power design, mixed signal, platform based design, and system level design. Will consumer demand for electronics products continue with the wireless focus, or are their other electronics products looming that will shift consumer demand to alter the forces that drive EDA innovation?

42.1 What's the New EDA Driver?

Raul Camposano - *Synopsys, Inc., Mountain View, CA*
Rick Hetherington - *Nexsi Systems Corp., San Jose, CA*
Larry Lerner - *Agilent Tech., Westlake Village, CA*
Davoud Samani - *Infineon Tech., Wolfratshausen, Germany*

Design Methods Sessions are shaded purple. Embedded Systems Sessions are shaded grey.

Session 43

rm: 292

CROSS-TALK NOISE ANALYSIS AND MANAGEMENT

CHAIR: Cheng-Kok Koh - *Purdue Univ., West Lafayette, IN*

ORGANIZERS: Kaushik Roy, Noel Menezes

With the scaling of technology, cross-talk noise is becoming increasingly important. The papers in this session describe techniques to analyze and estimate cross-talk noise effects and present routing tools which consider cross-talk as a constraint.

43.1 Estimation of the Likelihood of Capacitive Coupling Noise

Sarma Vrudhula - *Univ. of Arizona, Tucson, AZ*
David Blaauw - *Univ. of Michigan, Ann Arbor, MI*
Supamas Sirichotiyakul - *Sun Microsystems, Boston, MA*

43.2 Crosstalk Noise Estimation for Noise Management

Paul B. Morton, Wayne Dai - *Univ. of California, Santa Cruz, CA*

43.3S Variable Frequency Crosstalk Noise Analysis: A Methodology to Guarantee Functionality from DC to FMAX

Byron Krauter, David J. Widiger - *IBM Corp., Austin, TX*

43.4S Towards Global Routing With RLC Crosstalk Constraints

James Ma, Lei He - *Univ. of Wisconsin, Madison, WI*

Session 44

rm: 288

TEST COST REDUCTION FOR SOCS

CHAIR: Yervant Zorian - *Virage Logic Inc., Fremont, CA*

ORGANIZERS: Seiji Kajihara, Kwang-Ting (Tim) Cheng

The papers in this session focus on test cost reduction for SoC designs. The proposed test compression and scheduling methods bring significant reduction of test application time, test data volume and/or power dissipation during testing. The first paper describes a method of encoding test data. The second paper presents control schemes for testing embedded cores. The last paper describes an integrated framework for SoC test automation.

44.1 Reduction of SOC Test Data Volume, Scan Power and Testing Time Using Alternating Run-length Codes

Anshuman Chandra, Krishnendu Chakrabarty - *Duke Univ., Durham, NC*

44.2 Embedded Test Control Schemes for Compression in SoCs

Douglas Kay, Sung Chung - *Cisco Systems, Inc., San Jose, CA*
Samiha Mourad - *Santa Clara Univ., Santa Clara, CA*

44.3 Integrated Wrapper/TAM Co-Optimization, Constraint-Driven Test Scheduling, and Tester Data Volume Reduction for SOCs

Vikram Iyengar, Krishnendu Chakrabarty- *Duke Univ., Durham, NC*
Erik Jan Marinissen - *Philips Research Labs., Eindhoven, The Netherlands*

Session 45

rm: 287

SCHEDULING TECHNIQUES FOR EMBEDDED SYSTEMS

CHAIR: Rolf Ernst - *Tech. Univ. of Braunschweig, Braunschweig, Germany*

ORGANIZERS: Diederik Verkest, Donatella Sciuto

More and more embedded systems contain multiple on-chip processors and memory and are often battery powered. In these systems energy efficiency is of extreme importance. This session combines papers that look at how scheduling can influence power dissipation in all parts of the system. The first paper looks at how to better parallelize an application on a multi-processor architecture. The second paper looks at how an OS scheduler can direct DRAM power mode management. The last paper investigates the influence of scheduling on battery lifetime.

45.1 Communication Based Power Management for Battery Efficient System Design

Kanishka Lahiri - *Univ. of California at San Diego, La Jolla, CA*
Anand Raghunathan - *NEC Corp., Princeton, NJ*
Sujit Dey - *Univ. of California at San Diego, La Jolla, CA*

45.2 Scheduler-Based DRAM Energy Management

Victor M. De La Luz, Anand Sivasubramaniam, Mahmut T. Kandemir, Vijaykrishnan Narayanan, Mary Jane Irwin - *Penn State Univ., University Park, PA*

45.3 An Integer Linear Programming Based Approach for Parallelizing Applications in On-Chip Multiprocessors

Ismail Kadayif, Mahmut T. Kandemir - *Penn State Univ., University Park, PA*
Ugur Sezer - *Univ. of Wisconsin, Madison, WI*

Thursday June 13

2:00 to 4:00

All speakers are denoted in bold

S – denotes short paper

ß – denotes best paper

Session 46 – Videoed

rm: Auditorium B

SPECIAL SESSION: DESIGNING SOCS FOR YIELD IMPROVEMENT

CHAIR: Srivaths Ravi - *NEC Corp., Princeton, NJ*
ORGANIZERS: Anand Raghunathan, Alfred E. Dunlop

The increasing scale and complexity of System-on-Chips, together with the emergence of new failure mechanisms in nanometer technologies, poses serious challenges to various steps of the SoC manufacturing process, including manufacturing test, defect diagnosis, yield enhancement, and reliability improvement. Conventional approaches to address these issues are giving way to solutions that increasingly involve special IP blocks embedded in the SoCs (called infrastructure IP) to help with the above steps. The first presentation will focus on how infrastructure IPs can be used to address various manufacturing challenges, ranging from manufacturing test and silicon debug to improving yield and reliability. The second presentation addresses a recent and growing trend in SoCs - the use of embedded reconfigurable logic. It covers the self-test, diagnosis, and repair for yield improvement of embedded FPGAs, and outlines how they can be used to test other embedded cores.

46.1 Embedded Tutorial: Embedding Infrastructure IP for SoC Yield Improvement

Yervant Zorian - *Virage Logic Inc., Fremont, CA*

46.2 Embedded Tutorial: Using Embedded FPGAs for SoC Yield Improvement

Miron Abramovici - *Agere Systems, Inc., Murray Hill, NJ*
Charles Stroud - *Univ. of North Carolina, Charlotte, NC*
Marty Emmert - *Wright State Univ., Dayton, OH*

Session 47

rm: Auditorium A

ADVANCES IN SAT

CHAIR: Joao Marques-Silva - *IST/INESC, Lisboa, Portugal*
ORGANIZERS: Malgorzata Marek-Sadowska, Soha M. Hassoun

This session focuses on different techniques to enhance Boolean SAT solvers. The first paper presents a proof engine to combine different SAT-solving strategies. The second paper utilizes symmetry to speed-up solvers. The third paper describes a tool that reports the percentage of search space explored by the solver. The fourth paper proposes several optimization techniques that can improve speed. The last paper combines circuit-based and CNF-based algorithms.

47.1 A Proof Engine Approach to Solving Combinational Design Automation Problems

Gunnar Andersson, **Per Bjesse**, Byron Cook - *Prover Tech., Portland, OR*
Ziyad Hanna - *Intel Corp., Haifa, Israel*

47.2 Solving Difficult SAT Instances in the Presense of Symmetry

Fadi A. Aloul, Arathi Ramani, **Igor Markov**, Karem Sakallah - *Univ. of Michigan, Ann Arbor, MI*

47.3 Satometer: How Much Have We Searched?

Fadi A. Aloul, Brian Sierawski, Karem Sakallah - *Univ. of Michigan, Ann Arbor, MI*

47.4S SAT with Partial Clauses and Back-Leaps

Slawomir Pilarski, Gracia Hu - *Synopsys, Inc., Beaverton, OR*

47.5S Combining Strengths of Circuit-Based and CNF-Based Algorithms For a High-Performance SAT Solver

Malay K. Ganai - *NEC Corp., Princeton, NJ*
Lintao Zhang - *Princeton Univ., Princeton, NJ*
Pranav Ashar, Aarti Gupta - *NEC Corp., Princeton, NJ*
Sharad Malik - *Princeton Univ., Princeton, NJ*

Session 48

rm: 292

INDUCTANCE AND SUBSTRATE ANALYSIS

CHAIR: Noel Menezes - *Intel Corp., Hillsboro, OR*

ORGANIZERS: Jaijeet Roychowdhury, Mustafa Celik

Substrate and inductance effects are becoming increasingly important in high-speed digital/mixed-signal integrated circuits and systems. The first three papers deal with aspects of inductance extraction, modelling and analysis. The remaining two papers propose methods for substrate modelling and extraction.

48.1 A Solenoidal Basis Method For Efficient Inductance Extraction

Hemant Mahawar, Vivek Sarin, Weiping Shi - *Texas A&M Univ., College Station, TX*

48.2 On the Efficacy of Simplified 2D On-Chip Inductance Models

Tao Lin, Michael W. Beattie, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

48.3 A Physical Model for the Transient Response of Capacitively Loaded Distributed RLC Interconnects

Raguraman Venkatesan, Jeffrey Davis, James Meindl - *Georgia Institute of Tech., Atlanta, GA*

48.4 HSpeedEX: A High-Speed Extractor for Substrate Noise Analysis in Complex Mixed-Signal SOC

Adil Koukab, Catherine Dehollain, Michel Declercq - *EPFL-LEG, Lausanne, Switzerland*

48.5 Combined BEM/FEM Substrate Resistance Modeling

Eelco Schrik, N. P. van der Meijs - *Delft Univ. of Tech., Delft, The Netherlands*

Session 49

rm: 288

DEVELOPMENT OF PROCESSORS AND COMMUNICATION NETWORKS FOR EMBEDDED SYSTEMS

CHAIR: Jan Rabaey - *Univ. of California, Berkeley, CA*

ORGANIZERS: Grant E. Martin, Majid Sarrafzadeh

Processors and their interconnect networks are the building blocks of the next generation of embedded system platforms. The first paper in this session examines system level design issues, including instruction set extensions, for wireless security. As current processing technology has given us the capability of incorporating multi-processors systems on a single chip, it is timely that the subsequent papers in this section examine system design issues associated with building communication systems for these processors.

49.1 System Design Methodologies for a Wireless Security Processing Platform

Srivaths Ravi, Anand Raghunathan, Nachiketh Potlapally, Murugan Sankaradass - *NEC Corp., Princeton, NJ*

49.2 Constraint-Driven Communication Synthesis

Alessandro Pinto, Luca P. Carloni, Alberto L. Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

49.3 Component-Based Design Approach for Multicore SoCs

Wander O. Cesário, Amer Baghdadi, Lovic Gauthier, Damien Lyonnard, Gabriela Nicolescu, Yanick Paviot, Sungjoo Yoo, Ahmed A. Jerraya - *TIMA Lab., Grenoble, France*
Mario D. Nava - *STMicroelectronics, Grenoble, France*

49.4 Traffic Analysis for On-Chip Networks Design of Multimedia Applications

Girish V. Varatkar, Radu Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

Session 50

rm: 287

MOVING TOWARDS MORE EFFECTIVE VALIDATION

CHAIR: Magdy Abadir - *Motorola, Inc., Austin, TX*

ORGANIZERS: Carl Pixley, Masahiro Fujita

Designs are becoming more and more complex and thus in order to achieve high functional quality, functional validation must become more effective. In this session, several successful approaches are presented towards this end: using formal specification to drive test-generation and coverage, Coverage hole analysis, Simulation-based sequential ATPG and direct/pseudo-random testing and formal verification.

50.1 Deriving a Simulation Input Generator and a Coverage Metric From a Formal Specification

Kanna Shimizu, David L. Dill - *Stanford Univ., Stanford, CA*

50.2 Hole Analysis for Functional Coverage Data

Oded Lachish, Eitan Marcus, Shmuel Ur, Avi Ziv - *IBM Haifa Research Lab., Haifa, Israel*

50.3 Effective Safety Property Checking Using Simulation-Based Sequential ATPG

Shuo Sheng - *Rutgers Univ., Piscataway, NJ*
Koichiro Takayama - *Fujitsu Labs. Ltd., Sunnyvale, CA*
Michael S. Hsiao - *Virginia Tech., Blacksburg, VA*

50.4 A Comparison of Three Verification Techniques: Directed Testing, Pseudo-Random Testing and Property Checking

Mike G. Bartley, Darren Galpin, Tim Blackmore - *Infineon Tech., Bristol, Great Britain*

Thursday June 13

4:30 to 6:00

All speakers are denoted in bold

S – denotes short paper

ß – denotes best paper

Session 51 – Videoed

rm: Auditorium B

SPECIAL SESSION: ENERGY EFFICIENT MOBILE COMPUTING

CHAIR: Enrico Macii - *Politecnico di Torino, Torino, Italy*
ORGANIZER: Mani Srivastava

This special session will address issues related to the design of computing systems operating at low-power regimes and supporting wireless communication and network connection. Speakers will provide their perspectives regarding three key components of these kinds of systems. The first talk will face the problem of designing low-energy communication protocols; state-of-the-art solutions will be illustrated, also by way of examples. The second presentation will address design and implementation issues of energy-efficient digital architectures for signal processing. Finally, in the third paper, energy considerations concerning RF and mixed-signal circuits to be used in mobile computing systems will be discussed.

51.1 Energy-Efficient Communication Protocols

Carla F. Chiasserini - *Politecnico di Torino, Torino, Italy*
Pavan Nuggehalli, Vikaram Srinivasan, **Ramesh R. Rao** - *Univ. of California at San Diego, La Jolla, CA*

51.2 Reliable and Energy-Efficient Digital Signal Processing

Naresh R. Shanbhag - *Univ. of Illinois, Urbana, IL*

51.3 CMOS: A Paradigm for Low-Power Wireless?

Michiel Steyaert, **Peter Vancorenland** - *Katholieke Univ., Leuven, Belgium*

Session 52

rm: Auditorium A

FLOORPLANNING AND PLACEMENT

CHAIR: Ralph Otten - *Delf Univ. of Tech., Delf, The Netherlands*
ORGANIZERS: Ralph Otten, Steven Teig

In the past many representations for floorplans and rectangle dissections have been found. How to use these in a productive way, for example in optimization with the right objectives, is far from trivial. In this session ideas from combining representations to get better solutions faster to working with multiple constraints and objectives, will be presented.

52.1 TCG-S: Orthogonal Coupling of P*-admissible Representations for General Floorplans

Jai Ming Lin - *National Chiao Tung Univ., Hsinchu, Taiwan, ROC*
Yao Wen Chang - *National Taiwan Univ., Taipei, Taiwan, ROC*

52.2 Floorplanning with Alignment and Performance Constraints

Xiaoping Tang, D. F. Wong - *Univ. of Texas, Austin, TX*

52.3 Algorithms for Simultaneous Satisfaction of Multiple Constraints and Objective Optimization in a Placement Flow with Application to Congestion Control

Ke Zhong, Shantanu Dutt - *Univ. of Illinois, Chicago, IL*

Design Methods Sessions are shaded purple. Embedded Systems Sessions are shaded grey.

Session 53

rm: 292

CIRCUIT EFFECTS IN STATIC TIMING

CHAIR: Jamil Kawa - *Synopsys, Inc., Mountain View, CA*

ORGANIZERS: Chandu Visweswariah, Louis Scheffer

Static timing analysis increasingly needs to take circuit effects into account. This session presents novel approaches to incorporating delay changes due to power/ground noise, interconnect loading and crosstalk during static timing. The final paper is devoted to a study of electrostatic discharge failures.

53.1 Coping with Buffer Delay Change Due to Power and Ground Noise

Lauren Chen - *Avant! Corp., Fremont, CA*
Malgorzata Marek-Sadowska, Forrest Brewer - *Univ. of California, Santa Barbara, CA*

53.2S Osculating Thevenin Model For Predicting Delay and Slew of Capacitively Characterized Cells

Bernard N. Sheehan - *Mentor Graphics Corp., Willsonville, OR*

53.3S Timed Pattern Generation for Noise-on-Delay Calculation

Seung Hoon Choi - *Purdue Univ., West Lafayette, IN*
Florentin Dartu - *Intel Corp., Hillsboro, OR*
Kaushik Roy - *Purdue Univ., West Lafayette, IN*

53.4 VeriCDF: A New Verification Methodology for Charged Device Failures

Jaesik-Lee - *Lucent Tech., Murray Hill, NJ*
Ki-Wook Kim - *Pluris Inc., Cupertino, CA*
Sung-Mo Steve Kang - *Univ. of California, Santa Cruz, CA*

Session 54

rm: 288

DESIGN SPACE EXPLORATION FOR EMBEDDED SYSTEMS

CHAIR: Henk Corporaal - *IMEC/DESICS, Leuven, Belgium*

ORGANIZERS: Jo Dale Carothers, Luca Benini

This session encompasses aspects of design exploration for embedded systems. The first paper presents a methodology for exploring the design space of packet processing devices on the system level. The next paper presents a technique for energy estimation and optimization of embedded systems. The session concludes with a paper on energy reduction techniques for SDRAM memory systems.

54.1 A Framework for Evaluating Design Tradeoffs In Packet Processing Architectures

Lothar Thiele, Samarjit Chakraborty, Matthias Gries, Simon Kuenzli - *ETH Zurich, Zurich, Switzerland*

54.2 Energy Estimation and Optimization of Embedded VLIW Processors Based on Instruction Clustering

Andrea Bona - *ALari, Lugano, Switzerland*
Mariagiovanna Sami, Donatella Sciuto - *Politecnico di Milano, Milano, Italy*
Cristina Silvano - *Univ. di Milano, Milano, Italy*
Vittorio Zaccaria, - *Politecnico di Milano, Milano, Italy*
Roberto Zafalon - *STMicroelectronics, Agrate Brianza, Italy*

54.3 Energy Exploration and Reduction of SDRAM Memory Systems

Yongsoo Joo, Yongseok Choi, Hojun Shim, Hyung Gyu Lee, Kwanho Kim, Naehyuck Chang - *Seoul National Univ., Seoul, Korea*

Session 55

rm: 287

BEHAVIORAL SYNTHESIS

CHAIR: Petru Eles - *Linköping Univ., Linköping, Sweden*

ORGANIZERS: Ahmed A. Jerraya, Krzysztof Kuchcinski

Behavioral synthesis has been around for a long time but it is only now that it is addressing issues that will make it directly useful for designers. The first paper bridges the gap between behavioural synthesis and processor design using innovative synthesis techniques. The second paper leverages on engineering change paradigms to develop more flexible design flow. The last paper proposes a generic scheme for applying engineering changes to an arbitrary behavioural synthesis problem.

55.1 Coordinated Transformations for High-Level Synthesis of High Performance Microprocessor Blocks

Sumit Gupta - *Univ. of California, Irvine, CA,*
Timothy Kam, Michael Kishinevsky - *Intel Corp., Hillsboro, OR*
Shai Rotem - *Intel Corp., Haifa, Israel*
Nick Savoiu, Nikil Dutt, Rajesh Gupta, Alex Nicolau - *Univ. of California, Irvine, CA*

55.2 Forward-Looking Objective Functions: Concept And Applications In High Level Synthesis

Jennifer L. Wong, Seapahn Megerian, Miodrag Potkonjak - *Univ. of California, Los Angeles, CA*

55.3 ILP-Based Engineering Change

Farinaz Koushanfar - *Univ. of California, Berkeley, CA*
Jennifer L. Wong, Jessica Feng, Miodrag Potkonjak - *Univ. of California, Los Angeles, CA*

MONDAY TUTORIAL 1 - AN INTRODUCTION TO EMBEDDED SOFTWARE: ISSUES, TOOLS AND METHODS - FOR HW AND EDA DESIGNERS

Room: 294
Lunch in room 296

ORGANIZER: Marco Di Natale - *Scuola Superiore S. Anna, Pisa, Italy*
PRESENTERS: Frank Pospiech - *Alcatel, Zaventem, Belgium*
Krithi Ramamritham - *Indian Institute of Tech., Bombay, India*
Bran Selic - *Rational Software, Kanata, ON, Canada*
Gjalt de Jong - *Telelogic Components AB, Leuven, Belgium*

Audience: The tutorial is primarily intended for HW oriented designers and EDA designers, who due to growing software issues, need an introduction to fundamental methodologies, tools and algorithms for embedded real-time software design. The tutorial starts with fundamental issues and introductory material which is necessary to understand the state of the art in software development's best practices but also addresses major future areas of research and industrial practice.

Description: The tutorial focuses on the main problems related to embedded software design. We have divided the tutorial into 4 parts. The first part is an overview, which covers architectural models as well as tradeoffs and fundamental issues in the design and development of the software structure, from hardware dependent software to operating system, middleware and application layers. The second part addresses real-time operating systems, real-time analysis and guaranteed scheduling.

This section starts with an overview of common RTOS architectures and services and a discussion of major commercial RTOS capabilities together with real-life implementation issues. Current best practices in real-time scheduling and resource management, starting from the well-known Rate Monotonic policy are addressed.

The third and fourth sections cover ESW methodology and tools focusing on how to achieve higher productivity through automation. The tutorial introduces the use of visual design notations to describe embedded programs and features a survey of existing CASE (Computer Aided Software Engineering) tools that provide higher productivity and higher quality software by generation of code from visual designs. Among the existing models and tools, the tutorial focuses especially on UML (Unified Modeling Language) and SDL (Specification and Description Language), today the dominant visual design notations. Capabilities and limitations of both models in the context of real design practice are discussed.

The talks will also emphasize future trends and take a look at advanced issues such as the perspectives for a two language merger and the evolution of the standards.

Tutorial 2 — 9:00 AM - 5:00 PM — Friday, June 14

Tutorials are held at the Ernest N. Morial Convention Center.

8:00 AM - 1:00 PM ....Tutorial Registration Open
8:00 AM .....Continental Breakfast
9:00 AM - 5:00 PM ....Tutorials
12:00 Noon.....Lunch (room 393)

TUTORIAL 2 - INTELLECTUAL PROPERTY DESIGN AND INTEGRATION FOR SOCS

Room: 291

ORGANIZERS: Ralf Seepold - *FZI, Karlsruhe, Germany*
Natividad Martínez Madrid - *FZI, Karlsruhe, Germany*

PRESENTERS: Ralf Seepold - *FZI, Karlsruhe, Germany*
Martin Radetzki - *sci-worx GmbH, Hannover, Germany*
Janick Bergeron - *Qualis Design Corp., Ottawa, ON, Canada*
Volker Meyer zu Bexten - *ATMEL Germany GmbH, Ulm, Germany*
Grant Martin - *Cadence Design Systems, Inc., Berkeley, CA*
Michael Payer - *Infineon Technologies AG, Munich, Germany*

Audience: IP users and providers; SoC designers and integrators; design engineers, researchers and managers interested in updating their knowledge on methodologies and tools for IP design and integration.

Description: The complexity of current system design in networking, high-speed links, multimedia, wireless and automotive domains can be managed by applying Intellectual Property (IP) reuse. The application of reuse methodologies for System-on-Chip (SoC) design has already proven its validity by bridging the productivity gap, meeting critical time-to-market objectives, reducing costs, reducing design errors, and easing verification and testing.

The aim of this tutorial is to provide an updated overview on the main methodologies, techniques and tools to develop IP-based SoC design. Furthermore, special attention will be dedicated to selected and innovative hot-topics in the area.

The first aspect to be highlighted is IP qualification. Quality is becoming a decisive factor in the IP business. Customers often distrust the suppliers due to earlier bad experiences. The tutorial will present the quality criteria most important to facilitate successful IP reuse. Reusability should be applied not only to design but also to verification as a productivity enhancement. The tutorial will give an answer to the question of IP verification by introducing a best-in-class methodology for the functional verification of IP. After that, the tutorial will move into the challenges of analog and mixed-signal IP. Taking into account the increasing amount of SoCs incorporating analog components, more and more designers will have to face this challenge. A major key to the SoC design methodologies incorporating high levels of IP reuse is the application of platform-based design. The tutorial will define platform-based design, and describe the major methodologies for IP design and integration in this context, including system-level design, logical design, and physical design and integration as well as software IP and analogue-mixed-signal design issues, specifically as they relate to design platforms. Finally, the tutorial will provide experiences and practical aspects of IP integration from the point of view of an IP user, incorporating internal and external IPs into a custom specific SoC.

TUTORIAL 3 - MODELING TECHNOLOGY FOR HIGH FREQUENCY DESIGN

Room: 293

ORGANIZER: Joel R. Phillips - *Cadence Berkeley Labs., San Jose, CA*
PRESENTERS: Andreas Cangellaris - *Univ. of Illinois, Urbana, IL*
Luca Daniel - *Univ. of California, Berkeley, CA*
Joel R. Phillips - *Cadence Berkeley Labs., San Jose, CA*
Ken Shepard - *Columbia Univ., New York, NY*

Audience: The intended audience includes CAD tool developers, R&D engineers, and academic researchers.

Description: One of the fundamental challenges of design automation is the construction and manipulation of models that provide a bridge between different levels of abstraction in the representation of a physical system. Model reduction is a popular approach for automatically generating higher-level models from circuit- and physical- level system descriptions. This tutorial focuses on model reduction algorithms and their practical application to a broad range of problems in electromagnetic modeling, IC interconnect analysis, analog/RF circuit modeling, and MEMS.

The first part of the tutorial features background material necessary to understand the mathematics underlying modern model reduction algorithms, formulate modeling tasks as reduction problems, and successfully apply reduction algorithms. We discuss properties of rational approximation, theory and implementation of Krylov subspace algorithms such as PVL, Arnoldi, and PRIMA, and physical constraints such as passivity that must be preserved to ensure generation of well-behaved models.

Second, we discuss application of model reduction algorithms to design of circuits operating at gigahertz frequencies. We begin by analyzing requirements for electromagnetic modeling, including hierarchical interconnect models that incorporate increasingly sophisticated physical modeling, and new approaches necessary to treat on-chip passive components such as integrated inductors. We will work through examples of how model reduction algorithms can be used to generate circuit models from EM analysis codes, as well as how model reduction can be used to solve several problems arising in construction of EM analysis codes themselves.

Next, we consider model reduction techniques applied to high-frequency interconnect analysis on a large, full-chip scale. This includes techniques for extracting lumped quasi-static R, L, C models on a full-chip basis and combining these with model-order reduction techniques to analyze analog effects in the transmission of digital data across the chip (timing and signal integrity).

Finally, we survey application of model reduction algorithms to wider classes of systems, drawing examples from microelectromechanical systems modeling and RF circuit analysis.

TUTORIAL 4 - USING SYSTEMC™ FOR SYSTEM LEVEL MODELING AND DESIGN

Room: 294

ORGANIZERS: Kevin Kranen - *Synopsys, Inc., Mountain View, CA*
Mike Baird - *Willamette HDL, Inc., Beaverton, OR*
PRESENTERS: Mike Baird - *Willamette HDL, Inc., Beaverton, OR*
Rob Slater - *Motorola Semiconductor Israel, Ltd. (MSIL), Herzelia, Israel*
John Sanguinetti - *Forte Design Systems, San Jose, CA*

Audience: The tutorial is intended for system-oriented design and verification engineers, deeply embedded software and hardware developers and EDA tool developers who want to learn about effective system design and verification methodologies that utilize the newly-emerging SystemC language.

Description: This tutorial focuses on the process of capturing, verifying and refining a system-level design from a concept, expressed in an executable functional specification to a ready-to-implement fully-specified architecture, leveraging the SystemC language.

First, we survey the different languages in use today, including SystemC, Verilog, VHDL, "e", OpenVera, C/C++, and SuperLog, highlighting the capabilities of each for modeling a complete system at various levels of abstraction. Each language will be examined for its capability to facilitate RTL design, Verification, System design and Embedded Software development.

Next, we present an overview of SystemC v2.0, highlighting key capabilities of the SystemC language, specifically in the context of system design methodologies. We will share prototypical system-level design flows in use today, introducing the concepts of communications and functional refinement as well as defining levels of abstraction through the flow. This will be followed by a guided tour of the key constructs of the SystemC language, focusing on those that are critical to system-level modeling and to making early architectural tradeoffs, including modules, ports, channels, interfaces, processes, transactions and high-level datatypes.

An experienced user of SystemC will share a detailed view of the design flow his team used for several chip projects, outlining both the improvements and the caveats they experienced using SystemC. Finally, we will present a more detailed view on how SystemC can be used to speed system-level verification, while sharing new language concepts and constructs under development within the Open SystemC Initiative that simplify and extend the ability of SystemC for this purpose. Concepts covered include randomization, constraints, weighting and transactors.

SystemC is a standard design and verification language built in C++ that spans from concept to implementation in hardware and software. The SystemC platform, which includes the SystemC specification, source code and reference manual, can be downloaded at www.systemc.org.

SystemC is a trademark of the Open SystemC Initiative.

Tutorial 5 — 9:00 AM - 5:00 PM Friday, June 14

TUTORIAL 5 - PHYSICAL CHIP IMPLEMENTATION: HOT SPOTS AND BEST PRACTICES Room: 295

ORGANIZER: Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*
PRESENTERS: Paul Rodman - *ReShape, Inc., Mountain View, CA*
Paul Villarubia - *IBM Corp., Austin, TX*
Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*

Audience: The target audience includes (1) physical implementation methodologists and CAD system integrators (e.g., in the COT context), (2) EDA researchers and developers, and (3) system and circuit designers and design project managers who would benefit from understanding the limitations and capabilities of leading-edge design technology. Attendees should have some background knowledge of physical design and back-end methodology.

Description: A reliable physical implementation path from RTL to GDSII is more than the sum of its parts. Successful chip implementation must focus on "hot spots" in the flow and work around tool limitations. At the same time, resource constraints must be met. For example, a COT team with limited CAD resources must usually rely on a mostly off-the-shelf flow, unlike the team at an ASIC design center or IDM. This tutorial will present the state of existing capabilities and "best practices", including specifics of vendor tools, tool-independent technology considerations, and insight into internal design capabilities. After establishing a baseline overall physical implementation methodology, the tutorial will address the following "hot spots".

0. Early decisions in project bringup, including use of cores and other third-party IP, use of hierarchy, RTL practices (e.g., registered-in / registered-out design and other "rules of the tavern"), implications of test strategy (e.g., scan BIST), pad layout implications, and choice of library.

1. Modern timing optimization and closure methodology at synthesis, placement, and detailed routing stages of implementation, using degrees of freedom such as fanout tree rebuilding, repeater/buffer insertion, sizing, and rewiring. The discussion will center on use of recent integrated placement and timing convergence tools, and also include congestion management in synthesis and RTL coding, as well as calibration and proper use of timing-driven features.

2. Signal integrity methodology, including management of crosstalk-induced noise and delay variation, inductance modeling, IR drop and ground bounce.

3. Hierarchy management, including advantages and disadvantages of hierarchical vs. flat, with respect to repeater insertion, pin assignment, hierarchy reconciliation, and performance macromodeling and analysis.

4. Floorplanning, including (i) creation of P&R blocks from the logical hierarchy, (ii) the use of abutment, repeater blocks, and bonus/spare cells and interconnects within the range of floorplanning approaches, (iii) consequences of area-I/O vs. peripheral I/O, and (iv) other considerations such as I/O bound "sparse" chip design and datapath planning.

5. Methodology for on-chip power and clock planning and distribution.

6. Verification issues, including manufacturability (antenna rule design and verification, area fill sub-flow, etc.), overall physical design integration issues (DRC/LVS), and the range of necessary equivalence checks.

7. Packaging, including flip-chip and I/O cell issues, system/package/chip codesign issues, and VDD/VSS and I/O distribution.

8. Other issues as time permits, including (i) adoption of new and innovative design tools and technologies, and (ii) the role of design verification, validation and integration (third-party IP issues, test benches, use of automated test and lab equipment, etc.).

TUTORIAL 6 - NEW COMPUTING PLATFORMS FOR EMBEDDED SYSTEMS

Room: 285

ORGANIZERS: Frank Vahid - *Univ. of California, Riverside & Center for Embedded Computer Systems, UC Irvine, Irvine, CA*
Walid Najjar - *Univ. of California, Riverside, CA*
PRESENTERS: Joerg Henkel - *NEC C&C Research Labs., Princeton, NJ*
Walid Najjar - *Univ. of California, Riverside, CA*
Frank Vahid - *Univ. of California, Riverside & Center for Embedded Computer Systems, UC Irvine, Irvine, CA*
Kees Vissers - *TriMedia Technologies, Milpitas, CA & Univ. of California, Berkeley, CA*

Audience: This tutorial is intended for embedded system designers, system-level CAD tool developers, and researchers, wanting to learn about the range of computing platforms available for embedded computing systems.

Description: The variety of computing platforms available to embedded system designers has grown tremendously in the past decade, well beyond the standard platforms of microcontrollers and 486 processors. The new platforms provide superb performance, power and cost points. This tutorial, targeted to embedded system designers, design automation developers, and researchers, focuses on the new platform landscape. The tutorial will highlight the workhorses, including standard microprocessors, microcontrollers and DSPs, with emphasis on popular devices like MIPS and ARM. It will cover field-programmable and reconfigurable logic devices, with discussion on their use in end-products. It will study new single-chip devices having both microprocessor and configurable logic, and other uses of on-chip configurable logic. The tutorial will discuss customizable processors (ASIPs), as well as new domain-specific processors like video and network processors. It will describe tuning of applications with platforms. It will conclude with a discussion of tool and methodology requirements, and a look to the future. Discussion of power, performance and cost metrics, of appropriateness of platforms to domains, and of design automation requirements and needs, will be included throughout.

Workshop on Teaching Functional Verification

Sunday, June 9

12:00 PM - 5:15 PM Room: 285

Recently, the chip design industry's focus on functional verification has exposed a shortage of verification engineers. With up to 70% of the design cycle spent in functional verification, it is increasingly difficult to staff a team of talented verification engineers. Today's verification engineer must be aware of all of the available methodologies and have an understanding of the underlying technology. This body of knowledge includes:

- Writing quality test plans
- Creating a balance of deterministic and random based testbenches
- Understanding the appropriate use of formal techniques and familiarity with the underlying algorithms
- Comprehending simulation engine algorithms
- Utilizing coverage techniques

Several universities, partnered with industry, identified the need for additional engineering curriculum in functional verification and are now teaching full semester classes at both the undergraduate and graduate levels. These classes reflect the realities of today's complex SOC and custom designs and provide students with insight on the emerging verification career path, an understanding of the verification process, and a working knowledge of the basic verification methodologies. This workshop will share the experiences and resources of these classes, and will include teaching materials, textbook overviews, lab exercises, grading and testing strategy, and EDA tools. Furthermore, this workshop will enable other university professors to join the collaborative efforts to refine and extend the teaching of functional verification.

ORGANIZERS: Bruce Wile - *IBM Server Group Verification Lead*
Steven P. Levitan - *Univ. of Pittsburgh*
Vijaykrishnan Narayanan - *Penn State Univ.*
John Goss - *North Carolina State Univ.*

REGISTRATION INSTRUCTIONS:

No Conference Registration is needed.

$40.00 *ACM/IEEE Members*
$60.00 *Non-Members*

SCHEDULE:

12:00 PM Lunch (room 285)
1:00 PM Welcome and Workshop Overview: Bruce Wile, Steven Levitan & Vijaykrishnan Narayanan
1:15 PM Textbook Overviews: Janick Bergeron - *Qualis Design Corp.* & Faisal Haque - *Cisco Systems*
2:00 PM Course Organization and Management: Vijay Narayanan, Steven P. Levitan and John Goss
2:45 PM Lab Exercise Overview: Bruce Wile
3:30 PM Break
3:45 PM Automated Testbench Concepts: Matthew Morley - *Verisity Design, Inc.*
4:30 PM Formal Verification using the Rulebase Model Checker: Yaron Wolfsthal - *IBM Research*
5:15 PM Adjourn

Introduction to Chips and EDA for a General Audience

Monday, June 10

10:00 AM - 12:00 PM Room: 288

This workshop provides:

- An explanation for the layman of how chips are made
- A portrayal of chip design using Electronic Design Automation
- An opportunity to see and touch the parts that make up chips and electronic products
- A non-threatening, fun event with a basic, working knowledge to take away
- An understanding of why the EDA industry can be a good financial investment

This workshop is for:

- Non-engineering staff from technology companies
- Analysts and media people unfamiliar with EDA and semiconductor industries
- Educators and students who are curious about chip technology

REGISTRATION INSTRUCTIONS:

No Conference Registration is needed.

$10.00 Registration Fee

Tutorial Objectives:

- Provide knowledge and understanding of EDA and semiconductors to non-technical people
- Present information in a non-threatening, fun environment
- Use hands-on parts (wafers, chips, masks...) for an enhanced experience
- Encourage people to join the EDA industry
- Promote the EDA industry as a good financial investment
- Entice audience to learn more
- Address ongoing requests to help non-technical people in our industry understand what we do!

PRESENTER: Karen Bartleson, Synopsys, Inc.

Workshop for Women in Design Automation 1:15 PM - 4:00 PM Monday, June 10

Silk Purses and Sow's Ears: Turning Obstacles into Opportunity

Room: 286

WORKSHOP CHAIR:
Jan Willis,
Simplex Solutions, Inc.

More and more women are succeeding in technology, but a significant gap still exists between where we are today and where we have the potential to be in the next decade. Those who have succeeded can tell you about the obstacles, and the different ways they have used their strengths to overcome them. In this year's workshop, you'll once again have the unique opportunity to get advice and coaching from successful leaders across the industry as we examine ways to turn imperfect situations into glittering successes, much like the saying about turning sow's ears into silk purses.

SCHEDULE:

1:15 PM - 2:00 PM Registration and buffet lunch
2:00 P M - 3:45 PM Keynote Address and Panel
3:45 P M - 4:00 PM Achievement Award Ceremony:
Join us as we honor the recipient of this year's Marie R. Pistilli Women in EDA Achievement Award.
4:00 PM Cocktail Reception:
Sponsored by the EDA Consortium

ORGANIZERS: Karen Bartleson - *Director of Interoperability, Synopsys, Inc.*
Janet Greene - *Sr. Marcom Manager, Simplex Solutions, Inc.*
SY Tan-Stahel - *Vice President of Marketing, 1st Silicon*
Sonja Wilkerson - *Vice President of Human Resources, Sequence Design, Inc.*

STEERING COMMITTEE: Mar Hershenson - *CTO, Barcelona Design, Inc.*
Nanette Collins - *Publicity Chair, 39th DAC*
Marie R. Pistilli - *Co-Chair, Board of Directors, MP Associates, Inc.*

Keynote Address
Chris King
President and CEO, AMI Semiconductor
Chris shares her experience from rising through the ranks at IBM, launching IBM's ASIC business, making it the number one ASIC business in the world, and now becoming the first woman CEO of a semiconductor company. She addresses how to overcome stereotypes, position yourself for the plum assignment, use risk to your advantage, and fight that feeling of isolation when you're the only woman in the room, as well as how to find a mentor or coach. She'll give you her top five strategies for success in the challenging world of technology.

Panel: Coaching & Feedback: Do I Need It and Where Do I Get It?

Moderator: Kathleen Doler - *Electronic Business*

Successful industry veterans will share their experiences in overcoming obstacles in the workplace, how they've used feedback and coaching to their advantage and where they've found it.

Diane Bryant - *Intel Corp.*
Deirdre Hanford - *Synopsys, Inc.*
Jim Hogan - *Cadence Design Systems, Inc.*
Teresa Meng - *Atheros Communications*
Michele Lane Reitz - *Synplicity, Inc.*

REGISTRATION INSTRUCTIONS:

No Conference Registration is needed.

$40.00 ACM/IEEE Members
$60.00 Non-Members

Interoperability Workshop

Monday, June 10

12:00 PM - 5:00 PM Room: 285

This year's DAC is hosting the third Workshop on Interoperability, a subject of perpetual and passionate interest. What progress has been made and what lies ahead?

Designers are still struggling with advancing technology, growing system complexity and shorter schedules. Tools flows are becoming more complicated. EDA companies are merging and offering highly-integrated "complete" solutions. DA Managers ask for better tools, but can't afford their evaluation, while universities and small EDA companies strive to get innovative point tools incorporated. System and Semiconductor companies want to mix and match best-of-breed tools with their own software to gain a competitive advantage.

Since the last Workshop, the Open Access Coalition has been formed and established a standard API for design data access, based on Cadence's Genesis Data Model and its source code. Will this standard enable the needed tightly integrated design systems to be built with leading edge components selected from multiple suppliers? Learn more about the Interoperability issues, progress and the future. Ask your questions to the experts in the System, Semiconductor and EDA Industries.

ORGANIZERS: Terry Blanchard - *Mgr. VLSI Technology Center, Hewlett-Packard Co.*
John Darringer - *Mgr. System-Design, IBM Research*
Greg Spirakis - *General Mgr. Design Technology, Intel Corp.*

REGISTRATION INSTRUCTIONS:

No Conference Registration is needed.

$40.00 ACM/IEEE Members
$60.00 Non-Members

SCHEDULE:

12:00 PM Lunch *(buffet served in room 285)*

1:00 PM Welcome: John Darringer - *Mgr. System-Design, IBM Research*

1:15 PM Session 1 - Customer View on Interoperability Progress and Future Chair: Terry Blanchard - *Mgr. VLSI Tech. Ctr., H-P Co.*
Dale Hoffman - *Dir. EDA, IBM Corp.*
Sumit Dasgupta - *Dir. SOC-IP Design Systems, Motorola, Inc.*
Jean-Pierre Geronomi - *Dir. CAD, ST Microelectronics*
Greg Spirakis - *GM. Design Technology, Intel Corp.*
Sudhakar Sabada - *VP Design Tech. Dev., LSI Logic Corp.*
Jan-Olof Kismalm - *Dir. Corporate Strategy, Ericsson*

2:15 PM Open Access Coalition Status - Scott Petersen - *Dir. Silicon Optimization, LSI Logic Corp.*

2:30 PM Session 2 - EDA Industry View of Interoperability Progress and Future Chair: Greg Spirakis - *Mgr. Design Technology, Intel Corp.*
Lavi Lev - *Sr. VP IC Solutions, Cadence Design Systems, Inc.*
Richard Goldman - *VP Strategic Market Dev., Synopsys, Inc.*
Moshe Gavrielov - *CEO, Verisity Design, Inc.*
Michael Sanie - *Dir. Marketing Dev., Numerical Technologies, Inc.*
Aki Fujimura - *President and COO, Simplex Solutions, Inc.*
Sang Wang - *CEO, Nassda Corp.*

3:30 PM Break

3:45 PM Panel: What is the Future of Interoperability? Chair: Richard Goering - *Editor, EE Times*
Panel members to be selected from workshop speakers.

5:00 PM Adjourn

Hands-On Tutorials

Hands-On Tutorials General Information

All Hands-On Tutorials take place in Room 293 or 294 of the Ernest N. Morial Convention Center.

Hands-on Tutorials are three-hour tutorials presented by exhibitors to demonstrate their solutions to issues related to "verifying embedded systems". This is an opportunity for attendees with a need to learn about or evaluate products in this area a chance to see, in an in-depth manner, a variety of solutions. Demonstrations are done with the attendees working from Sun workstations while the presenters lead the discussion. The tutorials are limited to the first 30 attendees with a student to workstation ratio of 2:1. (Due to the proprietary nature of the discussions, presenting companies have the right to refuse access to employees or contractors of competitors. The cost per tutorial is $40 and attendees are encouraged to enroll in more than one tutorial. Attendees must register for a minimum of an exhibits only registration in order to be eligible to enroll in a Hands-on Tutorial.)

1) Developing Bus-Functional Models for Embedded ATM Switch Verification

SynaptiCAD Inc. and Synopsys, Inc.

Monday 9:00 AM - 12:00 PM Room 293

SynaptiCAD and Synopsys will offer a hands-on tutorial where the attendees will construct an OpenVera test bench to verify an embedded ATM network switch using SynaptiCAD's graphical code generator TestBencher Pro and Synopsys's VERA test bench tool. Attendees will learn state of the art verification techniques, including modeling of data flow, random generation and ordering data cells and authentication of data that flows out of the device. The constructed test bench will also manage synchronization issues, avoid race conditions, and use algorithms and data structures that have traditionally only been needed for software verification. While the example used in this tutorial is an ATM switch, these techniques are beneficial for testing virtually all complex designs, particularly designs where hardware is replacing software functionality.

Attendees will use SynaptiCAD's TestBencher Pro to graphically describe transmit and receive transactions. TestBencher will generate OpenVera code directly from the graphical descriptions. Attendees will get a brief overview of OpenVera code. Next the attendees will compile the OpenVera test bench using the Synopsys VERA tool. Finally users will link the VERA run time object to the Verilog model of the ATM switch, simulate the design using Synopsys's VCS Verilog simulator, and analyze the simulation results.

Hands-On Tutorials

2) Creating and Using a Virtual Prototype for Embedded System Verification

AXYS Design Automation, Inc., Denali Software, Inc., Mentor Graphics Corp. and Verisity Design, Inc.

Monday 2:00 PM - 5:00 PM Room 293

Advances in EDA tools now make virtual prototyping a significant solution for embedded system verification. Today, the functional verification challenge is assembling a virtual prototype of the complete system with components from various companies. These virtual prototypes must exist at multiple levels of abstraction for high performance and accuracy, yet easily adjusted for verification requirements. This seminar demonstrates a virtual prototype system encompassing a range of tools and models from different vendors. The tools enable model creation, integration and verification of a complex multi-processor system. The focus is on tool interoperability and the verification methodologies to create a virtual prototype. The demonstration contains:

- A microprocessor subsystem based on the ARM PrimeXsys Wireless Platform, including the ARM926EJ-S core with instruction set simulation model
- AMBA bus protocol checking performed by Verisity's Invisible Specman
- A R.E.A.L. DSP model from Adelante Technologies, created using the MaxCore and MaxSim tools from AXYS Design Automation
- All memory components are modeled and simulated with Denali Software's MMAV product. The C models are integrated with Verisity's Specman and Mentor Graphics Seamless and ModelSim products. PureView is used for system data debugging\
- User-specific content initially modeled in a C-based language and later replaced by an RTL implementation

System verification tools used: Mentor Graphics' Seamless HW/SW co-verification, ModelSim digital simulator and XRAY software debugger; plus Verisity's Specman for testbench creation/protocol checking; Denali's MMAV for memory modeling/simulation; Pureview for system data debugging and AXYS' MaxSim for embedded SW simulation.

3) Assertion-Based Validation with Hardware/Software for Comprehensive Embedded System Verification

Co-Design Automation, Inc., Real Intent, ARM

Tuesday 2:00 PM - 5:00 PM Room 293

The growth in silicon real estate has increased the use of embedded processors such as the ARM core, and driven a rise in third-party IP applications and design reuse. The operation of third party IP within an embedded platform is notoriously error prone. The use of assertions to describe inter-block communication protocols, driven partly by software tests, is proving an effective method to mitigate the inherent issues resulting from multiple teams cooperating on the same design.

Having demonstrated how an IP assertion set can be created, this tutorial will leverage formal techniques to test the IP component using the assertions to effectively describe IP communication and functionality. It will then show how the same assertion set can be applied within a system simulation environment, where a processor core may drive the IP, checking it in situ within the platform using the same assertions. This will show how IP producer provided assertions may be leveraged by the IP consumer, breaking down intra team barriers.

This tutorial will be set up so that the user will get hands-on experience of writing and analyzing assertions across an embedded system. Users will learn to use formal verification in an embedded setting, software tests to drive a hardware platform simulation, and standard assertions across multiple tools and throughout the design flow.

Focus will be placed on Co-Design / Real Intent Superlog Assertions (CRSA), donated to Accellera for inclusion in the SystemVerilog standard. A standard ARM-based platform will be used with the ARM core operating an AMBA bus driving the IP.

Hands-On Tutorials

4) Hardware-Software Integration on the ARM Wireless PrimeXsys Platform using the CoWare N2C Design System

CoWare, Inc., ARM

Wednesday 9:00 AM - 12:00 PM Room 293

SoCs are becoming more complex with more functionality in software, multiple processors and complex bus architectures, all of which makes embedded systems integration and verification difficult to achieve with traditional methods.

In this tutorial, we will cover two very crucial aspects of embedded systems verification: choosing and verifying the optimal SoC architecture prior to implementation/prototype and verifying system integration and HW/SW interactions, paying particular attention to the simulation speed and debugging visibility for the hardware and embedded software. During this tutorial, the attendee will verify the Wireless PrimeXsys Platform based on the ARM926 microprocessor core, ARM PrimeCell® peripherals and multi-layer AHB bus. The CoWare N2C design system will be used to simulate, debug and analyze the ARM-based platform.

Participants should be familiar with SoC design in one or more of the following disciplines: system architecture, firmware development or hardware design. All tools run on the Solaris operating system.

5) Verification of Embedded Communication Systems

Cadence Design Systems, Inc., Xilinx, Inc., Synplicity, Inc.

Wednesday 2:00 PM - 5:00 PM Room 293

Growing complexity and accelerated design cycles demand closer collaboration among engineering disciplines to meet critical project deadlines. Using a communication case study, Cadence will guide you through the steps required to build a truly integrated hardware and software design environment. Students will learn how advanced methodology supported by efficient technologies can reduce development time and lower the risks of deliverables from different engineering disciplines not working together. Discussions and hands-on activities will include:

Starting with a baseband algorithm reference model, participants will explore parameter studies, reviewing BER simulation results and add blocks written in C, C++ or SystemC. In addition, they will learn how to debug a design and to accelerate simulation.

Evaluating the RF subsystem. TX and RX parameters will be examined to derive RF specifications. The results will be used to run Verilog AMS models with the baseband.

Writing firmware by replacing blocks in designs with a Digital Signal Processor model. This replacement will allow students to test the software within the complete system.

Targeting both ASICs and FPGAs, we will offer a mix of modeling techniques that covers: creating graphical blocks, writing VHDL & Verilog, and importing Xilinx CORE Gen DSP functions. Since all models can be verified with the system level testbench, engineers can select their favorite modeling technique.

Driving everything to implementation, using Synplify for FPGA synthesis and datapath synthesis for ASIC, the latter typically provides 15%-43% area reduction from traditional ASIC synthesis.

Hands-On Tutorials

6) Hardware and Software Debug Methods for a Programmable System

Xilinx, Inc., Wind River

Thursday 9:00 AM - 12:00 PM Room 294

Xilinx and Wind River Systems are providing a comprehensive software development tool chain that allows engineers to perform hardware bring-up and develop applications built directly in the Virtex-II Pro device. Xilinx is building upon this framework with ChipScope™ Pro CoreConnect Integrated Bus Analyzer, the industry's first embedded bus analyzer core. System bus access and visibility in a traditional embedded processor SoC design is difficult if not impossible to obtain. Access to system busses within the hardcore processor core requires the use of complex logic analysis equipment and the allocation of I/O dedicated to debug. Xilinx ChipScope Pro tools provide system bus access from within the device using embedded logic analysis cores. This access and visibility can greatly reduce processor bring-up and application debug time and occurs over the common JTAG port, minimizing the impact to the users overall system.

In this tutorial one can see real-world examples of hardware and software debug on a system evaluation board featuring the Xilinx Virtex-II Pro device. We will demonstrate embedded software debugging using advanced tools from Wind River Systems built specifically for the Virtex-II Pro device and will utilize ChipScope Pro CoreConnect bus analysis cores to view critical CoreConnect bus transactions between the embedded PowerPC 405 processor and user defined IP. This tutorial will help the user understand how Xilinx is providing a complete hardware software development solution that runs on the same host system over the same physical target connection to the JTAG port on the Virtex-II Pro device.

7) Top-Level Validation of Complex SoCs

Esterel Technologies

Thursday 2:00 PM - 5:00 PM Room 293

Complex SoC design requires new verification methodologies. Classical methodologies build verification plans from the high functional specifications, tests from the verification plan, and coverage measures by running the tests. There are several well-known problems with this method: Writing tests is laborious; Tests are sensitive to design change; Coverage is only measured with respect to the given verification plan and not with respect to the functionality of the design itself.

Esterel Technologies' new SoC Top Level Validation Solution is specifically designed to address these problems. It is applicable to modern multi-core designs, requires minimum knowledge of IP behavior, and is not severely affected by late RTL changes.

Participants will perform a top level validation for an MPEG design from beginning to end:

1) Simple models of a DMA and a DECODER will be designed at the transactional level (read, write, etc.).

2) Esterel Studio's automatic test generation will be applied to generate all meaningful concurrent transaction patterns between the SoC blocks to be tested.

3) Functional coverage will be measured with respect to the SoC functionality while various strategies will be compared to observe effect on test suites size.

4) Transaction patterns will be transformed into C test cases to be run on a C/C++ based validation platform, or into an HDL testbench.

5) Constraints will be added to generate tests for only parts of the design or to take into account SoC usage environment restrictions.

The results will be analyzed in terms of coverage, quality and productivity. Examples of actual industrial applications will also be discussed.

Additional Meetings

Birds-Of-a-Feather (BOF) Meetings

DAC provides conference rooms for informal groups to discuss items of common technical interest. These very informal non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather". All BOF meetings are held at the Hilton New Orleans Riverside, Wednesday, June 12, 2002, 6:00 PM - 7:30 PM. DAC will facilitate common interest group meetings to discuss DA related topics. To arrange a BOF meeting sign up at the Information Desk at-conference. A room will only be assigned if ten or more people sign up. An overhead projector and screen will be provided on request. Check DACnet and the Birds-of-a-Feather board at the Information Desk.

High Level Modeling for Validation (BOF)

The term "high level model" is highly overloaded; some of the intended uses of such an "HLM" include high level synthesis, a "live design model", or a performance model enhanced with functionality. The proposed topic adds another dimension; that of validation (i.e., "How do we use an HLM for better validation?").

METRICS for Design Productivity Measurement and Optimization (BOF)

METRICS encompasses the instrumentation of design tools and design processes, the collection of design artifact and design process data, and the prediction of future results and data based on current information. METRICS seeks to address the improvement of system design and implementation technology (e.g., flows and methodology) as science, rather than as art.

EDA Business Forum at DAC 2002

The annual EDA Business Forum™ at DAC is an exclusive event for financial and market analysts, technology and business editors, venture capitalists, and the CEOs and CFOs of member companies in the EDA Consortium. This year, the Forum panelists will discuss how to leverage new developments to increase the EDA industry's momentum. This invitation-only event will be held on Tuesday, June 11, from 12:00 noon - 1:50 PM in Room 271 at the Ernest N. Morial Convention Center in New Orleans. For more information, call (503) 643-7663 or visit www.akipr.com/edabf.

5th SIGDA Ph.D Forum

ACM/SIGDA will hold a semi-annual meeting on Tuesday evening, June 11, 2002, from 6:00 PM - 8:30 PM in Room 284. A light dinner will be served. The primary focus of the meeting will be the fifth annual SIGDA Ph.D. Forum. The meeting is open to all members of the DA community. The Ph.D. Forum, hosted by SIGDA, aims to strengthen the ties between academic research and industry. During the SIGDA meeting, students will use posters to discuss their Ph.D. thesis work with interested attendees. This session will provide the students an opportunity to receive feedback on their work. It also previews academic work-in-progress to the DA community. For more information about the Forum, please visit http://www.sigda.acm.org/Programs/PHDForum. SIGDA members and non-members are invited.

Additional Meetings

System-Level Design: Here & Now!

June 11, 2002, 12:00 PM - 2:00 PM, Rm: 393

Join us for a free lunch on Tuesday, June 11, to hear from a stimulating and informative panel of industry leaders who will present on the realities of system-level design employing SystemC. With its SystemC Modeling Platform, the Open SystemC Initiative (OSCI) provides an industry-defining solution to system-level design, Intellectual Property (IP) sharing and verification. While enjoying OSCI's complimentary lunch, you will hear a brief overview and update from OSCI, followed by 4 success stories from real-world users of SystemC. To register please send an email to: lunchatdac@systemc.org.

Accellera Membership Meeting

Wednesday, June 12, 2002, 10:00 AM - 11:00 AM, Rm: 257

Ernest N. Morial Conference Center. Presentation by Dennis Brophy, Chairman. There will also be a Accellera Technical Committee Roadmap, which will include committee updates about SystemVerilog, Formal Verification, ALF, Interfaces, Assertions, Rosetta and Verilog AMS.

VSIA Luncheon at the 39th DAC

June 12, 2002, 12:00 PM - 2:00 PM, Rm: 260

LUNCH IS ON US!! Please join the VSI Alliance for lunch on Wednesday. An exciting panel of experts will discuss where EDA tools fit in this new world of Hardware/Software SoC development. Join in the audience Q&A.

The VSI Alliance's current status and new efforts to develop specifications for software, as well as hardware, Virtual Component (VC) reuse will also be discussed.

Breakfast and Panel Discussion Sponsored by Accellera and Novilit

Wednesday, June 12, 2002, 7:30 AM, Hilton New Orleans Riverside, Marlborough Room

Plug and Play: HW/SW/firmware Flow for Successful SoC Design in 2002

Moderator: Ron Wilson - ISD

Today's design puzzle is fitting together. Large IP blocks, standard busses and software components from a number of vendors, on top of FPGAs, ASICs and custom ICs to meet the needs of a rapidly expanding and changing market place.

SpecC User Group Meeting

Thursday, June 13, 6:00 PM - 8:00 PM, Rm: 257

"SpecC technology" is the system design methodology with system-level design language SpecC. The industrial applications and academic research fields of SpecC technology are spreading over the design of embedded system, software and hardware includes SoC. This meeting focuses on to share the latest information about SpecC language specification (SpecC 2.0), available tools, application case studies and the activities of STOC (SpecC technology open consortium). This meeting is organized by Language WG and Case Study WG of STOC.

Student Design Contest

The purpose of the Student Design Contest is to promote excellence in the design of electronic systems by providing competition between graduate and undergraduate students at universities and colleges. This year we received submissions in two categories: "Conceptual" and "Operational". Operational designs are those which have been implemented and tested. Conceptual designs have not yet been fabricated and tested but must have been thoroughly simulated.
Students compete for cash prizes donated by a number of industrial sponsors IEEE/CAS, ACM/SIGDA and by DAC itself. Prizes will be awarded at a special luncheon during the conference. Prize winners have been invited to show their work at the University Booth on the show floor. In addition, two of the submissions have been included in this year's technical program (see pages 25 and 30).

DAC 2002 Student Design Contest Winners

Operational Category:

1st Place *Unlocking the Design Secrets of a 2.29 Gb/s Rijndael Processor (session 41.1)*
Patrick R. Schaumont, Ingrid M. Verbauwhede, Henry Kuo - *University of California, Los Angeles, CA*

2nd Place *System Design of iBadge for Smart Kindergarten*
Ivo Locher, Sung I. Park, Andreas Savvides - *Univ. of California, Los Angeles, CA*

3rd Place *A Low Noise Switched-Capacitor Interface Electronics for Sub-micro Gravity Resolution Micromachined Accelerometers*
Haluk Kulah - *Univ. of Michigan, Ann Arbor, MI*

Conceptual Category:

1st Place *A Microsystem for Near-Patient Accelerated Clotting Time Blood Tests*
Steven M. Martin, Roy H. Olsson, Richard B. Brown - *Univ. of Michigan, Ann Arbor, MI*

2nd Place *Design of a Crossbar Switch Chip for Use in a Demonstration System of an Optoelectronic Multi-Chip Module*
Jason D. Bakos, Donald M. Chiarulli - *Univ. of Pittsburgh, Pittsburgh, PA*

3rd Place (tie) *Highly Parallel DNA Sequence Matching and Alignment Processor*
A. T. Patzer - *Duke Univ., Durham, NC*

3rd Place (tie) *Low-Jitter Power-Aware Non-PLL Clock Generator for GHz Microprocessors*
Chulwoo Kim, Inchul Hwang - *Univ. of Illinois, Urbana, IL*
Sung Mo Kang - *Univ. of California, Santa Cruz, CA*

Honorable Mention:

A Low-Power Line Driver Using Resonant Charging With Reduced High-Order Frequency Components
Clemens Schlachta, Burkart Voss, Manfred Glesner - *Darmstadt Univ., Darmstadt, Germany*

Systematic Design of a 200 Ms/s 8-bit Interpolating/Averaging A/D Converter (session 29.4)
Jan Vandenbussche - *Katholieke Univ., Leuven, Belgium*

Power Minimization for Digital Optical Interconnects
Xiaoqing Wang, Fouad Kiamilev, Jeremy Ekman - *Univ. of Delaware, Newark, Delaware*

Awards

2002 Best Paper Awards

This year, awards are made for the best papers in three categories. Winners were determined from detailed reviews of the accepted papers in the technical sessions. Each award is accompanied by a plaque.

The awards are given by ACM/SIGDA (Special Interest Group on Design Automation), IEEE/CASS (Institute of Electrical and Electronics Engineers/Circuits and Systems Society) and EDA Consortium (Electronic Design Automation Consortium).

DESIGN TOOLS

Paper 4.3: *Guaranteed Passive Balancing Transformations for Model Order Reduction*

Author: **Joel R. Phillips**
Affiliation: Cadence Berkeley Labs., San Jose, CA

Author: **Luca Daniel**
Affiliation: Univ. of California, Berkeley, CA

Author: **Miguel Silveira**
Affiliation: INESC, Lisboa, Portugal

DESIGN METHODOLOGY

Paper 29.2: *Remembrance of Circuits Past: Macromodeling by Data Mining in Large Analog Design Spaces*

Authors: **Hongzhou Liu, Amit Singhee, Rob A. Rutenbar, L. Richard Carley**
Affiliation: Carnegie Mellon Univ., Pittsburgh, PA

EMBEDDED SYSTEMS

Paper 3.1: *A Universal Technique for Fast and Flexible Instruction-Set Architecture Simulation*

Authors: **Achim Nohl, Gunnar Braun, Andreas Hoffmann, Oliver Schliebusch, Rainer Leupers, Heinrich Meyr**
Affiliation: Aachen Univ. of Technology, Aachen, Germany

Awards

Marie R. Pistilli Women in EDA Achievement Award

• **Ann Rincon** - Senior Engineer, IBM Corp., Microelectronic Division, Burlington, VT

For her significant contributions in helping women advance in the field of DA technology.

2002 IEEE CASS Fellows

• **Georges G. E. Gielen** - Katholieke Univ., Leuven, Belgium

For contributions to computer-aided design and design automation of analog and mixed-signal integrated circuits and systems.

• **Sharad Malik** - Princeton Univ., Princeton, NJ

For contributions to electronic design automation techniques in logic and embedded software synthesis.

• **Lawrence T. Pileggi** - Carnegie Mellon Univ., Pittsburgh, PA

For contributions to simulation and modeling of integrated circuits.

• **Kaushik Roy** - Purdue Univ., West Lafayette, IN

For contributions to the power-aware design of digital circuits.

• **Ellen June Yoffa** - IBM Research, Yorktown Heights, NY

For technical, professional, and business leadership in electronic design automation.

CAD Transactions Best Paper Award

Floorplanning Using a Tree Representation, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, vol. 20, no. 2, pg. 281-289, February 2001.

Pei-Ning Guo - Mentor Graphics Corp., San Jose, CA
Toshihiko Takahashi - Niigata Univ., Niigata, Japan
Chung-Kuan Cheng - Univ. of California at San Diego, La Jolla, CA
Takeshi Yoshimura - NEC Corp., Kawasaki, Japan

The Association for Computing Machinery/Special Interest Group on Design Automation (ACM/SIGDA) Distinguished Service Awards

• **Cheng-Kok Koh** - *Purdue Univ., West Lafayette, IN*

For exemplary service to ACM/SIGDA and the EDA industry -- as Co-director of SIGDA's CDROM Project, as SIGDA's Travel Grants Coordinator, and as Editor of the SIGDA Newsletter.

• **Steven P. Levitan** - *Univ. of Pittsburgh, Pittsburgh, PA*

For over a decade of service to ACM/SIGDA and the EDA industry – as DAC University Booth Coordinator, Student Design Contest organizer, founder and promoter of SIGDA's web server, and most recently, Chair of ACM/SIGDA from 1997 to 2001.

ACM/SIGDA Outstanding New Faculty Award

• **Charlie Chung-Ping Chen** - *Univ. of Wisconsin, Madison, WI*

For a junior faculty member early in his academic career who demonstrates outstanding potential as an educator and researcher in the field of electronic design automation.

Awards

The P. O. Pistilli Scholarship for Advancement in Computer Science and Electrical Engineering Undergraduate Scholarships

The objective of the P. O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering and Computer Science from under-represented groups (women, African American, Hispanic, Native American, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship. SIGDA and MP Associates, Inc. annually administer the program for DAC. DAC normally funds two or more $4000 scholarships, renewable up to 5 years, to graduating high school seniors. In 1999 the IEEE Circuits and Systems Society also began to sponsor these scholarships.

The 2002 winners will be announced at the Conference. The 2001 winners were:

Tenisha Evonne Austin - attending the Univ. of Michigan in Ann Arbor
Sylvia Blythe Glassco - attending Yale Univ.
Joelle B. Arnold - attending Franklin W. Olin College of Engineering
Jieyu Hao - attending Massachusetts Institute of Tech.
Mariya Sergeyevna Sadakova - attending Macalester College
Todd R. Roman - attending the Univ. of Arizona
Erika Lin - attending Massachusetts Institute of Tech.

For more information about the P. O. Pistilli scholarship, please contact Dr. Cherrice Traver, EE/CS Dept., Union College, Schenectady, NY 12308, email: traverc@union.edu.

Design Automation Conference Graduate Scholarships

Each year the Design Automation Conference sponsors several $24,000 scholarships to support graduate research and study in Design Automation (DA), with emphasis in "design and test automation of electronic and computer systems". Each scholarship is awarded directly to a university for the Faculty Investigator to expend in direct support of one or more DA graduate students. The criteria for granting such a scholarship expanded in 1996 to include financial need. The criteria are: the academic credentials of the student(s); the quality and applicability of the proposed research; the impact of the award on the DA program at the institution; and financial need. Preference is given to institutions that are trying to establish new DA research programs.

Prof. **Florin Balasa**, Univ. of Illinois, Chicago, IL
Students: **Sarat Chandra Maruvada, Karthik Krishnamoorthy**
Novel Exploration Techniques in Device-Level Placement for Analog and Radio Frequency Blocks

Prof. **Dinesh K. Bhatia**, Univ. of Texas at Dallas, Richardson, TX
Students: **Shankar Balachandaran, Parivallal Kannan**
Congestion and Routability Estimation for Large ASICs

Prof. **Krishnendu Chakrabarty**, Duke Univ., Durham, NC
Student: **Lei Li**
Algorithms and Tools for Plug-and-Play System-on-a-Chip Test Automation

Prof. **Ingrid Verbauwhede**, Univ. of California, Los Angeles, CA
Student: **Patrick Schaumont**
Domain Specific Tools and Methods for Application in Security Processor Design

Information on next year's DAC scholarship award program will be available on the DAC web page at: http://www.dac.com.

40th DAC Call for Papers

40th DESIGN AUTOMATION CONFERENCE®

Anaheim Convention Center, Anaheim, CA • June 2-6, 2003

DAC is the premier conference devoted to Design Automation (DA) and the application of DA tools in designing electronic systems. Five types of submissions are invited: regular papers, special topic sessions, panels, tutorials, and design contest entries. Submissions should be submitted electronically to www.dac.com. Panel and Tutorial suggestions are due NO later than **November 4, 2002, 5:00 PM** MST; all others are due NO later than **December 6, 2002, 5:00 PM MST**.

Requirements for Submission

All DAC Submissions must be made electronically using PDF format NO later than **December 6, 2002, 5:00 PM MST**. Reference the DAC web page (www.dac.com) for instructions on electronic submissions. Please submit 1 PDF file:

1) The paper should contain an abstract of approximately 60 words clearly stating the significant contribution, impact and results of the submission. The paper should be formatted in double columns with a minimum 10pt. font, not to exceed 6-pages including all figures, tables and references (format templates are available on the DAC web site for your convenience, they are not required). Submissions exceeding the 6 page limit, fonts smaller than 10pt., or identifying the authors or their affiliation will be automatically rejected.

The following information will be needed when submitting your paper:

- Name, affiliation, and complete address for each author
- A designated contact person including his/her phone #, fax #, and email address
- A designated presenter, should the paper be accepted
- A list of topic numbers preceded by the letter T (Tools Track), M (Methods Track), or E (Embedded Systems Topic) ordered by relevancy, most clearly matching the content of the paper
- The following statement: "All appropriate organizational approvals for the publication of this paper have been obtained. If accepted, the author(s) will prepare the final manuscript in time for inclusion in the Conference Proceedings and will present the paper at the Conference".
- Authors of accepted papers must sign a copyright release form for their paper. Authors must also provide MP Associates a copy of their presentation materials and grant permission for the publication of the presentation and presentation materials on the DAC web site.

To permit a blind review, do not include name(s) or affiliation(s) of the author(s) on the manuscript, abstract or bibliographic citations. The papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage. Notice of acceptance will be emailed to the contact person by February 28, 2003.

Panels, Tutorials, Special Topic Sessions

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure submitted panel and tutorial suggestions, including participants. Panel and tutorial suggestions may be electronically submitted by **November 4, 2002.**

Special Topic Sessions may be either independent papers with a common theme or a set of closely related papers describing an overall system. In both cases, independent reviews of each paper and evaluation of the session as a whole will be used to select sessions. Suggestions for Special Topic Sessions should be submitted along with the list of papers to be included in the session and should describe the session's theme. These submissions must be electronically submitted **NO later than December 6, 2002 (5:00pm MST).**

University Design Contest

Students are invited to submit descriptions of original electronic designs, either circuit level or system level. Submissions should contain the title of the project, a 60-word abstract and a complete description of the design, not exceeding 4000 words. The submission should clarify the originality, distinguishing features, and measured performance of the design. Two categories of designs are eligible for awards, operational and conceptual. For operational designs, proof-of-implementation is required, while for conceptual designs, complete simulation is necessary. Designs must have taken place as part of the students' work at the university and must have been completed after June 2001. Submitted designs should not have received awards in other contests. Selected designs will be presented at the conference. These submissions must be electronically submitted NO LATER THAN **December 20, 2002 (5:00pm MST)**.

Topics of Interest

Authors are invited to submit original technical papers describing recent and novel research or engineering developments in all areas of design automation. Topics of interest include, but are not limited to the listing on the following page.

Design Tools Track

The Design Tools track (T) is devoted to contributions to the research and development of design tools and their supporting algorithms. Focus is on innovation of specific modeling, analysis and optimization techniques.

T0.1 Fundamental CAD Algorithms, e.g., BDDs, SAT, graph coloring, partitioning
T1.1 Electrical-level circuit and timing simulation
T1.2 Discrete simulation
T1.3 Static timing analysis and timing verification
T1.4 Power estimation
T2.1 Testing, fault modeling and simulation, TPG, test validation and DFT
T2.2 Transaction-level, RTL and gate-level modeling and validation: simulation, equivalence checking, functional formal (and semi-formal) verification.
T3.1 Floorplanning and placement
T3.2 Global and detailed routing
T3.3 Module generation and compaction, transistor sizing and cell library optimization, layout verification
T4.1 Technology-independent, combinational logic synthesis
T4.2 Technology-dependent logic synthesis, library mapping, cell-based-design, interactions between logic design and layout
T4.3 Sequential and asynchronous logic synthesis and optimization
T4.4 System, logic and physical synthesis techniques for reconfigurable computing
T4.5 High-level synthesis
T5.1 Interconnect and package modeling and extraction
T5.2 Signal integrity and reliability analysis
T5.3 Analog and mixed-signal design tools and RF
T5.4 Microsensor and microactuator design tools
T5.5 Statistical design and yield maximization
T6.1 IP protection and watermarking techniques for designs, tools, and algorithms
T6.2 Frameworks, intertool communication, WWW-based tools and databases

Design Methods Track

The Design Methods track (M) deals with innovative methodologies for the design of electronic circuits and systems, as well as creative experiences with design automation in state-of-the-art designs. Submissions for this track will be judged on how innovatively tools are combined into a new methodology that is effectively applied to real-world design problems. Papers focusing on algorithmic advances in modeling, analysis and optimization should be submitted to the Design Tools Track.

Design methodologies and case studies for specific design tasks

M1.1 Design entry and specification
M1.2 Electrical-level simulation and modeling
M1.3 Discrete simulation and modeling
M1.4 Static timing and performance analysis
M1.5 Functional design verification
M1.6 Testing, test generation and debugging
M1.7 Physical design, module generation, design for manufacturing
M1.8 Logic synthesis, including interaction with physical synthesis
M1.9 High-level and architectural synthesis

Design methodologies and case studies for specific application domains and platforms

M2.1 Overall design flows and methodologies for specific design applications
M2.2 Configurable computing, FPGAs and rapid prototyping
M2.3 Deep sub-micron: signal integrity, interconnect modeling and extraction
M2.4 High-performance design: timing, clocking and power distribution
M2.5 Low power design
M2.6 Analog, mixed signal, and RF design
M2.7 Process technology development, extraction, modeling and new devices
M2.8 MEMS, sensors, actuators

Integration and management of DA systems

M3.1 Management of DA systems, design interfaces, standards
M3.2 Distributed, networked, and collaborative design
M3.3 Intellectual property, design re-use and design libraries

Embedded Systems Topics:

Embedded Systems are characterized by mixed hardware and software components with limited processing, I/O and storage resources. The increasing role played by software components and their associated support introduces a host of new system design issues. To focus on these, the 40th DAC will have embedded systems sessions covering both the "tools" and the "methods" aspects of the following topics:

E1 Low-power design: compilation, scheduling and partitioning
E2 Embedded software: retargetable compilation, memory/cache optimization, real-time single-processor scheduling
E3 HW/SW co-design: specification, modeling, co-simulation and performance analysis, system-level scheduling and partitioning
E4 Hardware and software platform design: IP-based design, communication design, embedded HW
E5 Case studies

Sponsors

The 39th Design Automation Conference is sponsored by the ACM/SIGDA (Association for Computing Machinery/Special Interest Group on Design Automation), IEEE/CAS (Institute of Electrical and Electronics Engineers/Circuits and Systems Society), and the EDA Consortium (Electronic Design Automation Consortium). Membership information is at the ACM and IEEE booths. Join before registering and save.

IEEE Circuits and Systems Society

The IEEE Circuits and Systems (CAS) Society is one of the largest societies within IEEE and in the world devoted to the analysis, design, and applications of circuits, networks, and systems. It offers its members an extensive program of publications, meetings and technical and educational activities, encouraging an active exchange of information and ideas. The Society's peer reviewed publication activities include: Trans. on CAD; Trans. on CAS-Part I (Fundamentals); Trans. on CAS-Part II (Analog & Digital Signal Processing); Trans. on VLSI; Trans. on CAS for Video Technology; and the new Transactions on Multimedia which is co-sponsored with IEEE sister societies. CAS also sponsors or co-sponsors a number of international conferences, which include the Design Automation Conference (DAC), the Int'l Conference on Computer-Aided Design (ICCAD) and the Int'l Symposium on Circuits & Systems (ISCAS). A worldwide comprehensive program of advanced workshops including a new series on "Emerging Technologies in Circuits and Systems", as well as our continuing education short courses bring to our worldwide membership the latest developments in cutting-edge technologies of interest to industry and academia alike.

The IEEE/CAS Society has been serving its membership for over 50 years with such member benefits as:

- Discounts on all Society publications, conferences and workshops (including co-sponsored and sister society publications and conferences)
- The Society newsletter which includes short articles on emerging technologies, society news and current events
- Opportunities to network with peers and experts within our 12 focused committee meetings, the local events of over 60 chapters and more than 20 annual conferences/workshops
- Opportunity to read and review papers, write articles and participate in the Society's government
- And all the personal and professional benefits of IEEE membership

For more information, please contact the IEEE/CAS Society.

Mail: IEEE/CAS Society
15 W. Marne Ave.
PO Box 265
Beverly Shores, IN 46301-0265

E-mail: cas.info@ieee-cas.org
Phone: (219) 871-0210
Web: http://www.ieee-cas.org

Sponsors

Join ACM/SIGDA and Benefit Yourself and Your Profession

ACM/SIGDA, one of the three organizations that sponsor DAC, has a long history of supporting DAC and the EDA profession. In addition to sponsoring DAC, SIGDA sponsors ICCAD, DATE, and ASP-DAC, and many smaller symposia and workshops.

SIGDA has pioneered electronic publishing of EDA literature, beginning with the DA Library in 1989, which captured 25 years of EDA literature onto an archival series of CDROMs. In the early 1990s, SIGDA published the first EDA conference proceedings on CDROMs, and now produces CDROM proceedings for most of the major EDA conferences and symposia each year. SIGDA also produces an annual CDROM Compendium of those proceedings, and more recently, Multimedia Monographs based on talks at DAC and ICCAD. Finally, SIGDA provides strong support for the ACM journal TODAES (Transactions on Design Automation of Electronic Systems).

SIGDA provides a broad array of additional resources to our members, and to the EDA profession in general. SIGDA organizes and provides partial funding for the University Booth at DAC, and funds various scholarships and awards (including the ACM/SIGDA Outstanding New Faculty Award presented at DAC). More recently, SIGDA's DA Summer School and our Ph.D. Forum at DAC have provided invaluable opportunities for graduate students in EDA. SIGDA's latest resource made its debut recently -- the first version of SIGDA's Monthly Planner, which we hope will help you plan your EDA conference activities throughout the year. For further information on SIGDA's programs and resources, see http://www.sigda.org.

In addition, SIGDA members may also want to consider joining our parent organization, ACM. ACM membership provides access to a variety of ACM products and resources, including discounts on conferences, subscriptions to ACM journals and magazines, and the ACM Digital Library, an invaluable IT resource. For further details, see ACM's home page at http://www.acm.org.

As an EDA professional, isn't it time YOU joined SIGDA?

SIGDA/DAC University Booth

Each year SIGDA organizes the University Booth. The booth is an opportunity for university researchers to display their results and to interact with visitors from industry. Priority is given to presentations that complement the conference technical program. Demos that highlight benchmark results are also encouraged. The Design Contest winners will give demonstrations presenting their designs at the University Booth, Tuesday, 12:00 PM - 2:00 PM. The schedule of presentations will be published at the conference and will also be available on the SIGDA website. We thank the Design Automation Conference for its continued support of this project.

EDA Consortium

Formed in 1989 the EDA Consortium is an international association of companies engaged in the development, manufacture, and sale of design tools and services to the electronic engineering community. The Consortium enhances the EDA industry's efficiency and perceived value by:

- Leading forums to discuss industry issues
- Maintaining a centralized web site
- Sponsoring the DAC and DATE (Europe) conferences
- Reporting revenue data on the EDA market
- Recognizing excellence through:
  - Phil Kaufman Award
  - Design Achievement Awards
- Supporting emerging EDA companies

For more information, contact EDA Consortium, 111 W. Saint John St., Ste. 220, San Jose, CA 95113, Phone: (408) 287-3322, Fax: (408) 283-5283, E-mail: info@edac.org, Web site: www.edac.org.

Membership Includes these Benefits:

- Company listing and links on the Consortium web site
- Invitations to Consortium events
- Member discounts on:
  - DAC & DATE exhibit spaces
  - Market Statistics Service - the only source for quarterly EDA revenue data

Proceedings

ACM, the Association for Computing Machinery, is an international scientific and educational organization dedicated to advancing the arts, sciences, and applications of information technology. With a worldwide membership of 80,000, ACM functions as a locus for computing professionals and students working in the various fields of Information Technology.

ACM publishes and distributes books, magazines, and peer reviewed journals targeted to particular computing fields, as well as the monthly magazine, *Communications of the ACM*, the most cited publication in computing. In late 1997, ACM launched its Digital Library, an invaluable online resource of over 350,000+ fully searchable pages of text (including a 15+ year archive) from ACM's high quality journals and proceedings dating back to 1984.

ACM has 34 Special Interest Groups that focus on different computing disciplines. More than half of all ACM members join one or more of these Special Interest Groups. The SIGs publish newsletters and sponsor important conferences such as SIGGRAPH, OOPSLA, DAC, ICCAD and CHI, giving members opportunities to meet experts in their fields of interest and network with other knowledgeable members.

Become an ACM member today and join thousands of other leading professionals, researchers and academics who benefit from all ACM has to offer. Join ACM online at http://www.acm.org, or contact ACM directly by phone: (800) 342-6626 (U.S. and Canada) or (212) 626-0500 (outside U.S.), by fax: (212) 944-1318, or by e-mail: acmhelp@acm.org. Hours of operation are from 8:30 AM - 4:30 PM EST.

39th DAC Proceedings

The 39th DAC proceedings will contain 160 papers, panels, and special invited presentations. DAC is offering each conference and student registrant the proceedings in the CD-ROM edition (one hardbound edition will be available to registrants for $25.00 at the time of registration). Should you wish to purchase any additional copies, you may do so at the ACM booth for $50.00. After the conference, mail orders should be sent to ACM; approximate cost after conference is $70 for members, and $140 for non-members. ACM should be contacted before placing your order to determine cost and availability of the proceedings. The addresses are:

ACM Order Department
P.O. Box 11315
New York, NY 10286-1315

(800) 342-6626 (U.S. and Canada)
(212) 626-0500 (all other countries)

Fax: (212) 944-1318
e-mail: orders@acm.org

IEEE Order Department
P.O. Box 1331
445 Hoes Ln.
Piscataway, NJ 08855-1331

(800) 678-IEEE (U.S. and Canada)
(732) 981-1393 (all other countries)

Fax: (732) 981-9667
e-mail: customer.service@ieee.org

Technical Program Committee

Miron Abramovici
Agere Systems, Inc.
600 Mountain Ave., Rm. 2C-225
Murray Hill, NJ 07974-0636
(908) 582-3933
miron@agere.com

Charles J. Alpert
IBM Corp.
11400 Burnet Rd., MS 904-6G016
Austin, TX 78758
(512) 838-1045
alpert@austin.ibm.com

Luca Benini
DEIS Univ. di Bologna
viale risorgimento 2
Bologna, Italy 40136
(39) 051-202-3782
lbenini@deis.unibo.it

Jo Dale Carothers
The Univ. of Arizona, Dept. of ECE
Tucson, AZ 85721
(520) 621-8733
carothers@ece.arizona.edu

Mustafa Celik
Monterey Design Systems
894 Ross Dr., Ste. 100
Sunnyvale, CA 94089
(408) 548-4663
celik@mondes.com

Chaitali Chakrabarti
Arizona State Univ., Dept. of EE
Tempe, AZ 85287-5706
(480) 965-9516
chaitali@asu.edu

Kwang-Ting (Tim) Cheng
Univ. of California, Dept. of ECE
Santa Barbara, CA 93106
(805) 893-7294
timcheng@ece.ucsb.edu

Abhijit Dharchoudhury
Intel Corp.
1501 S. Mopac Expy., Ste. 400
Austin, TX 78746
(512) 314-0093
abhijit.dharchoudhury@intel.com

Marco Di Natale
Univ. of Pisa, Dept. of CE
Scuola Superiore S. Anna via
Carducci, 40
Pisa, Italy 56100
(39) 050-883-453
marco@ssup.it

Limor Fix
Intel Semiconductors Ltd.
MTM Ind. Ctr., PO Box 498
Haifa, Israel 31000
(972) 4-865-5256
limor.fix@intel.com

Masahiro Fujita
Univ. of Tokyo, Dept. of EE
7-3-1 Hongo, Bunkyo-Ku
Tokyo, Japan 113-8656
(81) 3-5841-6673
fujita@ee.t.u-tokyo.ac.jp

Georges G. E. Gielen
Katholieke Univ., ESAT-MICAS
Kasteelpark Arenberg 10
Leuven, Belgium B-3001
(32) 16-321-047
georges.gielen@esat.kuleuven.ac.be

Soha M. Hassoun
Tufts Univ., Dept. of EECS
161 College Ave.
Medford MA 2421
(617) 627-5177
soha@eecs.tufts.edu

Xiaobo (Sharon) Hu
Univ. of Notre Dame, Dept. of CSE
Notre Dame, IN 46556
(219) 631-6015
shu@cse.nd.edu

Ahmed A. Jerraya
TIMA Lab.
46, avenue Felix Viallet
Grenoble Cedex, France F-38031
(33) 476-574759
Ahmed.Jerraya@imag.fr

Seiji Kajihara
Kyushu Institute of Tech., Dept. ofCSE
680-4 Kawazu
Lizuka, Japan 820-8502
(81) 948-29-7665
kajihara@cse.kyutech.ac.jp

Timothy Kam
Intel Corp.
Strategic CAD Labs., JF4-211
5200 NE Elam Young Pkwy.
Hillsboro, OR 97124-6497
(503) 264-7536
tkam@ichips.intel.com

Kurt Keutzer
Univ. of California, Dept. of EECS
566 Cory Hall, #1770
Berkeley, CA 94720-1770
(510) 642-9267
keutzer@eecs.berkeley.edu

Krzysztof Kuchcinski
Lund Institute of Tech.
Dept. of CS, Box 118
Lund, Sweden 221 00
(46) 46-222-3414
krysztof.kuchcinski@cs.lth.se

Tadahiro Kuroda
Keio Univ., Dept. of EE
Hiyoshi 3-14-1, Kohoku-ku
Yokohama, Japan 223-8522
(81) 45-566-1534
kuroda@elec.keio.ac.jp

Technical Program Committee

Enrico Macii
Politecnico di Torino
Dip. Di Elettronica e Info.
Corso Duca degli Abruzzi 24
Torino, Italy 10129
(39) 011-564-7074
enrico@athena.polito.it

T.M. Mak
Intel Corp.
2200 Mission College Blvd.,
SC12-604
Santa Clara, CA 95052
(408) 765-4543
t.m.mak@intel.com

Malgorzata Marek-Sadowska
Univ. of California, Dept. of ECE
Santa Barbara, CA 93106
(805) 893-2721
mms@ece.ucsb.edu

Grant E. Martin
Cadence Design Systems, Inc.
555 River Oaks Pkwy.
San Jose, CA 95134
(510) 647-2804
gmartin@cadence.com

Yusuke Matsunaga
Kyushu Univ., Dept. of CS and CE
6-1 Kasuga Koen, Kasuga
Fujuoka, Japan 816-8580
(81) 92-583-7621
matsunaga@c.csce.kyushu-u.ac.jp

Kartikeya Mayaram
Oregon State Univ.,
Dept. of ECE, Owen 220
Corvallis, OR 97331
(541) 737-2972
karti@ece.orst.edu

Renu Mehra
Synopsys, Inc.
700 E Middlefield Rd.
Mountain View, CA 94043
(650) 584-1516
renu@synopsys.com

Noel Menezes
Intel Corp.
2111 NE 25th Ave., MS JFT-104
Hillsboro, OR 97124
(503) 264-8259
noel.menezes@Intel.com

Shin-ichi Minato
NTT Network Innovation Labs.
1-1 Hikarinooka
Yokosuka-shi, Japan 239-0847
(81) 468-59-3021
minato@ieee.org

Steven M. Nowick
Columbia Univ., Dept. of CS
New York, NY 10027
(212) 939-7000
nowick@cs.columbia.edu

Ralph Otten
Delft Univ. of Tech.
ITS/ENS, Mekelweg 4
Delft, The Netherlands CD2628
(31) 15-278-1600
otten@akebono.ics.ele.tue.nl

Joel R. Phillips
Cadence Berkeley Labs.
555 River Oaks Pkwy., MS 1A1
San Jose, CA 95134
(408) 944-7983
jrp@cadence.com

Carl Pixley
Synopsys, Inc.
19500 NW Gibbs Dr.
Beaverton, OR 97006
(503) 748-2405
cpixley@synopsys.com

Miodrag Potkonjak
Univ. of California, Dept. of CS
3532G Boelter Hall
Los Angeles, CA 90095-1596
(310) 825-0790
miodrag@cs.ucla.edu

Anand Raghunathan
NEC Corp.
C & C Research Lab.
4 Independence Way
Princeton, NJ 08540
(609) 951-2967
anand@nec-lab.com

Annette Reutter
Robert Bosch BmbH
Dept. of AE/DIC, PO Box 1342
Reutlingen, Germany 72703
(49) 0-7121-35-2217
Annette.Reutter@de.bosch.com

Kaushik Roy
Purdue Univ., 1285 EE Bldg.
West Lafayette, IN 47907
(765) 494-2361
kaushik@ecn.purdue.edu

Jaijeet Roychowdhury
Univ. of Minnesota, Dept. of ECE
200 Union St. SE, Rm. 4-155
Minneapolis, MN 55455
(612) 626-7203
jaijeet@ece.umn.edu

Karem A. Sakallah
Univ. of Michigan
1301 Beal Ave.
Ann Arbor, MI 48109-2122
(734) 936-1350
karem@umich.edu

Majid Sarrafzadeh
Univ. of California, Dept. of CS
3532C Boelter Hall
Los Angeles, CA 90095-1596
(310) 794-4303
majid@cs.ucla.edu

Technical Program Committee

TECHNICAL PROGRAM COMMITTEE

Louis Scheffer
Cadence Design Systems, Inc.
555 River Oaks Pkwy., MS 2B2
San Jose, CA 95134
(408) 944-7114
lou@cadence.com

Donatella Sciuto
Politecnico di Milano
Dip. Di Elettronica e Info.
P.zza L. da Vinci 32
Milano, Italy 20133
(39) 02-2399-3662
sciuto@elet.polimi.it

Narendra V. Shenoy
Synopsys, Inc.
131/82/2C 3rd A Cross
18th Main, 6th Block,
Koramangala
Bangalore, India 560095
(91) 80-552-2201
nshenoy@synopsys.com

Steven Teig
Simplex Solutions, Inc.
521 Almanor Ave.
Sunnyvale, CA 94085
(408) 617-6129
steve@simplex.com

Ingrid Verbauwhede
Univ. of California, Dept. of EE
Box 951594, 7440B Boelter Hall
Los Angeles, CA 90095-1594
(310) 794-5209
ingrid@ampere.ee.ucla.edu

Diederik Verkest
IMEC, DESICS Div.
Kapeldreef 75
Leuven, Belgium B-3001
(32) 16-281-594
verkest@imec.be

Kees A. Vissers
TriMedia Technologies, Inc.
1840 McCarthy Blvd.
Milpitas, CA 95035
(408) 739-7647
kees.vissers@trimedia.com

Chandu Visweswariah
IBM TJ Watson Research Ctr.
Rte. 134 and Taconic
Yorktown Heights, NY 10598
(914) 945-3124
chandu@watson.ibm.com

Sarma Vrudhula
Univ. of Arizona, Dept. of ECE
1230 E. Speedway Blvd., ECE Bldg.
Tucson, AZ 85721
(520) 621-3291
sarma@ece.arizona.edu

PANEL SUBCOMMITTEE

Dennis Brophy
Model Technology, Inc.
10450 SW Nimbus Ave., Bldg. R-B
Portland, OR 97223-4347
(503) 526-1694
dennisb@model.com

Deirdre Hanford
Synopsys, Inc.
700 E. Middlefield Rd.
Mountain View, CA 94043-4033
(650) 584-4201
ryan@synopsys.com

Andrew B. Kahng
Univ. of California at San Diego
Dept. of CSE, MC-C-014
La Jolla, CA 92093-0114
(858) 822-4884
abk@cs.ucsd.edu

Tokinori Kozawa
STARC
Onariman BN Bldg.
6 chome 16-10, Shimbashi
Minatoku, 105-0004, Japan
(81) 33-436-1250
kozawa@starc.or.jp

Philippe Magarshack
STMicroelectronics, CRD Grp. VP
850 rue Jean Monnet
Crolles Cedex, France 38926
(33) 4-769-26498
philippe.magarshack@st.com

Shishpal S. Rawat
Intel Corp.
MS FM5-108
Folsom, CA 95630
(916) 356-6639
shishpal.s.rawat@intel.com

Rob A. Rutenbar
Carnegie Mellon Univ.
2118 Hammerschlag Hall
5000 Forbes Ave.
Pittsburgh, PA 15213-3890
(412) 268-3334
rutenbar@ece.cmu.edu

Student Design Contest Judges / Exhibitor Liaison Committee

STUDENT DESIGN CONTEST JUDGES

Robert C. Frye
Agere Systems, Inc.
600 Mountain Ave.,
Rm: 2T-204
Murray Hill, NJ 07974
(908) 582-5353
rcf@agere.com

Shane Bell
Intel Corp.
334 South St.
SHR1-1/S30
Shrewsbury, MA 01545
(508) 841-1613
shane.bell@intel.com

Jim Goodman
Lumic Electronics Inc.
18 Antares Dr., Ste. 200
Ottawa, ON, Canada K2E 1A9
(613) 224-9926
jimg@lumictech.com

Ivan Kourtev
Univ. of Pittsburgh
Dept. of EE
336 Benedum Hall
Pittsburgh, PA 15261
(412) 624-9088
ivan@ee.pitt.edu

Steve Maciejewski
Advanced Micro Devices
One AMD Pl.
PO Box 3453, MS 363
Sunnyvale, CA 94088-3453
(408) 774-7763
stevenj.maciejewski@amd.com

H. Alan Mantooth
Univ. of Arkansas
Dept. of EE
Bell Engr. Ctr. 3217
Fayetteville, AR 72701
(479) 575-4838
mantooth@engr.uark.edu

Grant Martin
Cadence Design Systems, Inc.
2001 Addison St., 3rd Fl.
Berkeley, CA 94704
(510) 647-2804
gmartin@cadence.com

EXHIBITOR LIAISON COMMITTEE

Bryan Ackland
General Chair, 39th DAC
Agere Systems, Inc.
101 Crawfords Corner Rd.
Rm. 4E-508
Holmdel, NJ 07733-1900
(732) 949-7248
bda@agere.com

Nanette Collins
Publicity Chair, 39th DAC
37 Symphony Rd., Unit A
Boston, MA 02115
(617) 437-1822
nanette@nvc.com

Sue Drouin
Mentor Graphics Corp.
8005 SW Boeckman Rd.
Wilsonville, OR 97070-7777
(503) 685-1183
sue_drouin@mentorg.com

Larry Eberle
EDA Consortium
Representative, 39th DAC
Synopsys, Inc.
700 E. Middlefield Rd.
Mountain View, CA 94043-4033
(650) 584-4418
leberle@synopsys.com

William H. Joyner, Jr.
EDA Industry Chair, 39th DAC
Semiconductor Research Corp.
PO Box 12053
Research Triangle Park,
NC 27709
(919) 941-9472
joyner@src.org

Peter Kalenak
Numerical Technologies, Inc.
70 W. Plumeria Dr.
San Jose, CA 95110
(408) 273-4316
pkalenak@numeritech.com

Darby Mason-Merchant
Xilinx, Inc.
2100 Logic Dr.
San Jose, CA 95124
(408) 879-5228
darby@xilinx.com

Mark Miller
Tera Systems, Inc.
2105 S. Bascom Ave.,
Ste. 135
Campbell, CA 95008
(408) 879-1990
mmiller@terasystems.com

Steve Pollock
Real Intent
3910 Freedom Cir.,
Ste. 102A
Santa Clara, CA 95054
(408) 982-5412
pollock@realintent.com

Richard Porter
Innoveda, Inc.
293 Boston Post Rd.
W. Marlboro, MA 01753
(508) 303-5434
rporter@innoveda.com

Gary Smith
Dataquest
251 River Oak Pkwy.
San Jose, CA 95134
(408) 468-8271
gary.smith@dataquest.com

Lee Wood
Exhibit Manager, 39th DAC
MP Associates, Inc.
5305 Spine Rd., Ste. A
Boulder, CO 80301
(303) 530-4562
lee@mpassociates.com