About the Conference

DAC 2003 is the 40th Design Automation Conference. To commemorate this, DAC will emphasize the traditional activities that have made it invigorating and enlightening in the past, and introduce new ones to make it even more so.

The major theme of this year's conference is Minimizing Power Consumption in Design.

For those new to DAC, it is the pre-eminent and unique forum that brings designers and the electronic design automation (EDA) community together. It provides a forum for technology interchange among a vast and diverse community -- EDA researchers and developers; engineers and managers who use EDA tools and systems to design, test and manufacture circuits and systems; vendors who provide EDA and embedded systems and silicon; and industry observers that include the press, financial, and market analysts who follow semiconductor and EDA businesses.

As usual, DAC offers a full and exciting Technical Program, Exhibition, Panels, Tutorials, Workshops, Meetings and Social Events, all designed to encourage learning and interaction.

We kick-off this year's Technical Program with Tuesday's keynote speaker -- Sir Robin Saxby, Chairman of ARM Holdings plc who will look into the future and identify challenges that we face. Thursday's keynote speaker, Professor Alberto L. Sangiovanni-Vincentelli, will examine EDA over the last 40 years to mine patterns and major events that shaped our business in the past and use this to predict the future.

The Technical Program had the highest-ever number of submissions and it promises to be one of the best ever. It has two major tracks -- Design Tools (new EDA techniques) and Design Methods (design methodologies). Embedded Systems, the convergence of hardware and software design methodologies and tools, continues to be a major emphasis. New this year: Five "Best of ISSCC Papers". Technical program attendees will receive a DVD containing all DAC proceedings for the past 40 years.

Once again, the exhibit floor will come alive with new and exciting developments in EDA, embedded systems and silicon from more than 190 exhibitors including over 15 first timers.

The conference will continue Hands-on Tutorials which emphasize Power and Signal Integrity this year, a Monday tutorial on Power Issues, the Monday Introduction to EDA for non-technical people and the popular DAC Pavilion on the exhibit floor. Nowhere are advances and breakthroughs more pronounced than during DAC. For anyone in electronics design today, it's an event not to be missed. We look forward to seeing you.

Co-Located Conferences	The 40th Design Automation Conference Week in Review				
	Monday, June 2	**Tuesday, June 3**	**Wednesday, June 4**	**Thursday, June 5**	**Friday, June 6**
• **IWLS** * May 28-30 *Surf and Sand Resort* *Laguna Beach, CA* • **MSE** * June 1-2 *Anaheim Marriott* *Anaheim, CA*	• Full Day Tutorial • Hands-on Tutorials • Workshops • Exhibits • Demo Suites	• Opening Session • Keynote Address • Technical Sessions • Hands-on Tutorial • Exhibits • Demo Suites	• Technical Sessions • Hands-on Tutorials • Exhibits • Demo Suites • DAC Party	• Keynote Address • Technical Sessions • Hands-on Tutorials • Demo Suites • Best Paper Awards	• Full Day Tutorials

New @ DAC

40th Design Automation Conference

Highlights of ISSCC

Attend sessions 40 & 41 for the special presentation of selected International Solid State Circuits Conference papers highlighting a variety of leading edge chip designs. DAC is partnering with ISSCC, known for presentation of the leading circuit design papers, to present the "Highlights of ISSCC." Take advantage of these sessions for a unique look at the design challenges of high-performance systems and circuits. Learn about design tools, flows and methodologies used today to meet these challenges.

Management Focus Day at DAC

Tuesday, June 3, 2003

DAC is proud to introduce a new program at DAC for managers and executives! Working in partnership with the Fabless Semiconductor Association (FSA), the Management Focus Day is a program specifically designed to address business issues for executives of semiconductor and fabless companies. Among the topics presented and discussed at the Management Focus Day will be IP business models, strategies for fab partnerships, EDA tool licensing models, and more. Attendees will participate in two exclusive sessions and the EDA Business Forum luncheon. In addition, registration includes the Keynote Address by Sir Robin Saxby and access to the exhibit floor. [The intended audience is manager/director/up level executives who want to learn about best practices in their industry.]

DAC Exhibit Floor Microbrew Party

Monday, June 2, 2003 • 4:00 PM - 6:00 PM

Just when you thought Free Monday at DAC couldn't get any better - it does! Be sure to visit the exhibit floor between 4:00 PM and 6:00 PM on Monday, June 2, as exhibitors host the Microbrew Party from their booths. Look for several varieties of local microbrewed beers and soft drinks along with munchies. This informal gathering is the ideal opportunity to meet vendors and enjoy some well-deserved refreshments.

Ice Cream Social

Tuesday, June 3, 2003 • 2:00 PM - 4:00 PM

Another new service at DAC this year is the Tuesday afternoon ice cream social on the exhibit floor. Look for the carts at selected locations on the exhibit floor Tuesday from 2:00 PM - 4:00 PM. For a cold creamy treat.

Awards

P.O. Pistilli Scholarships (ACSEE)

Scholarships will be awarded to two high school students of under-represented minorities who will be pursuing a degree in Electrical Engineering or Computer Science.

Marie R. Pistilli Women in EDA Achievement Award

The fourth annual award will be presented to a recipient who has made significant contributions in helping women advance in the field of DA technology.

Student Design Contest Awards

The purpose of the Student Design Contest is to promote excellence in the design of electronic systems by providing competition between graduate and undergraduate students at universities and colleges. Prize winners will be listed in the final program and have been invited to show their work at the University Booth on the show floor. Awards will be given at the Pavilion, on Tuesday, June 3, 2003 from 11:30 AM - 12:00 PM.

Best Paper Awards

Best Paper Awards of $1000 each will be announced at the Thursday Keynote. Papers eligible for awards in this category are nominated by the Program Committee and selected by a referee process.

Phil Kaufman Award

The award honors an individual who has contributed to creating or driving technology advances that have had measurable impact on the productivity of design engineers. The 2002 recipient:

Ronald Roher - *Magma Design Automation, Cupertino, CA*
- Neolinear Inc., Pittsburgh, PA

IEEE Emmanuel Priore Award

Giovanni DeMicheli - *Stanford Univ., Stanford, CA*

2003 IEEE Fellows

John Maxwell Cohn - *IBM Microelectronics, Essex Junction, VT*
For contributions to the development of CAD tools and design methodology for high-performance custom integrated circuits.

Andreas Kuehlmann - *Cadence Berkeley Labs., Berkeley, CA*
For the development of formal equivalence checking technology and its successful application to microprocessor and ASIC designs.

Sachin Suresh Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*
For contributions to the optimization of timing and layout in VLSI circuits.

Program Highlights

Technical Program - details on pgs. 14 - 35

The technical program includes over 177 papers, panels and special sessions in five parallel tracks covering system level design, synthesis, physical design, verification, interconnect, power and AMS issues. Highlights include a focus on power and signal integrity and embedded systems (see right) as well as a number of special sessions with invited paper presentations.

TUESDAY KEYNOTE
Sir Robin Saxby
Chairman
ARM Holdings plc, Cambridge, UK
Tuesday, June 3 - 8:30 AM
Room: Ballroom A-C

THURSDAY KEYNOTE
Alberto L. Sangiovanni-Vincentelli
Professor
Univ. of California, Berkeley, CA
Thursday, June 5 - 1:00 PM
Room: Ballroom A-C

SIGDA Ph.D. Forum - details on pg. 45

Tuesday, June 2, 2003 • 6:30 PM - 9:00 PM Rm. 213A-C

A chance for Ph.D. students and industry representatives to get together. Students get feedback on their research proposals; industry gets a chance to meet students and preview their work.

Hands-on Tutorials - details on pgs. 60 - 63

Hands-on Tutorials are three-hour tutorials presented by exhibitors to demonstrate their solutions to issues related to "signal and power integrity, analysis and methodology".

Power - Sessions: 2, 8, 9, 11, 36, 52

Over 22 papers, panel, tutorial and hands-on tutorials will cover topics such as reshaping EDA for power, power estimation, power grid analysis, variable voltage scaling, leakage power and low energy system design.

Embedded Systems - Sessions: 5, 6, 9, 15, 19, 25, 28, 45, 50

Over 35 papers and panels will cover topics such as low-power embedded system design, design space and architectural exploration, performance modeling, compilation, memory optimization and wireless for embedded software.

Tutorials - details on pgs. 36 - 38

Monday, June 2, 2003 • 9:00 AM - 5:00 PM

1) Design Techniques for Power Reduction

Friday, June 6, 2003 • 9:00 AM - 5:00 PM

2) System-on-Chip Test Strategies
3) Design for Manufacturing in the Sub-100nm Era
4) Assertion-Based Verification
5) Assembling an SoC: Communication Architectures and Protocols
6) High-Performance ASIC Design

Exhibit Highlights

Exhibit Floor

Monday - Wednesday, June 2-4, 2003 10:00 AM - 6:00 PM

Over 190 EDA, Silicon, IP and Embedded Systems companies participate in the DAC exhibition and demo suites. All exhibits and demo suites are located in Halls A-D of the Anaheim Convention Center.

The Embedded Systems Showcase offers exhibitors and attendees a highly focused area to display and view tools for the design of embedded systems-on-chip.

Exhibitor Listing .....Pages 46 - 47
Exhibiting Company Descriptions.....Pages 48 - 58
Hands-on Tutorials .....Pages 60 - 63

Demo Suites

Monday - Wednesday, June 2-4, 2003 .....8:00 AM - 9:00 PM
Thursday, June 5, 2003 .....8:00 AM - 5:00 PM

- Demo Suites will be in Halls A & D of the Anaheim Convention Center.
- Exhibiting companies offer their customers private product demos within the Convention Center.
- Demo Suites are available by invitation only.

Children under the age of 14 will NOT be allowed in the exhibit hall or demo suite area.

Exhibit-Only Registration

- **Free Monday Exhibit-Only Passes** - Attend the exhibition free of charge Monday, June 2.
- $50 Exhibit-Only registration will allow you to attend exhibits Monday through Wednesday.
- Call **(800) 321-4573**, or register on-line at **www.dac.com.**

DAC Pavilion

The Pavilion, located in booth #1372, offers live panel discussions with industry experts, broadcasts of selected technical sessions and a lounge area to relax. Join us as we bring DAC's world-class technical program to the exhibit floor! **See pages 8-9 for details.**

New Exhibitors at DAC

DAC has always been the best place to see the industry's newest companies, and this year is no exception. With over 20 new exhibitors this year, DAC is the place to be to find out what the hot start-ups are up to. Among the companies participating in DAC for the first time are:

Anadigm, Inc.
Apache Design Solutions, Inc.
Arrow's Global Information Business
DINI Group (The)
ELANIX, Inc.
FEI Co.
ObjectStore, a division of Progress Software
Optimal Corp.
Paragon IC Solutions, Inc.
PDF Solutions, Inc.
ProDesign Electronic & CAD Layout
SOISIC
SynAPPS Software Corp.
TDA Systems, Inc.
Tenison EDA
TriCN
True Circuits, Inc.
Voom, Inc.
X Initiative

Tuesday Keynote <100nm...A Giant Leap for Mankind?

Sir Robin Saxby
Chairman
ARM Holdings plc, Cambridge, UK
Tuesday, June 3, 2003, 8:30 AM - 10:00 AM
Room: Ballroom A-C

Moore's Law is predicted to continue its relentless pace for the next 15 or so years. By a series of small steps we have 100Mtr of ASIC capacity available today, and will have more than 1 billion within the next five years. The product opportunities presented by this opportunity will change our lives ... However with every new opportunity come some new challenges. Rapidly escalating mask charges and wafer fabrication costs will cause the shape of the semiconductor industry to change. The shake down of lead players focused on wafer foundry and others focused on IP building blocks will continue. The approach to total system design will need to change with verification and validation becoming the biggest bottlenecks.
Design, long considered as a negligible amortized cost, has started to compete with fabrication costs! But whilst fabrication costs are rising as a square law, design costs are rising with at least a cubic law! For an industry where FAB costs have dominated, this shift of emphasis over the next few years will shake the foundations of our entire industry. What giant leap is required, how will the global landscape alter, what are the emerging applications and can we take advantage of all those available transistors?

Biography: Sir Robin Saxby was involved in the founding of ARM and served as Chairman, President and Chief Executive Officer since joining the company full-time in February 1991. In October 2001, he split the role of chairman and chief executive officer, becoming Executive Chairman while Warren East took on the role of Chief Executive Officer. Besides directing ARM, Robin was also appointed to the board of Glotel plc as a non-executive director in April 1999. Prior to this, he worked for five years for European Silicon Structures SA (ES2), where he was Vice-President of Northern Europe, Managing Director ES2 Limited and President of its USA affiliate US2. Between 1984 and 1986, Robin was Chief Executive Officer of Henderson Security Systems Limited and before that, spent eleven years with Motorola Semiconductors in a variety of sales, marketing and engineering management roles. His early career was in design and development with Rank Bush Murphy and PyeTMC. Robin also served as Chairman of the Open Microprocessor Initiative Advisory Group, a European Union panel set up to advise on collaborative R&D activity in Europe. In 2000, Robin was awarded an honorary Doctorate D.Eng from Liverpool University. He was also appointed a visiting professor to his old Department of Electronics at the University. In July 2001, he was awarded an honorary Doctorate D.Tech from Loughborough University. He was awarded a Knighthood in the 2002 New Year Honours for services to the Information Technology industry.

Thursday Keynote The Tides of EDA

Alberto L. Sangiovanni-Vincentelli
Professor
Univ. of California, Berkeley, CA
Thursday, June 5, 2003, 1:00 PM - 1:45 PM
Room: Ballroom A-C

Giovan Battista Vico, a philosopher and historian who lived across the XVII and XVIII centuries, was the first to note in his masterpiece "Scienza Nuova" (New Science) that the history of man and his endeavors follow a cyclical pattern. Economies, as well as the power of nations, have exhibited a clear and cyclical behavior and EDA has not escaped this fundamental law. EDA technology advances have oscillated between verification and synthesis, the perc e ption in the mind of the electronic design community of EDA has been rising and falling in a regular pattern, EDA companies have risen and declined, the consideration of the financial community for EDA has been periodically increasing and decreasing, and the algorithms used in EDA have swung from general purpose techniques borrowed from mathematics, computer science, operation research, and artificial intelligence, to ad hoc techniques that leverage the nature of the specific design problem to be solved. Yet, valuable sediment has been deposited by these tides over the years. I will show that progress is achieved when new methodologies crystallize, with new tools and techniques acting as catalysts, that the construction of layers of abstraction are the steps that have helped us reach new heights, that the progress of EDA technology has slowed down just when complexity has reached levels never seen before. I will argue that the designer community must leave its traditional shores, under attack by the swarm of killer transistors, and sail towards a new world where transistors have been tamed. The EDA and the design communities must plan and build together the sturdy ships needed to traverse these stormy seas. The risks of this expedition must be born in equal parts by these two communities if we wish to reach the land of opportunity that technology unveils. The lack of systematic collaboration within the EDA community, and among the EDA community and its various customers, poses a serious threat to the recovery of the electronic industry. We cannot let this happen!

Biography: Alberto Sangiovanni Vincentelli is Professor of Electrical Engineering and Computer Sciences at the University of California at Berkeley where he has been on the faculty since 1976. He is a co-founder of Cadence and Synopsys, the two leading companies in the area of Electronic Design Automation. He is the Chief Technology Advisor of Cadence and sits on the Board of Directors of Cadence. He also sits on the boards of Sonics, Accent and Softface. He is a member of the HP Strategic Technology Advisory Board. He has consulted for a number of companies including IBM, Intel, ATT, GTE, GE, Harris, Nynex, DEC, HP, Kawasaki Steel, Fujitsu, Sony, Hitachi, ST, Alcatel, BMW, Daimler-Chrysler, Magneti-Marelli, Bull. He is the Scientific Director of PARADES, a European Group of Economic Interest funded in 1996 by Cadence, Magneti-Marelli, and ST.

In 1981 he received the Distinguished Teaching Award of the University of California and in 1995 the worldwide Graduate Teaching Award of the IEEE (a Technical Field award for "inspirational teaching of graduate students"). He has received three Best Paper Awards (1982, 1983 and 1990) and a Best Presentation Award (1982) at the Design Automation Conference, three best paper awards from the International VLSI conference, and is the co-recipient of the Guillemin-Cauer Award (1982-1983), the Darlington Award (1987-1988), and the Best Paper Award of the Circuits and Systems Society of the IEEE (1989-1990). He was the recipient of the 2001 EDA Kaufman Award and of the 2002 Aristotle Award of the SRC. He is the author of over 600 papers and fifteen books in the area of design methodologies and tools.

Dr. Sangiovanni-Vincentelli has been a fellow of the Institute of Electrical and Electronics Engineers since 1982 and a Member of the National Academy of Engineering.

DAC Pavilion - Booth #1372

DAC brings its technical program to the exhibit floor through live panel discussions and broadcasts of highlighted technical sessions in the DAC Pavilion. DAC attendees and exhibitors are invited to visit the DAC Pavilion to participate in these engaging technical presentations or take a few minutes to relax in our lounge.

Monday, 10:30 AM - 11:30 AM

Managing Mask Costs

Moderator: Joe Sawicki - *Mentor Graphics Corp.*
Panelists: Mojy Chian - *Mindspeed Tech., A Conexant Business*
Tim Daniels - *LSI Logic Europe*

The cost of mask sets continues to increase with each process node. Can ASIC design sustain the projected cost of mask sets and continue to operate a business as usual? If mask costs are a concern, what are users and the semiconductor industry doing to address this issue? From the customer point of view, the issue may not just be the cost of a mask set: rather, design today is a $20M proposition that needs to be managed. In this context, mask costs are just one aspect of design costs, and looking only at this one aspect may not be sufficient to control costs. At the same time, specific mask set cost reduction techniques can be applied as part of an overall approach to design cost management. From the semiconductor supplier point of view, certainly mask cost issues impact the traditional ASIC model, and are being addressed. Specific examples will be given of alternative design methods that are being deployed by the semiconductor industry to eliminate this cost.

Monday, 12:00 PM - 1:00 PM

Semiconductor IP Business - Is It Real?

Moderator: Rick Nordin - *Silicon Design Systems*
Panelists: R. Vijayaraghavan - *Comit Systems, Inc.*
Dan Ganousis - *AccelChip, Inc.*

Independent semiconductor IP vendors have been facing varying degrees of success in the marketplace and in the majority of cases (i.e. non-specific IP core vendors) are struggling just to get by. Given the widespread recognition that IP is the only solution for staying on Moore's Law and consumer expectation curves, why then is the IP industry in such a dilemma? Some observers even question whether IP vendors are following a flawed business model. The panelists will discuss the fine points of why the broad IP market has not met its forecasted success and likelihood of how it will evolve in the future.

Monday, 1:00 PM - 2:00 PM

Ask the CTO

Moderator: Philippe Magarshack - *STMicroelectronics*
Panelists: Raul Camposano - *Synopsys, Inc.*
Ted Vucurevich - *Cadence Design Systems, Inc.*

This Pavilion panel gives an informal setting in which the audience can ask two major EDA company CTOs about their vision and key directions for future technology. This panel is expected to be a friendly and open forum, with many deep questions about innovation, upcoming technologies, technology roadmap, and other "Ask the CTO" topics.

DAC Pavilion - Booth #1372

Tuesday, 11:30 AM - 12:00 PM

Student Design Contest Award Presentations

Co-Chairs: Steven Levitan, Alan Mantooth, David Greenhill

The Student Design Contest is sponsored by the Design Automation Conference (DAC) and the International Solid State Circuits Conference (ISSCC) to promote excellence in the design of electronic systems by providing competition between graduate and undergraduate students at universities and colleges. Designs can be for analog, digital, or programmable circuits and systems. Submissions can be embodied as integrated circuits, reconfigurable processors, SoCs, platform-based or embedded systems designs.

Tuesday, 12:00 PM - 1:00 PM

ARM Twisting: Ask Sir Robin

Interview co-organized with IEEE Design & Test of Computers

Moderator: Kenneth W. Wagner - *IEEE Design & Test of Computers*

Panelist: Sir Robin Saxby - Chairman, *ARM Holdings plc*

Following the keynote speech by Sir Robin Saxby, Founder of ARM Ltd. and Chairman of ARM Holdings plc will be interviewed live at the DAC pavilion. The interview will touch upon a range of issues including the secret behind ARM's success as a global leader in semiconductor IP, his view of the foundaries, semiconductor and systems design companies, and what the future holds. This interview is co-organized with the IEEE Design & Test of Computers.

Tuesday, 3:00 PM - 4:00 PM

EDA Business Forecast Highlights

Moderator: Dennis Brophy - *Model Technology, a Mentor Graphics Co.*

Panelist: Gary Smith - *Gartner/Dataquest*

The annual Gartner/Dataquest EDA forecast for will be released prior to the start of the Design Automation Conference. Highlights from that presentations and questions that have come from it will be posed to explore the trends and directions of the industry.

Wednesday, 10:30 AM - 11:30 AM

Wall Street's View of EDA - The 2003 Update

Moderator: Jessica Kourakos - *Synopsys, Inc.*

Panelists: Sumit Dhanda - *Bank of America Securities*
Jose Medeiros - *Blum Capital Partners*

2003 is the third year of the economic stall for systems and semiconductor companies. While EDA has held up relatively well compared to these sectors, the duration of the downturn finally affected EDA in 2002 and will likely continue to put pressure on the industry in 2003. This has resulted in a stop to the flurry of EDA IPOs we saw over the last couple of years and the heightened level of industry consolidation as startups seek new rounds of funding with limited success. Given this backdrop, it is time to reassess how Wall Street views EDA as an investment opportunity in 2003 and beyond and to obtain a fresh perspective on what EDA vendors should be doing to best respond to the changing environment. This pavilion discussion is geared as an update to a panel held at DAC 2002 on this subject.

Wednesday, 12:00 PM - 1:00 PM

Platforms-YES, but What Type Is Best?

Moderator: Grant Martin - *Cadence Design Systems, Inc.*

Panelists: Chris Lennard - *ARM, Ltd.*
Patrick Lysaght - *Xilinx, Inc.*

The term "Platform" may seem old, but the problems associated with it are only now surfacing with the availability of platform based products. There are many different types and the scope of platforms extends well beyond hardware. ASIC/ASSP style platforms take one approach; reconfigurable platforms with hard processor cores a somewhat different one. The tradeoffs for using one or the other are quite different. In addition, since all SoC platforms involve processors, the question of software infrastructure and who provides it is a key one for platform developers and users. In this panel, a proponent of a "middle-out architectures" approach to platform based design, and a proponent of a "bottoms-up libraries" approach, will have a dialogue between these quite different points of view.

Monday, June 2, 2003

	Room 210AB	Room 211AB	Room 210CD	Room 205AB	Room 209AB
9:00	**Tutorial 1** Design Techniques for Power Reduction (Continental Breakfast 8:00 AM - 9:00 AM)	**Hands-on Tutorial** What is All This Noise About Signal and Power Integrity? • *Sequence Design, Inc.*			
10:00					Introduction to Chips and EDA For a Non-Technical Audience 10:00 AM - 12:00 PM
12:00	Lunch				
1:00	**Tutorial 1 (cont.)** Design Techniques for Power Reduction	**Hands-on Tutorial** Signal and Power Integrity Analysis and Methodology • Cadence Design Systems, Inc., IOTA Technology Inc., Synplicity, Inc.	Interoperability Workshop 12:00 PM - 5:00 PM	Lunch 1:00 PM Workshop for Women in Design Automation: Would Life be Different if Risk Were Not a Factor? Managing Life & Career Transition 2:00 PM - 5:00 PM	
2:00					
5:00					

Booth #1372
DAC Pavilion
Managing Mask Costs 10:30 - 11:30
Semiconductor IP Business - Is it Real? 12:00 - 1:00
Ask the CTO 1:00 - 2:00

Exhibit Hours 10:00 AM - 6:00 PM / **Demo Suite Hours** 8:00 AM - 9:00 PM

Tutorial 1 - Design Techniques for Power Reduction - see pg 36

Hands-on Tutorial - What is All This Noise About Signal and Power Integrity? • Sequence Design, Inc. • see pg 60

Hands-on Tutorial - Signal and Power Integrity Analysis and Methodology • Cadence Design Systems, Inc., IOTA Technology Inc., Synplicity, Inc. • see pg 61

Interoperability Workshop • see pg 41

Workshop for Women in Design Automation • see pg 40

Would Life be Different if Risk Were Not a Factor? Managing Life & Career Transition

Introduction to Chips and EDA For a Non-Technical Audience • see pg 39

Tuesday, June 3, 2003

- indicates videoed session

Opening Session and Keynote Speaker Location: Ballroom A-C

<100nm...A Giant Leap for Mankind?

Sir Robin Saxby – Chairman, ARM Holdings plc, Cambridge, UK

8:30 to 10:00

BREAK 10:15 – 10:30

Booth #1372	Ballroom AB	207A-D	210CD	210AB	209AB	
DAC Pavilion	Session 1	Session 2	Session 3	Session 4	Session 5	
Student Design Contest Awards 11:30 - 12:00	**SPECIAL SESSION:** Real Challenges and Solutions for Validating Systems-on-Chip	**PANEL:** Reshaping EDA for Power	Design for Manufacturability and Global Routing	Design Analysis Techniques	Embedded Hardware Design Case Studies	10:30 to 12:00
ARM Twisting: Ask Sir Robin 12:00 - 1:00						
EDA Business Forecast Highlights 3:00 - 4:00						
	LUNCH 12:00 – 2:00					
	Session 6	Session 7	Session 8	Session 9	Session 10	
	SPECIAL SESSION: Emerging Design and Tool Challenges in RF and Wireless Applications	**PANEL:** COT - Customer Owned Trouble?	Power Grid Analysis and Optimization	Low-Power Embedded System Design	Cyclic and Non-Cyclic Combinational Circuit Synthesis	2:00 to 4:00
	BREAK 4:00 – 4:30					
	Session 11	Session 12	Session 13	Session 14	Session 15	
	Managing Leakage Power	**PANEL:** Emerging Markets: Design Goes Global	Timing-Oriented Placement	Model Order Reduction	Issues in Partitioning and Design Space Exploration for Codesign	4:30 to 6:30

2:00-5:00 Hands-on Experience on Signal Integrity and Ground Bounce in PCBs and IC Packages

hands-on

SIGDA Ph.D. Forum In Rm. 213A-C from 6:30 PM – 9:00 PM

Exhibit Hours 10:00 AM - 6:00 PM / **Demo Suite Hours** 8:00 AM - 9:00 PM

All Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Presenters will be available in room 208AB for additional 20-minute question and answer periods after the session.

Wednesday, June 4, 2003

	Ballroom AB	207A-D	210CD	210AB	209AB
	Session 16	**Session 17**	**Session 18**	**Session 19**	**Session 20**
8:30 to 10:00	**SPECIAL SESSION:** Nano Technology: Design Implications and CAD Challenges	**PANEL:** Mixed Signals on Mixed-Signal: The Right Next Technology	Simulation Coverage and Generation for Verification	Tool Support for Architectural Decisions in Embedded Systems	New Topics in Logic Synthesis
	BREAK 10:00 - 10:30				
	Session 21	**Session 22**	**Session 23**	**Session 24**	**Session 25**
10:30 to 12:00	**SPECIAL SESSION:** Coping with Variability: The End of Deterministic Design	**PANEL:** Cheap Submicron: The Next Implementation Fabric An IEEE D&T Feature Panel	Testbench, Verification and Debugging: Practical Considerations	Delay and Noise Modeling in the Nanometer Regime	Modeling Issues in the Design of Embedded Systems
	LUNCH 12:00 - 2:00				
	Session 26	**Session 27**	**Session 28**	**Session 29**	**Session 30**
2:00 to 4:00	**SPECIAL SESSION:** How Application/ Technology Evolutions will Shape Classical EDA?	SAT and BDD Algorithms for Verification Tools	Elements of Functional and Performance Analysis	Nonlinear Model Order Reduction	Novel Techniques in High-Level Synthesis
	BREAK 4:00 - 4:30				
	Session 31	**Session 32**	**Session 33**	**Session 34**	**Session 35**
4:30 to 6:30	Mixed-Signal Design and Simulation	**PANEL:** Nanometer Design: Place Your Bets	Novel Self-Test Methods	Technology Mapping, Buffering, and Bus Design	Compilation Techniques for Reconfigurable Devices

Booth #1372

DAC Pavilion

Wall Street's View of EDA - The 2003 Update
10:30 - 11:30

Platforms-YES, but What Type is Best?
12:00 - 1:00

9:00-12:00 Ensuring Signal and Power Integrity at Nanometer Technologies
hands-on

2:00-5:00 3.125 Gbps With Your Hair on Fire
hands-on

Wednesday Night Party • 7:30 PM - 10:00 PM • Disney's California Adventure™ park

Exhibit Hours 10:00 AM - 6:00 PM / **Demo Suite Hours** 8:00 AM - 9:00 PM

All Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Presenters will be available in room 208AB for additional 20-minute question and answer periods after the session.

Thursday, June 5, 2003

- indicates videoed session

9:00-12:00 Full-Chip Dynamic Power Grid Methodology From hands-on Planning to Verification

Ballroom AB	207A-D	210CD	210AB	209AB	
Session 36	**Session 37**	**Session 38**	**Session 39**	**Session 40**	
Architectural Power Estimation and Optimization	**PANEL:** Libraries: Lifejacket or Straitjacket?	Techniques for Reconfigurable Logic Applications	Test and Diagnosis for Complex Designs	**SPECIAL SESSION:** Highlights of ISSCC: High-Speed Heterogenous Design Techniques	8:30 to 10:00
BREAK 10:00 - 10:30					
Session 41	**Session 42**	**Session 43**	**Session 44**	**Session 45**	
SPECIAL SESSION: Highlights of ISSCC and The Design of State-of-the-Art Microprocessors	**PANEL:** Formal Verification: Prove It or Pitch It	High Frequency Interconnect Modeling	Novel Approaches in Test Cost Reduction	Retargetable Tools for Embedded Software	10:30 to 12:00
Keynote - *The Tides of EDA* • 1:00 - 1:45 • Room: Ballroom A-C ***Alberto L. Sangiovanni-Vincentelli*** - Professor, Univ. of California, Berkeley, CA				**Best Paper Award Presentations**	

2:00-5:00 Signal and Power Integrity Validation With hands-on In-Circuit Measurements

Session 46	**Session 47**	**Session 48**	**Session 49**	**Session 50**	
SPECIAL SESSION: ASIC Design in Nanometer Era - Dead or Alive?	Floorplanning and Placement	Advances in SAT	Novel Design Methodologies and Signal Integrity	Memory Optimization for Embedded Systems	2:00 to 4:00
BREAK 4:00 - 4:30					
Session 51	**Session 52**	**Session 53**	**Session 54**	**Session 55**	
SPECIAL SESSION: Design Automation for Quantum Circuits	Energy-Aware System Design	Budgeting, Simulation and Statistical Timing	Interconnect Noise Avoidance Methodologies and Slew Rate Prediction	Analog Design Space Exploration	4:30 to 6:00

Demo Suite Hours 8:00 AM - 5:00 PM

All Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Presenters will be available in room 208AB for additional 20-minute question and answer periods after the session.

Tuesday
June 3

10:30
to
12:00

All speakers are denoted in **bold**

S – denotes short paper

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Session 1

rm: Ballroom AB

SPECIAL SESSION: REAL CHALLENGES AND SOLUTIONS FOR VALIDATING SYSTEMS-ON-CHIP

CHAIR: Wolfgang Rosenstiel - *Univ. of Tubingen, Tubingen, Germany*
ORGANIZER: Wolfgang Rosentiel

The first paper will discuss the application of FPV to the validation of the Pentium® 4 microarchitecture. New approaches are considered to broaden the application of FV techniques, particularly at higher abstraction levels. GSTE and SAT will significantly increase the scope of what can be formally verified. Second, the verification strategy for the integration of a multi-processors baseband chip for the 3G wireless phone market is presented. Examples and metrics illustrate the key design challenges of large SoC verification, enhancement opportunities are explored. Last but not least the development of large servers is facing multiple challenges like mixing design styles from custom VLSI to ASIC and SoC designs, including various IP as well as a combination of hardware and firmware.

1.1 High-Level Formal Verification of Next-Generation Microprocessors

Tom Schubert - *Intel Corp., Hillsboro, OR*

1.2 Verification Strategy for Integrating 3G Baseband Soc

Yves Mathys - *Motorola, Inc., Geneva, Switzerland*

1.3 Improvements In Functional Simulation Addressing Challenges In Large, Distributed Industry Projects

Klaus-Dieter Schubert - *IBM Corp., Boeblingen, Germany*

Session 2

rm: 207A-D

PANEL: RESHAPING EDA FOR POWER

CHAIR: Jan Rabaey - *Univ. of California, Berkeley, CA*
ORGANIZERS: Dennis Sylvester, David Blaauw

Today's rising power densities are reminiscent of the end of the bipolar design era twenty years ago and are widely cited as the foremost challenge to continued CMOS scaling. On a more optimistic note, the power bottleneck provides excellent opportunities for EDA innovation in areas such as leakage reduction, power distribution, and low-power clocking. This panel brings together experts in circuit design and CAD tool development to discuss the current status of low-power EDA offerings and provide opinions on what new capabilities are most important in the power-constrained design era.

2.1 Reshaping EDA for Power

PANELISTS: Kerry Bernstein - *IBM Corp., Essex Junction, VT*
Jerry Frenkil - *Sequence Design Inc., Acton, MA*
Mark Horowitz - *Stanford Univ., Stanford, CA*
Wolfgang Nebel - *Oldenburg Univ., Oldenburg, Germany*
Takayasu Sakurai - *Univ. of Tokyo, Tokyo, Japan*
Andrew Yang - *Apache Design Solutions, Inc. Mountain View, CA*

Design Methods Sessions are shaded red. Embedded Systems Sessions are shaded grey.

Session 3

rm: 210CD

DESIGN FOR MANUFACTURABILITY AND GLOBAL ROUTING

CHAIR: Martin Wong - *Univ. of Illinois, Urbana, IL*
ORGANIZERS: Charles J. Alpert, Dennis Sylvester, Raymond Nijssen

This session addresses manufacturability topics that become prominent in subwavelength lithography as well as issues relating to the prominence of global interconnections in IC performance. The first paper focuses on reducing the cost of making optical proximity corrections by manipulating commercial sizing tools. The second paper describes a first approach to limiting the impact of metal fill on circuit delay. The third paper proposes a new method to reduce congestion in global routing by avoiding unnecessary detours. The final presentation presents an example showing the relationship between architecture and physical design.

3.1 A Cost-Driven Lithographic Correction Methodology Based on Off-the-Shelf Sizing Tools

Puneet Gupta, Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*
Dennis Sylvester, Jie Yang - *Univ. of Michigan, Ann Arbor, MI*

3.2 Performance-Impact Limited Area Fill Synthesis

Yu Chen- *Univ. of California, Los Angeles, CA*
Puneet Gupta - *Univ. of California at San Diego, La Jolla, CA*

3.3s Improved Global Routing by Amplified Congestion Estimation

Raia T. Hadsell, Patrick H. Madden - *State Univ. of New York, Binghamton, NY*

3.4s Microarchitecture Evaluation With Physical Planning

Jason Cong, Ashok Jagannathan, Glenn Reinman, Michail Romesis - *Univ. of California, Los Angeles, CA*

Session 4

rm: 210AB

DESIGN ANALYSIS TECHNIQUES

CHAIR: Michael Kishinevsky - *Intel Corp., Hillsboro, OR*
ORGANIZERS: Ahmed A. Jerraya, Steven Haynal

This session addresses different design flows as well as design environments. The main focus is on high-level design issues and their role in the design process. The first issue will be design techniques for differential power analysis protection. The second topic is a methodology that uses a SystemC and a network simulation environment for the verification of a 802.11 MAC chip design. Finally the the application of design patterns to hardware design is discussed.

4.1 Energy Aware Design Techniques for Differential Power Analysis Protection

Luca Benini - *Deis Univ. Di Bologna, Bologna, Italy*
Alberto Macii, Enrico Macii - *Politecnico di Torino, Torino, Italy*
Elvira Omerbegovic - *BullDAST s.r.l., Torino Italy*
Massimo Poncino - *Univ. Di Verona, Verona, Italy*
Fabrizio Pro - *BullDAST s.r.l., Torino, Italy*

4.2 A Timing-Accurate Modeling and Simulation Environment for Networked Embedded Systems

Franco Fummi - *Univ. Di Verona, Verona, Italy*
Paolo Gallo - *Telecom Italia Lab., Torino, Italy*
Stefano Martini, Giovanni Perbellini - *Embedded Systems Design Ctr., Verona, Italy*
Massimo Poncino - *Univ. Di Verona, Verona, Italy*
Fabio Ricciato - *Telecom Italia Lab., Torino, Italy*

4.3 Application of Design Patterns for Hardware Design

Robertas Damasevicius, Giedrius Majauskas, Vytautas Stuikys - *Kaunas Univ. of Tech., Kaunas, Lithuania*

Session 5

rm: 209AB

EMBEDDED HARDWARE DESIGN CASE STUDIES

CHAIR: Chris Rowen - *Tensilica, Inc., Santa Clara, CA*
ORGANIZERS: Grant E. Martin, Kurt Keutzer, Pai H. Chou

The range of embedded hardware design applications is extremely wide and this session illustrates it. The first paper comes from the student design competition and presents an interesting design approach for a portable secure embedded system. The second paper deals with the design of an advanced high performance memory system for embedded System-on-chip design. The final paper introduces a whole new application area and systematic design approach to DAC: light sensor components for embedded appliances. This is an exciting group of applications that illustrate the interaction between embedded design and methodologies.

5.1 STUDENT DESIGN CONTEST: Design Flow for HW/SW Acceleration Transparency In the ThumbPod Secure Embedded System

David Hwang, Patrick Schaumont, Yi Fan, Alireza Hodjat, Bo Cheng Lai, Kazuo Sakiyama, Shenglin Yang, Ingrid Verbauwhede - *Univ. of California, Los Angeles, CA*

5.2 A Fully-Programmable Memory Management System Optimizing Queue Handling at Multi Gigabit Rates

George Kornaros, Ioannis Papaefstathiou, Aristidis Nikologiannis, Nikolaos Zervos - *Ellemedia Tech., Heraklio, Greece*

5.3 Design Techniques for Sensor Appliances: Foundations and Light Compass Case Study

Jennifer L. Wong, Seapahn Megerian, Miodrag Potkonjak - *Univ. of California, Los Angeles, CA*

Tuesday
June 3

2:00
to
4:00

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Session 6

rm: Ballroom AB

SPECIAL SESSION: EMERGING DESIGN AND TOOL CHALLENGES IN RF AND WIRELESS APPLICATIONS

CHAIR: Georges Gielen - *Katholieke Univ., Leuven, Belgium*
ORGANIZER: Limor Fix

RF/wireless applications have emerged as important markets, driven by cellular and high-speed wireless data communications (e.g. 802.11 WLAN), but with other applications such as 4G communications, ambient intelligence and ubiquitous ad-hoc sensor networks looming on the horizon. This special session will address the challenges in terms of design capabilities, technology choices and design tools that are ahead of us to materialize these applications. Starting from the system requirements, an overview will be given of technology choices and design challenges that await the designers at both the system architectural level and the circuit level. Also new modeling and simulation tools for these systems will be discussed.

6.1 Seamless Multi-Radio Integration Challenges
Uri Barkai - *Intel Corp., Petach-Tikva, Israel*

6.2 RF SoC-CMOS vs. Bipolar Technology
Pieter Hooijmans - *Philips Research Labs., Eindhoven, The Netherlands*

6.3 4G-Terminals: How are We Going To Design Them
Jan Craninckx, Stephane Donnay - *IMEC, Leuven, Belgium*

6.4 New Techniques for Non-Linear Behavioral Modeling of Microwave/RF ICs from Simulation and Non-Linear Microwave Measurement
David E. Root, John Wood, Nick Tufillaro - *Agilent Technologies, Santa Rosa, CA*

Session 7

rm: 207A-D

PANEL: COT – CUSTOMER OWNED TROUBLE?

CHAIR: Bob Dahlberg - *ReShape, Inc., Mountain View, CA*
ORGANIZERS: Jen Bernier, Shishpal Rawat

Increasingly, system houses are attracted to the COT model to gain more control on their schedules and cost. The pathways to implement a COT design include (a) Manage the sourcing (internal or third party resources) of individual supply chain and cost reduction functions (b) Use an integrated design-to-parts service or (c) A hybrid of these two extremes. COT project risk and cost are high, so the design team needs to be expertly prepared. This panel will consider the pros and cons for each approach.

7.1 COT – Customer Owned Trouble?

PANELISTS: Gina Gloski - *eSilicon, Sunnyvale, CA*
Aurangzeb Khan - *Cadence Design Systems, Inc., San Jose, CA*
Kaushik Patel - *Azanda Network Devices, Sunnyvale, CA*
Paul Ruddy - *Cisco Systems, San Jose, CA*
Naveed Sherwani - *Intel Corp., Portland, OR*
Ronnie Vasishta - *LSI Logic Corp., Milpitas, CA*

Session 8

rm: 210CD

POWER GRID ANALYSIS AND OPTIMIZATION

CHAIR: Sani R. Nassif - *IBM Corp., Austin, TX*
ORGANIZERS: Abhijit Dharchoudhury, Anirudh Devgan

CMOS scaling is leading to a reduction in the power supply voltage and a simultaneous increase in the on-chip power density. This trend mandates increased focus on power grid signal integrity. This session deals with exciting new approaches in the analysis and optimization of on-chip power networks. The first paper presents a technique for static power drop estimation, followed by two papers on power grid analysis using algebraic multi-grid techniques. Fourth paper addresses impact of leakage on the supply integrity. The last paper presents techniques for optimizing the power distribution network.

8.1 Random Walks in a Supply Network

Haifeng Qian - *Univ. of Minnesota, Minneapolis, MN*
Sani R. Nassif - *IBM Corp., Austin, TX*
Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

8.2 A Static Pattern-Independent Technique for Power Grid Voltage Integrity Verification

Dionysios Kouroussis, Farid N. Najm - *Univ. of Toronto, Toronto, ON, Canada*

8.3s Analyzing Power Network of General Topology Using an Adaptive Algebraic Multigrid Approach

Zhengyong Zhu, Bo Yao, Chung-Kuan Cheng, Ernest Kuh - *Univ. of California, Berkeley, CA*

8.4s Power Grid Reduction Based on Algebraic Multigrid Principles

Haihua Su, Emrah Acar, Sani R. Nassif - *IBM Corp., Austin, TX*

8.5 On-chip Power Supply Network Optimization Using Multigrid-based Technique

Kai Wang, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*

Session 9

rm: 210AB

LOW-POWER EMBEDDED SYSTEM DESIGN

CHAIR: Rajesh K. Gupta - *Univ. of California at San Diego, La Jolla, CA*
ORGANIZERS: Diederik Verkest, Taewhan Kim

The session presents papers in embedded low power system design considering various design aspects such as variable voltage scaling, memory organization for low power, and power management using component mode transitions.

9.1 Scalable Modeling and Optimization of Mode Transitions Based on Decoupled Power Management Architecture

Dexin Li, Qiang Xie, Pai H. Chou, Nader Bagherzadeh - *Univ. of California, Irvine, CA*

9.2 Optimal Voltage Allocation Techniques for Dynamically Variable Voltage Processors

Woo-Cheol Kwon - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*
Taewhan Kim - *KAIST, Daejon, Republic of Korea*

9.3 Energy Reduction Techniques for Multimedia Applications with Tolerance to Deadline Misses

Shaoxiong Hua, Gang Qu, Shuvra Bhattacharya - *Univ. of Maryland, College Park, MD*

9.4 Xtream-Fit: An Energy-Delay Efficient Data Memory Subsystem for Embedded Media Processing

Anand Ramachandran, Margarida F. Jacome - *Univ. of Texas, Austin, TX*

Session 10

rm: 209AB

CYCLIC AND NON-CYCLIC COMBINATIONAL CIRCUIT SYNTHESIS

CHAIR: Victor Kravets - *IBM Corp., Yorktown Heights, NY*
ORGANIZERS: Marek Perkowski, Soha Hassoun

This session addresses logic minimization. The first paper presents practical enhancements to recently proposed constructive decomposition. The second paper proposes a new approach to SOP minimization based on decomposition. The third paper explores novel general cofactoring for multi-valued functions to speed up functional evaluation. The last two papers address combinational optimizations for cyclic circuits.

10.1 A New Enhanced Constructive Decomposition and Mapping Algorithm

Alan Mishchenko - *Univ. of California, Berkeley, CA*
Xinning Wang, Timothy Kam - *Intel Corp., Hillsboro, OR*

10.2 Large-Scale SOP Minimization Using Decomposition and Functional Properties

Alan Mishchenko - *Univ. of California, Berkeley, CA*
Tsutomu Sasao - *Kyushu Institute of Tech., Fukuoka, Japan*

10.3s Generalized Cofactoring for Logic Function Evaluation

Yunjian Jiang, Slobodan Matic, Robert K. Brayton - *Univ. of California, Berkeley, CA*

10.4s Making Cyclic Circuits Acyclic

Stephen A. Edwards - *Columbia Univ., New York, NY*

10.5 The Synthesis of Cyclic Combinational Circuits

Marc D. Riedel, Jehoshua Bruck - *Caltech, Pasadena, CA*

Tuesday
June 3

4:30
to
6:30

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Session 11

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MANAGING LEAKAGE POWER

CHAIR: Siva Narendra - *Intel Corp., Hillsboro, OR*
ORGANIZER: Renu Mehra

Leakage power consumption is projected to be one of the most dominant power components in very deep-submicron technologies. Papers in this session address different issues related to leakage power estimation and minimization.

11.1 Accurate Estimation of Total Leakage Current In Scaled CMOS Logic Circuits Based on Compact Current Modeling

Saibal Mukhopadhyay, Arijit Raychowdhury, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

11.2 Analysis and Minimization Techniques for Total Leakage Considering Gate Oxide Leakage

Dongwoo Lee, Wesley Kwong, Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

11.3 Distributed Sleep Transistor Network for Power Reduction

Changbo Long - *Univ. of Wisconsin, Madison, WI*
Lei He - *Univ. of California, Los Angeles, CA*

11.4s Implications of Technology Scaling on Leakage Reduction Techniques

Yuh-Fang Tsai - *Penn State Univ., University Park, PA*
David Duarte - *Intel Corp., Portland, OR*
Vijaykrishnan N., Mary J. Irwin - *Penn State Univ., University Park, PA*

11.5s Static Leakage Reduction through Simultaneous Threshold Voltage and State Assignment

Dongwoo Lee, **David Blaauw** - *Univ. of Michigan, Ann Arbor, MI*

Session 12

rm: 207A-D

PANEL: EMERGING MARKETS: DESIGN GOES GLOBAL

CHAIR: Chi-Foon Chan - *Synopsys, Inc., Mountain View, CA*
ORGANIZERS: Deirdre Hanford, Jian-Yue Pan, Narendra V. Shenoy

China and India represent two of the most rapidly evolving markets for IC design today. According to the CMP China IC Design Survey 2002, demand for IC design services in China is growing exponentially alongside 8- and 12-inch wafer fab construction. In India, multinationals and local companies continue to accelerate the development of complex ICs, matching the sophistication of design teams world wide. China and India are graduating the most EEs annually of any other countries. This dynamic growth of IC design and its associated infrastructure in China & India is causing all participants in the semiconductor value chain to carefully consider their business interactions in these countries. This panel will evaluate how IC design is changing in these emerging markets. Panelists will represent a variety of viewpoints, including multinationals, local government, local universities, and large local companies. The panel will also explore the effect of this emerging market on the EDA industry.

12.1 Emerging Markets: Design Goes Global

PANELISTS: Mahesh Mehendale - *Texas Instruments, Inc., Bangalore, India*
A. Vasudevan - *Wipro Technologies, Bangalore, India*
Sam T. Wang - *Semiconductor Manufacturing International Corp., Shanghai, China*
Shaojun Wei - *Datang Telecom, Beijing, China*

Session 13

rm: 210CD

TIMING-ORIENTED PLACEMENT

CHAIR: Ralph H.J.M. Otten - *Eindhoven Univ. of Tech., Eindhoven, The Netherlands*
ORGANIZERS: C. Y. Roger Chen, Carl Sechen

Since delay is an increasingly important issue in chip design, emphasis is shifting from area and wire length towards timing. Delay budgeting and retiming have found their place in design trajectory, but integration with placement is very much a topic of today. Also the possibility of logic replication in order to meet timing constraints will be considered in this session. Once the timing requirements can be formulated as constraints on nets, powerful tool combinations can provide high quality placements.

13.1 Timing Optimization of FPGA Placements by Logic Replication

Giancarlo Beraudo, John Lillis - *Univ. of Illinois, Chicago, IL*

13.2 Delay Budgeting in Sequential Circuits with Application to FPGA Placement

Steve Yeh, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*

13.3 Multilevel Global Placement with Retiming

Jason Cong, Xin Yuan - *Univ. of California, Los Angeles, CA*

13.4 Force Directed Mongrel with Physical Net Constraints

Tung Cao - *Intel Corp., Santa Clara, CA*
Sung Hur - *Syracuse Univ., Syracuse, NY*
Amit Chowdhary - *Intel Corp., Santa Clara, CA,*
Bill Halpin - *Intel/Syracuse Univ., Santa Clara, CA*
Yegna Parasuram, Karthik Rajagopal, Vladimir Tiourin - *Intel Corp., Santa Clara, CA*

Session 14

rm: 210AB

MODEL ORDER REDUCTION

CHAIR: Ying (Frank) Liu - *IBM Corp., Austin, TX*
ORGANIZER: Sachin S. Sapatnekar

Model order reduction is a critical component in CAD extraction and verification. The first two papers focus on realizable reduction of RLCK networks. The third paper proposes a novel reduction method incorporating skin effect, and the final paper addresses modeling of nonuniform transmission lines.

14.1 Realizable Parasitic Reduction Using Generalized Y-Δ Transformation

Zhanhai Qin, C. K. Cheng - *Univ. of California at San Diego, La Jolla, CA*

14.2 Realizable RLCK Circuit Crunching

Chirayu S. Amin, Masud H. Chowdhury, Yehea I. Ismail - *Northwestern Univ., Evanston, IL*
Chandramouli V. Kashyap, Byron L. Krauter - *IBM Corp., Austin, TX*

14.3 Efficient Model Order Reduction Including Skin Effect

Shizhong S. Mei, Chirayu Amin, Yehea I. Ismail - *Northwestern Univ., Evanston, IL*

14.4 Model Order Reduction of Nonuniform Transmission Lines Using Integrated Congruence Transform

Emad F. Gad, Michel Nakhla - *Carleton Univ., Ottawa, ON, Canada*

Session 15

rm: 209AB

ISSUES IN PARTITIONING AND DESIGN SPACE EXPLORATION FOR CODESIGN

CHAIR: Nikil Dutt - *Univ. of California, Irvine, CA*
ORGANIZERS: Donatella Sciuto, Jan Madsen

The first paper presents a system level approach to simplify task scheduling by grouping tasks which should be executed on the same resource. The second paper presents run-time partitioning where software is monitored and possible dynamically translated into hardware, based on monitoring and synthesis algorithms placed in hardware. Third paper performs instruction set extension based on capabilities provided by the processor architecture. The fourth paper presents generation of abstract instruction encodings needed for software tool generation during architecture exploration.

15.1 Partial Task Assignment of Task Graphs under Heterogeneous Resource Constraints

Radoslaw W. Szymanek, Krzysztof Kuchcinski - *Lund Univ., Lund, Sweden*

15.2 Dynamic HW/SW Partitioning: A First Approach

Greg M. Stitt, Roman Lysecky, Frank Vahid - *Univ. of California, Riverside, CA*

15.3 Automatic Application-Specific Instruction-Set Extensions under Microarchitectural Constraints

Kubilay Atasu, Laura Pozzi - *EPFL-I&C-LAP, Lausanne, Switzerland*
Paolo Ienne - *Swiss Federal Institute of Tech., Lausanne, Switzerland*

15.4 Instruction Encoding Synthesis for Architecture Exploration using Hierarchical Processor Models

Achim Nohl, Volker Greive - *CoWare, Inc., San Jose, CA*
Rainer Leupers, Gunnar Braun - *Aachen Univ. of Tech., Aachen, Germany*
Oliver Schliebusch - *ISS, Aachen, Germany*
Heinrich Meyr - *Aachen Univ. of Tech., Aachen, Germany*

Wednesday
June 4

8:30
to
10:00

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Session 16

rm: Ballroom AB

SPECIAL SESSION: NANO TECHNOLOGY: DESIGN IMPLICATIONS AND CAD CHALLENGES

CHAIR: Xiaobo Sharon Hu - *Univ. of Notre Dame, Notre Dame, IN*

ORGANIZERS: Xiaobo Sharon Hu, Wolfgang Porod

Nano technology and devices will have revolutionary impact on the CAD field. Similarly, CAD research at circuit, logic and architectural levels for nano devices can provide valuable feedbacks to nano research and illuminate ways for developing new nano devices. It is time for CAD researchers to play an active role in nano research. This special session aims to arouse the interests of CAD researchers in more ``revolutionary'' types of nano devices. It brings together a group of industry and academia experts to review latest advances in molecular electronics and discuss design implications and CAD challenges introduced by nano devices.

16.1 Quantum-dot Cellular Automata: Computing by Polarized Systems

Gary H. Bernstein - *Univ. of Notre Dame, Notre Dame, IN*

16.2 Recent Advances and Future Prospects in Single-Electronics

Christoph Wasshuber - *Texas Instruments, Inc., Dallas, TX*

16.3 Manipulation and Characterization of Molecular Scale Components

Islamshah Amlani - *Motorola, Inc., Tempe, AZ*

Session 17

rm: 207A-D

PANEL: MIXED SIGNALS ON MIXED-SIGNAL: THE RIGHT NEXT TECHNOLOGY

CHAIR: Rob A. Rutenbar - *Carnegie Mellon Univ., Pittsburgh, PA*

ORGANIZERS: James Spoto, Rob A. Rutenbar

CMOS dominates digital microelectronics. However, wireless applications require RF circuits at 1-5GHz, and exotic higher frequency applications are on the horizon. Silicon-Germanium (SiGe) is a growing choice for these designs. But is it "the" answer? Some argue that scaled CMOS will handle all tomorrow's RF ICs. Others argue that one-chip SoC solutions will never be the winning strategy for these highly heterogeneous designs, and place their bets on system-in-package (SiP) technologies. Is there a right answer here? Is CMOS the "only" way, or just "another" way?

17.1 Mixed Signals on Mixed-Signal: The Right Next Technology

PANELISTS: David Harame - *IBM Corp., Burlington, VT*
Kurt Johnson - *Cadence Design Systems, Inc., San Jose, CA*
Paul Kempf - *Jazz Semiconductor, Newport Beach, CA*
Teresa Meng - *Stanford Univ./ Atheros Communications, Stanford, CA*
Reza Rofougaran - *Broadcom, El Segundo, CA*
James Spoto - *Applied Wave Research, Inc., El Segundo, CA*

Session 18

rm: 210CD

SIMULATION COVERAGE AND GENERATION FOR VERIFICATION

CHAIR: Umberto Rossi - *STMicroelectronics, Agrate Brianza, Italy*

ORGANIZERS: Hikeung T. Ma, Shin-ichi Minato

Coverage of assertions, source code, FSMs and other measures is common in the industry. The first three papers of this session deal with interesting ways of measuring coverage and industrial experience. The last paper deals with an algorithm to generate simulation vectors in a constrained random way.

18.1 Coverage-Oriented Verification of Banias

Alon Gluska - *Intel Corp., Haifa, Israel*

18.2 Coverage Directed Test Generation for Functional Verification using Bayesian Networks

Shai Fine, Avi Ziv - *IBM Haifa Research Lab., Haifa, Israel*

18.3s Dos and Don'ts of CTL State Coverage Estimation

Nikhil Jayakumar, Mitra Purandare, Fabio Somenzi - *Univ. of Colorado, Boulder, CO*

18.4s Constraint Synthesis for Environment Modeling in Functional Verification

Jun Yuan - *Motorola, Inc., Austin, TX*
Adnan Aziz - *Univ. of Texas, Austin, TX*
Carl Pixley - *Synopsys, Inc., Hillsboro, OR*
Ken Albin - *Motorola, Inc., Austin, TX*

Session 19

rm: 210AB

TOOL SUPPORT FOR ARCHITECTURAL DECISIONS IN EMBEDDED SYSTEMS

CHAIR: Grant E. Martin - *Cadence Design Systems, Inc., Berkeley, CA*

ORGANIZERS: Grant E. Martin, Kurt Keutzer, Pai H. Chou

Architects and micro-architects face a vast number of decisions in the development of embedded systems. Software tools have the potential to play a significant role in informing these decisions. This session describes tools that address three different problems in developing embedded architectures. The first paper addresses the high-level problem of refining communication at the application-level on to underlying communication structures. The second paper describes a tool for examining different approaches to code compression. The third paper looks at a tool for evaluating bus-scheduling approaches.

19.1 Automatic Communication Refinement for System Level Design

Samar Abdi, Dongwan Shin, Daniel D. Gajski - *Univ. of California, Irvine, CA*

19.2 CoCo: A Hardware/Software Platform for Rapid Prototyping of Code Compression Technologies

Haris Lekatsas, Joerg Henkel - *NEC Corp., Princeton, NJ*

19.3 A Tool for Describing and Evaluating Hierarchial RealTime Bus Scheduling Policies

Trevor C. Meyerowitz, Claudio Pinello, Alberto L. Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

Session 20

rm: 209AB

NEW TOPICS IN LOGIC SYNTHESIS

CHAIR: Shigeru Yamashita - *NTT Communication Science Labs., Kyoto, Japan*

ORGANIZERS: Marek Perkowski, Steven M. Nowick

The papers in this session explore new topics in logic synthesis. The first paper explores synthesizing optimal two-qubit quantum circuits. The second paper presents novel algorithms for synthesizing reversible circuits in terms of n x n Toffoli gates. The third paper advocates using PLI to model asynchronous circuits at the behavioral level. The final paper describes an algorithm and applications (routing table reductions and access control list reduction) for dynamic on-chip logic minimization.

20.1 A Transformation Based Algorithm for Reversible Logic Synthesis

D. Michael Miller - *Univ. of Victoria, Victoria, BC, Canada*
Dmitri Maslov, Gerhard W. Dueck - *Univ. of New Brunswick, Fredericton, NB, Canada*

20.2 Implementing An Arbitrary Two-qubit Computation In 23 Elementary Gates Or Less

Igor L. Markov, Stephen S. Bullock - *Univ. of Michigan, Ann Arbor, MI*

20.3s Verilog HDL, Powered by PLI: a Suitable Framework for Describing and Modeling Asynchronous Circuits at All Levels of Abstraction

Arash Saifhashemi, Hossein Pedram - *Amirkabir Univ. of Tech., Tehran, Iran*

20.4s On-Chip Logic Minimization

Roman Lysecky, Frank Vahid - *Univ. of California, Riverside, CA*

Wednesday
June 4

10:30
to
12:00

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Session 21

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SPECIAL SESSION: COPING WITH VARIABILITY: THE END OF DETERMINISTIC DESIGN

CHAIR: Michael Orshansky - *Univ. of California, Berkeley, CA*
ORGANIZER: Kurt Keutzer

Tool developers and designers may have thought that after successively facing the challenges of timing closure, deep sub-micron effects, and power problems, they were due for a rest. But this session indicates that increasing process variability may have a more profound impact on tools and design methodology than any of these prior challenges. The first paper defines elements of process variability and discusses the relative magnitudes of their deleterious effects. The second indicates a series of tool and methodology challenges that must be faced if variability is to be managed. The third paper describes technical advances on statistical approaches to modeling timing.

21.1 Parameter Variations and Impact on Circuits & Microarchitecture

Shekhar Borkar - *Intel Corp., Hillsboro, OR*

21.2 Death, Taxes and Failing Chips

Chandu Visweswariah - *IBM Corp., Yorktown Heights, NY*

21.3 Computation and Refinement of Statistical Bounds on Circuit Delay

Aseem B. Agarwal, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*
Vladimir Zolotov - *Motorola, Inc., Austin, TX*
Sarma Vrudhula - *Univ. of Arizona, Tucson, AZ*

Session 22

rm: 207A-D

PANEL: CHEAP SUBMICRON: THE NEXT IMPLEMENTATION FABRIC AN IEEE D&T FEATURE PANEL

CHAIR: Abbas El-Gamal - *Stanford Univ., Stanford, CA*
ORGANIZERS: John Cohn, Andrew B. Kahng

The semiconductor industry is caught on two horns of the economic dilemma: economics of technology, and economics of design productivity. Today, design is slow, expensive, and out of control. What next-generation fabric will restore cost-effective implementation? The panelists will address such issues as (1) How much regularity is needed for adequate yield and cost control?, (2) Will via-programmability make headway against traditional FPGAs?, (3) Are cost and performance gaps between custom and lower-cost fabrics growing or shrinking?, and (4) What are the n eeds of platform SOC and pure-play foundry constituencies?

22.1 Cheap Submicron: The Next Implementation Fabric

PANELISTS: Andy Bloom - *AMI Semiconductor, Pocatello, ID*
Ivo Bolsens - *Xilinx, Inc., San Jose, CA*
Christopher L. Hamlin - *LSI Logic Corp., Milpitas, CA*
Philippe Magarshack - *STMicroelectronics, Crolles Cedex, France*
Zvi Or-Bach - *eASIC Corp., San Jose, CA*
Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

Session 23

rm: 210CD

TESTBENCH, VERIFICATION AND DEBUGGING: PRACTICAL CONSIDERATIONS

CHAIR: Michael Beaver - *iReady Corp., Santa Clara, CA*

ORGANIZERS: Carl Pixley, Rajeev Ranjan

This session deals with a hybrid method for formal and simulation based verification using high level abstraction as well as how to compare C programs to RTL. In addition, an effective debugger based upon design exploration is presented. Finally an architecture for mapping a design into emulators is presented to vastly speed up verification.

23.1 Using a Formal Specification and a Model Checker to Monitor and Direct Simulation Verifying the Multiprocessing Hardware of the Alpha 21364 Microprocessor

Serdar Tasiran - *KOC Univ., Istanbul, Turkey*
Yuan Yu - *Microsoft Corp., Mountain View, CA*
Brannon Batson - *Intel Corp., Santa Clara, CA*

23.2 Advanced Techniques for RTL Debugging

Bassam Tabbara, Yu Chin Hsu, Yirng An Chen, Furshing Tsai - *Novas Software, Inc., San Jose, CA*

23.3s Behavioral Consistency of C and Verilog Programs Using Bounded Model Checking

Daniel Kroening, Edmund Clarke, Karen Yorav - *Carnegie Mellon Univ., Pittsburgh, PA*

23.4s Re-Use-Centric Architecture for a Fully Accelerated Testbench Environment

Renate Henftling, Andreas Zinn, Matthias Bauer, Martin Zambaldi, Wolfgang Ecker - *Infineon Tech., Munich, Germany*

Session 24

rm: 210AB

DELAY AND NOISE MODELING IN THE NANOMETER REGIME

CHAIR: Vasant Rao - *IBM Corp., Hopewell Junction, NY*

ORGANIZERS: Chandu Visweswariah, Narendra V. Shenoy

Deep sub-micron effects are necessitating the rethinking of delay and noise models for digital circuits. This session describes several novel methods of timing high-performance circuits while taking coupling noise into account.

24.1 An Effective Capacitance Based Driver Output Model for On-Chip RLC Interconnects

Kanak B. Agarwal, Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

24.2s Closed Form Delay and Slew Metrics Made Easy

Charles J. Alpert, Frank Liu, Chandramouli V. Kashyap, Anirudh Devgan - *IBM Corp., Austin, TX*

24.3s Blade and Razor: Cell and Interconnect Delay Analysis Using Current-Based Models

John F. Croix - *Silicon Metrics Corp., Austin, TX*
Martin D. F. Wong - *Univ. of Illinois, Urbana, IL*

24.4 Non-Iterative Switching Window Computation for Delay-Noise

Bhavana Thudi, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

Session 25

rm: 209AB

MODELING ISSUES IN THE DESIGN OF EMBEDDED SYSTEMS

CHAIR: Wolfgang Rosenstiel - *Univ. of Tuebingen, Tuebingen, Germany*

ORGANIZERS: Annette Reutter, Donatella Sciuto

The session is devoted to the presentation of different performance and communication modeling aspects in the design of embedded systems. The first contribution introduces a performance modeling technique for component based embedded system design. The second paper presents a trace transformation method to perfom communication modeling and refinement of applications. The third paper introduces an approach to optimize performance of programmable heterogeneous multiprocessors through model-based scheduling. The fourth contribution introduces a new shared messaging communication model for efficient inter-task communication in signal processing applications.

25.1 Architecture-Level Performance Evaluation of Component-Based Embedded Systems

Jeffry T. Russell, Margarida F. Jacome - *Univ. of Texas, Austin, TX*

25.2 An IDF-based Trace Transformation Method for Communication Refinement

Andy D. Pimentel, Cagkan Erbas - *Univ. of Amsterdam, Amsterdam, The Netherlands*

25.3s Schedulers as Model-Based Design Elements in Programmable Heterogeneous Multiprocessors

JoAnn M. Paul, Alex Bobrek, Jeffrey E. Nelson, Joshua J. Pieper, Donald E. Thomas - *Carnegie Mellon Univ., Pittsburgh, PA*

25.4s A Complexity Effective Communication Model for Behavioral Modeling of Signal Processing Applications

Satya Kiran - *Indian Institute of Tech., New Delhi, India*
Jayram M.N. - *Philips Research Labs., Eindhoven, The Netherlands*
Pradeep Rao, Soumitra K. Nandy - *Indian Institute of Science, Bangalore, India*

Wednesday
June 4

2:00
to
4:00

All speakers are denoted in **bold**

S – denotes short paper

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Session 26

rm: Ballroom AB

SPECIAL SESSION: HOW APPLICATION/TECHNOLOGY EVOLUTIONS WILL SHAPE CLASSICAL EDA?

CHAIR: Ahmed A. Jerraya - *TIMA Lab., Grenoble, France*
ORGANIZERS: Ahmed A. Jerraya, Andrew B. Kahng

26.1 Leading-Edge and Future Design Challenges – Is the Classsical EDA Ready?
Greg Spirakis - *Intel Corp., Santa Clara, CA*

26.2 How to Make Efficient Communication, Collaboration, and Optimization from System to Chip
Akira Matsuzawa - *Tokyo Institute of Tech., Tokyo, Japan*

26.3 Extending SoC Life Beyond the Nanometer Wall
Philippe Magarshack - *STMicroelectronics, Crolles Cedex, France*

26.4 Panel Discussion: Platform Based Design vs. Network on Chip
Greg Spirakis - *Intel Corp., Santa Clara, CA*
Akira Matsuzawa - *Matsushita Electric Industrial Co., Ltd., Osaka, Japan*
Philippe Magarshak - *STMicroelectronics, Crolles Cedex, France,*
Andrew B. Kahng, Alberto L. Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*
Giovanni De Micheli - *Stanford Univ., Stanford, CA*

Session 27

rm: 207A-D

SAT AND BDD ALGORITHMS FOR VERIFICATION TOOLS

CHAIR: Robert Damiano - *Synopsys, Inc., Hillsboro, OR*
ORGANIZERS: Carl Pixley, Hikeung T. Ma, Shin-ichi Minato

SAT and BDDs are the two most prominent algorithms employed in verification tools today. The first paper of this session mixes SAT, separation logic and uninterpreted functions in an efficient way. The second paper defines a new, economical use of BDDs which saves memory. The third paper shows how clever use of circuit structure information can improve the performance of a SAT solver. The fourth paper discusses complete and incomplete methods can be combined to solve the latch mapping problem more efficiently.

27.1 A Hybrid SAT-Based Decision Procedure for Separation Logic with Uninterpreted Functions
Randal E. Bryant, Shuvendu K. Lahiri, Sanjit A. Seshia- *Carnegie Mellon Univ., Pittsburgh, PA*

27.2 Symbolic Representation with Ordered Function Templates
Amit Goel - *Carnegie Mellon Univ., Pittsburgh, PA*

27.3 A Signal Correlation Guided ATPG solver and its Applications For Solving Difficult Industrial Cases
Feng Lu, Li C. Wang, Kwang-Ting Cheng- *Univ. of California, Santa Barbara, CA*
John Moondanos, Ziyad Hanna - *Intel Corp., Hof Carmel, Israel*

27.4 Solving the Latch Mapping Problem in an Industrial Setting
Kelvin Ng - *Univ. of British Columbia, Vancouver, BC, Canada*
Mukul R. Prasad, Rajarshi Mukherjee, Jawahar Jain - *Fujitsu Labs. of America, Inc., Sunnyvale, CA*

Session 28

rm: 210CD

ELEMENTS OF FUNCTIONAL AND PERFORMANCE ANALYSIS

CHAIR: Rolf Ernst - *Technical Univ. of Braunschweig, Braunschweig, Germany*

ORGANIZERS: Annette Reutter, Margarida F. Jacome

The first paper proposes a formalism capturing key features of transaction level models and an associated set of performance metrics to support design space exploration. The second paper shows how to transform complex process interaction patterns into minimum and maximum arrival curves, thus enabling the use of formal real time analysis techniques. The third paper proposes an automatic approach to check whether simulation traces satisfy functional and performance properties. The fourth paper models the combined effects of speculation, caching and wrong path instruction prefetching to determine the WCET of a program.

28.1 Static Analysis of Transaction-Level Models

Giovanni Agosta, Francesco Bruschi, Donatella Sciuto - *Politecnico di Milano, Milano, Italy*

28.2 Enabling Scheduling Analysis of Heterogeneous Systems with Multi-Rate Data Dependencies and Rate Intervals

Marek Jersak, Rolf Ernst - *Technical Univ. of Braunschweig, Braunschweig, Germany*

28.3 Automatic Trace Analysis from Quantitative Constraint Formulas

Xi Chen, Harry Hsieh - *Univ. of California, Riverside, CA*
Felice Balarin, Yosinori Watanabe - *Cadence Berkeley Labs., Berkeley, CA*

28.4 Accurate Timing Analysis by Modeling Caches, Speculation and their Interaction

Xianfeng Li, Tulika Mitra, Abhik Roychoudhury - *National Univ. of Singapore, Singapore, Singapore*

Session 29

rm: 210AB

NONLINEAR MODEL ORDER REDUCTION

CHAIR: Luca Daniel - *Massachusetts Institute of Tech., Cambridge, MA*

ORGANIZER: Kartikeya Mayaram

Nonlinear model order reduction is emerging as a valuable technique for simulation and modeling of analog and MEMS components. The first two papers capture nonlinearities using Volterra series and combine them with Krylov subspace projection methods. The third and fourth papers capture nonlinearities using a trajectory piecewise polynomial and linear approximations combining them with a Krylov subspace projection method and a truncated balance reduction technique respectively.

29.1 NORM: Compact Model Order Reduction of Weakly Nonlinear Systems

Peng Li, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

29.2 Analog and RF Circuits Macromodels for System-Level Analysis

Xin Li, Peng Li, Yang Xu, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

29.3 Piecewise Polynomial Nonlinear Model Reduction

Ning Dong, Jaijeet Roychowdhury - *Univ. of Minnesota, Minneapolis, MN*

29.4 A TBR-based Trajectory Piecewise-Linear Algorithm for Generating Accurate Low-order Models for Nonlinear Analog Circuits and MEMS

Dmitry G. Vasilyev, Michal Rewienski, Jacob White - *Massachusetts Institute of Tech., Cambridge, MA*

Session 30

rm: 209AB

NOVEL TECHNIQUES IN HIGH-LEVEL SYNTHESIS

CHAIR: Christophe Wolinski - *Los Alamos National Lab., Los Alamos, NM*

ORGANIZERS: Gila Kamhi, Krzysztof Kuchcinski

Higher level synthesis is the eagerly wanted technology but seem to be hard to get. This session brings new hopes with innovative techniques to solve some of the known difficulties of high level synthesis. The first paper innovates by using a static analysis technique, based on smart interval methods from affine arithmetic, to help converting full floating point DSP code into finite-precision format. Two papers explore asynchronous design techniques for high level design. They discuss the efficiency of asynchronous synthesis for processor design. Both papers show promising results. The fourth paper combines space exploration methods from parallelizing compiler practice with estimates approaches from behavioral synthesis. It shows that this combination is highly effective and efficient for large space exploration.

30.1 Toward Efficient Static Analysis of Finite-Precision Effects in DSP Applications via Affine Arithmetic Modeling

Claire F. Fang, Rob A. Rutenbar - *Carnegie Mellon Univ., Pittsburgh, PA*

30.2 Automating the Design of an Asynchronous DLX Microprocessor

Manish Amde - *IIT Bombay, Bombay, India*
Ivan Blunno - *Politecnico di Torino, Torino, Italy*
Christos P. Sotiriou - *Institute of Computer Science-Forth, Heraklion, Crete, Greece*

30.3 High-Level Synthesis of Asynchronous Systems by Data-Driven Decomposition

Catherine G. Wong, Alain J. Martin - *Caltech, Pasadena, CA*

30.4 Using Estimates from Behavioral Synthesis Tools in Compiler-Directed Design Space Exploration

Byoungro So, Pedro C. Diniz, Mary W. Hall - *Univ. of Southern California, Marina del Rey, CA*

Wednesday
June 4

4:30
to
6:30

All speakers are denoted in **bold**

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Session 31

rm: Ballroom AB

MIXED-SIGNAL DESIGN AND SIMULATION

CHAIR: Alan Mantooth - *Univ. of Arkansas, Fayetteville, AR*
ORGANIZER: David Allstot

System-on-chip solutions combine analog, digital, RF and MEMS circuits. This session presents emerging analog design and simulation techniques. Two design papers describe a mixed-signal microsystem with integrated MEMS and a fractional-N synthesizer design method. The simulation papers focus on substrate noise, analysis of noise in switched-capacitor circuits and strongly nonlinear symbolic analysis.

31.1 STUDENT DESIGN CONTEST: A 16-Bit Mixed-Signal Microsystem with Integrated CMOS-MEMS Clock Reference

Robert M. Senger, Eric D. Marsman, Michael S. McCorquodale, Fadi H. Gebara, Keith L. Kraver, Richard B. Brown - *Univ. of Michigan, Ann Arbor, MI*

31.2 Fractional-N Frequency Synthesizer Design at the Transfer Function Level Using a Direct Closed Loop Realization Algorithm

Charlotte Y. Lau, Michael H. Perrott - *Massachusetts Institute of Tech., Cambridge, MA*

31.3 Characterizing the Effects of Clock Jitter Due to Substrate Noise In Discrete-Time Δ/Σ Modulators

Payam Heydari - *Univ. of California, Irvine, CA*

31.4s Computation of Noise Spectral Density In Switched Capacitor Circuits using the Mixed-Frequency-Time Technique

Vinita Vasudevan, Ramakrishna Mokkapati - *Indian Institute of Tech.-Madras, Chennai, India*

31.5s An Algorithm for Symbolic Strongly Nonlinear Analysis

Alicia Manthe, **Zhao Li**, Richard Shi - *Univ. of Washington, Seattle, WA*

Session 32

rm: 207A-D

PANEL: NANOMETER DESIGN: PLACE YOUR BETS

CHAIR: Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*
ORGANIZERS: Gloria Nichols, Bing Sheu

In the DAC-2001 debate-panel, "Who's Got Nanometer Design Under Control?", methodologists won the audience vote in a landslide over physics die-hards. Today, physics and economics are much worse than we thought. Yes, methodology can solve any problem, but at what cost? Panelists will prioritize technologies and allocate a fixed R&D budget to address nanometer design challenges. Which problems should get what portion of the budget? What is the likelihood of near-term and long-term success? And who will supply the solutions?

32.1 Nanometer Design: Place Your Bets

PANELISTS: Shekhar Borkar - *Intel Corp., Hillsboro, OR*
John Cohn - *IBM Microelectronics, Essex Junction, VT*
Antun Domic - *Synopsys, Inc., Mountain View, CA*
Patrick Groeneveld - *Magma Design Automation, Inc., Cupertino, CA*
Louis Scheffer - *Cadence Design Systems, Inc., San Jose, CA*
Jean-Pierre Schoellkopf - *STMicroelectronics, Crolles, Cedex, France*

Session 33

rm: 210CD

NOVEL SELF-TEST METHODS

CHAIR: Janusz Rajski - *Mentor Graphics Corp., Wilsonville, OR*

ORGANIZERS: Kwang-Ting Cheng, T. M. Mak

This session presents new self-test techniques for improving test quality and/or reducing overall test cost. The first paper employs the emerging software-based self-test approach to a modern embedded processor. The second and third papers devise new pattern generation schemes for BIST for higher test quality and lower hardware overhead. The fourth paper presents a logic BIST architecture with efficient generation, compression and application of test data. The last paper discusses a low-cost BIST method for linear analog circuits by reusing on-chip resources.

33.1 A Scalable Software-based Self-Test Methodology for Programmable Processors

Li Chen - *Univ. of California at San Diego, La Jolla, CA*
Srivaths Ravi, Anand Raghunathan - *NEC Corp., Princeton, NJ*
Sujit Dey - *Univ. of California at San Diego, La Jolla, CA*

33.2 A Scan BIST Generation Method using Markov Source and Partial Bit-Fixing

Wei Li, Chaowen Yu - *Univ. of Iowa, Iowa City, IA*
Irith Pomeranz - *Purdue Univ., West Lafayette, IN*
Sudhakar M. Reddy - *Univ. of Iowa, Iowa City, IA*

33.3 Seed Encoding with LFSRs and Cellular Automata

Ahmad A. Alyamani, Edward J. McCluskey - *Stanford Univ., Stanford, CA*

33.4 Efficient Compression and Application of Deterministic Patterns in a Logic BIST Architecture

Peter Wohl, John A. Waicukauski, Sanjay Patel, Minesh B. Amin - *Synopsys, Inc., Mountain View, CA*

33.5 Ultimate Low Cost Analog BIST

Marcelo Negreiros, Luigi Carro, Altamiro A. Susin - *UFRGS, Porto Alegre, Brazil*

Session 34

rm: 210AB

TECHNOLOGY MAPPING, BUFFERING, AND BUS DESIGN

CHAIR: John Lillis - *Univ. of Illinois, Chicago, IL*

ORGANIZERS: Charles J. Alpert, Dennis Sylvester, Raymond Nijssen

This session presents fundamental innovations in buffering and technology mapping. The first paper presents an industrial strength, comprehensive technique for technology mapping using logical effort theory. The second paper examines the van Ginneken's classic buffer insertion algorithm. It presents a sub-quadratic implementation of the classic work. The third paper presents analysis for bi-directional buses that illustrates that midway interleaving of repeaters is not optimium for delay and noise. Analysis leading to an asymmetric positioning is presented. Finally, the session concludes with a paper that uses novel digital filtering techniques to reduce crosstalk in high-speed package-level busses.

34.1 Gain-Based Technology Mapping for Discrete-size Cell Libraries

Bo Hu - *Univ. of California, Santa Barbara, CA*
Yosinori Watanabe - *Cadence Berkeley Labs., Berkeley, CA*
Alex Kondratyev - *Thesus Logic, Berkeley, CA,*
Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*

34.2 A Fast Algorithm for Optimal Buffer Insertion

Weiping Shi, Zhuo Li - *Texas A&M Univ., College Station, TX*

34.3 Optimum Positioning of Interleaved Repeaters in Bidirectional Buses

Maged M. Ghoneima, Yehea I. Ismail - *Northwestern Univ., Evanston, IL*

34.4 Synthesizing Optimal Filters for Crosstalk-Cancelation for High-Speed Buses

Jihong Ren, Mark R. Greenstreet - *Univ. of British Columbia, Vancouver, BC, Canada*

Session 35

rm: 209AB

COMPILATION TECHNIQUES FOR RECONFIGURABLE DEVICES

CHAIR: Ryan Kastner - *Univ. of California, Santa Barbara, CA*

ORGANIZERS: Jens Palsberg, Scott Hauck

Reconfigurable systems are driving new approaches to the compilation of hardware systems. This session brings together efforts in compilation and mapping for FPGAs and reconfigurable devices.

35.1 Fast Timing-driven Partitioning-based Placement For Island Style FPGA?s

Pongstorn Maidee, Cristinel Ababei, Kia Bazargan - *Univ. of Minnesota, Minneapolis, MN*

35.2 Global Resource Sharing for Synthesis of Control Data Flow Graphs on FPGAs

Seda Ogrenci Memik, Gokhan Memik - *Univ. of California, Los Angeles, CA*

35.3 Compiler-Generated Communication for Pipelined FPGA Applications

Heidi E. Ziegler, Mary Hall, Pedro Diniz - *Univ. of Southern California, Marina Del Rey, CA*

35.4 High-Level Data Communication Optimization for Reconfigurable Systems

Adam Kaplan, Ryan Kastner - *Univ. of California, Santa Barbara, CA*

Thursday June 5

8:30 to 10:00

All speakers are denoted in **bold**

S – denotes short paper

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Session 36

rm: Ballroom AB

ARCHITECTURAL POWER ESTIMATION AND OPTIMIZATION

CHAIR: Vijay Narayanan - *Penn State Univ., University Park, PA*
ORGANIZER: Chaitali Chakrabarti

Papers in this session present different solutions for architectural power estimation and optimization, involving clock-tree power minimization, issue-queue design in high-end microprocessor architectures and on-chip bus interface design.

36.1 Clock-Tree Power Optimization Based on RTL Clock-Gating

Monica Donno, Alessandro Ivaldi - *Politecnico di Torino, Torino, Italy*
Luca Benini - *Deis Univ. Di Bologna, Bologna, Italy*
Enrico Macii - *Politecnico di Torino, Torino, Italy*

36.2 Low-Power Design Methodology for an On-Chip Bus with Adaptive Bandwidth Capability

Rizwan Bashirullah - *North Carolina State Univ., Raleigh, NC*
Wentai Liu - *Univ. of California, Santa Cruz, CA*
Ralph Cavin - *Semiconductor Research Corp., Research Triangle Park, NC*

36.3s Power-Aware Issue Queue Design for Speculative Instructions

Tali Moreshet, Iris Bahar - *Brown Univ., Providence, RI*

36.4s State-Based Power Analysis for Systems-on-Chip

Reinaldo A. Bergamaschi - *IBM Corp., Yorktown Heights, NY*
Yunjian W. Jiang - *Univ. of California, Berkeley, CA*

Session 37

rm: 207A-D

PANEL: LIBRARIES: LIFEJACKET OR STRAITJACKET?

CHAIR: Carl Sechen - *Univ. of Washington, Seattle, WA*
ORGANIZERS: Chandu Visweswariah, Gerard Mas

The library abstraction in chip design is breaking down. Many trends are conspiring to necessitate a paradigm shift. The advent of transistor-level options such as multiple threshold voltage choices, availability of multiple oxide thicknesses and transistor sizes (including choices of beta ratios and taper ratios) is causing the sample space for library creation to explode. At the same time, diverse requirements such as ultimate performance, low power, and mixed analog/digital designs in SoCs require intelligent use of all these choices, to say nothing of multiple Vdd choices, high-voltage I/O cells, low-leakage sleep transistors and extremely dense embedded memories including 6T-SRAMs. Can sub-micron technologies continue to grow library size? Will we soon have libraries with 10,000 cells? Will tools and characterization methods cope? Will design methodologies be profoundly impacted? Is it the end of libraries as we know them?

37.1 The End of Libraries as We Know Them

PANELISTS: Barbara Chappel - *Intel Corp., Hillsboro, OR*
Jim Hogan - *Artisan Components, Inc., Sunnyvale, CA*
Andrew Moore - *TSMC, San Jose, CA*
Tadahiko Nakamura - *STARC, Yokohama, Japan*
Gregory Northrop - *IBM Corp., Yorktown Heights, NY*
Anjaneya Thakar - *Synopsys, Inc., Mountain View, CA*

Session 38

rm: 210CD

TECHNIQUES FOR RECONFIGURABLE LOGIC APPLICATIONS

CHAIR: Michael Butts - *Cadence Design Systems, Inc., Portland, OR*

ORGANIZERS: Majid Sarrafzadeh, Scott Hauck

By harnessing the reconfigurable nature of FPGA devices, new high-performance applications are possible, and new techniques are required to utilize these devices. In this session we bring together efforts on high-performance computation, and the precision analysis and fault tolerance techniques necessary to create them.

38.1 Designing Fault Tolerant Systems Into SRAM-based FPGAs

Fernanda G. Lima, Luigi Carro, Ricardo L. Reis - *UFRGS, Porto Alegre, Brazil*

38.2 Switch-Level Emulation

Ali Reza Ejlali, Seyed Ghassem Miremadi - *Sharif Univ. of Tech., Tehran, Iran*

38.3 Determining Appropriate Precisions for Signals In Fixed-Point IIR Filters

Joan E. Carletta, Robert Veillette, Frederick Krach, Zhengwei Fang - *Univ. of Akron, Akron, OH*

Session 39

rm: 210AB

TEST AND DIAGNOSIS FOR COMPLEX DESIGNS

CHAIR: Rathish Jayabharathi, - *Intel Corp., Folsom, CA*

ORGANIZERS: Seiji Kajihara, T. M. Mak

Designs are certainly getting more complex and not any simpler. Various aspects of testing and diagnosing these complex circuits are highlighted by the four papers in this session. The first paper discusses scan patterns application for designs with multiple clock domains. The second paper shows how to improve delay path diagnosis using statistical models. The third paper outlines a method by which internal bus protocols are checked in real time for new silicon. The last paper in the session proposes new ways to test FPGA interconnects.

39.1 Test Generation for Designs with Multiple Clocks

Xijiang Lin, Rob Thompson - *Mentor Graphics Corp., Wilsonville, OR*

39.2 Enhancing Diagnosis Resolution For Delay Defects Based Upon Statistical Timing and Statistical Fault Models

Angela Krstic, Li C. Wang, Kwang-Ting Cheng - *Univ. of California, Santa Barbara, CA,*
Jing Jia Liou - *National Tsing-Hua Univ., Hsinchu, Taiwan*
T. M. Mak - *Intel Corp., Santa Clara, CA*

39.3s Using Embedded Infrastructure IP for SOC Post-Silicon Verification

Yu Huang, Wutung Cheng - *Mentor Graphics Corp., Wilsonville, OR*

39.4s Using Satisfiability In Application Dependent Testing of FPGA Interconnects

Mehdi Baradaran Tahoori - *Stanford Univ., Stanford, CA*

Session 40

rm: 209AB

SPECIAL SESSION: HIGHLIGHTS OF ISSCC: HIGH-SPEED HETEROGENOUS DESIGN TECHNIQUES

CHAIR: Paul Zuchowski - *IBM Microelectronics, Essex Junction, VT*

ORGANIZERS: Limor Fix, Luciano Lavagno

The first paper describes how to apply the standing wave propagation technique to distribute 10GHz clocks with extremely low skew and jitter. The second paper is devoted to a self-biased PLL with wide multiplication range (1-4096) and extremely low period jitter. The third paper describes the architecture and implementation of a complex signal processing IC. The chip includes an embedded FLASH memory, as well as an embedded dynamically reconfigurable FPGA, usable both to extend the ISA of a micro-processor and as a stand-alone reconfigurable block.

40.1 10 GHz Clock Distribution using Coupled Standing-Wave Oscillators

F. O'Mahony, M. A. Horowitz, S. S. Wong - *Stanford Univ., Stanford, CA*
C. Patrick Yue - *Aeluros, Inc., Mountain View, CA*

40.2 Self-Biased High-Bandwidth Low-Jitter 1-to-4096 Multiplier Clock Generator PLL

J. Maneatis, J. Kim, I. McClatchie - *True Circuits, Inc., Los Altos, CA*
J. Maxey, M. Shankaradas - *Texas Instruments, Inc., Dallas, TX*

40.3 A 0.18um, 1GOPS Reconfigurable Signal Processing IC with Embedded FPGA and 1.2GB/s, 3-Port Flash Memory Subsystem

M. Borgatti, L. Cali, G. De Sandre, B. Foret, D. Iezzi, F. Lertora, G. Muzzi, M. Pasotti, M. Poles, P. L. Rolandi - *STMicroelectronics, Agrate Brianza, Italy*

Thursday June 5

10:30 to 12:00

All speakers are denoted in bold

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Session 41

rm: Ballroom AB

SPECIAL SESSION: HIGHLIGHTS OF ISSCC AND THE DESIGN OF STATE-OF-THE-ART MICROPROCESSORS

CHAIR: Noel Menezes - *Intel Corp., Hillsboro, OR*
ORGANIZERS: Limor Fix, Luciano Lavagno

The first paper describes the physical design methodology used to achieve timing closure for a 1.3GHz IBM microprocessor. The second paper describes the architectural and circuit techniques used to reduce power consumption in the design of a 1.5GHz Itanium processor. The third paper focuses on the protection of the circuitry from noise generated by radiation and EMI and on the clock circuitry design in a 1.5GHz SPARC64 processor.

41.1 Physical Synthesis Methodology for High Performance Microprocessors

Yiu Hing Chan - *IBM Corp., Poughkeepsie, NY*
Prabhakar Kudva, Gregory Northrop, Lisa B. Lacey - *IBM Corp., Yorktown Heights, NY*
Thomas Rosser - *IBM Corp., Austin, TX*

41.2 A Fifth Generation SPARC64 Microprocessor

Hisashige Ando, Yuuji Yoshida, Aiichiro Inoue, Itsumi Sugiyama, Takeo Asakawa, Kuniki Morita, Toshiyuki Muta, Tsuyoshi Motokurumada, Seishi Okada, Hideo Yamashita, Yoshihiko Satsukawa, Akihiko Konmoto, Ryouichi Yamashita, Hiroyuki Sugiyama - *Fujitsu Ltd., Kanagawa, Japan*

41.3 A 1.5GHz Third Generation Itanium® Processor

Jason Stinson, Stefan Rusu - *Intel Corp., Santa Clara, CA*

Session 42

rm: 207A-D

PANEL: FORMAL VERIFICATION: PROVE IT OR PITCH IT

CHAIR: Rajesh K. Gupta - *Univ. of California, San Diego, CA*
ORGANIZERS: Sandeep Shukla, Shishpal Rawat

As the complexity of chips rides up the Moore's law curve, so does the task of verifying them. Dynamic simulation continues to be critical in this task, but scales poorly. Simulation is time and resource expensive, and so is the cost of crucial bug escapes. For the past few decades, formal verification has held out the most promise. And yet, validation continues to consume most time and effort. Why is this so? Is there relief in sight? Will formal verification eliminate or limit unit level verification and provide the necessary glue for a realistic validation flow? Will the testbenches be replaced by constraints and assertions? Can they be? Can the process be automated? Can validation effort be reused? This panel will explore the issues related to building practical validation flows, and the technologies that the designer community can realistically look forward to materializing in their lifetimes.

PANELISTS: Brian Bailey - *Mentor Graphics Corp., Wilsonville, OR*
Dan Beece - *IBM Corp., Yorktown Heights, NY*
Masahiro Fujita - *Tokyo Univ., Tokyo, Japan*
Carl Pixley - *Synopsys, Inc., Hillsboro, OR*
John O'Leary - *Intel Corp., Hillsboro, OR*
Fabio Somenzi - *Univ. of Colorado, Boulder, CO*

Session 43

rm: 210CD

HIGH FREQUENCY INTERCONNECT MODELING

CHAIR: Charlie C. P. Chen - *Univ. of Wisconsin, Madison, WI*

ORGANIZERS: Bernard N. Sheehan, Byron L. Krauter

This session presents papers in the area of inductance modeling and transmission lines. The first paper presents algorithms used in FastImp, a program for the accurate analysis of wide-band electromagnetic effects in complicated geometries. The next paper develops an inductance extractor based on vector potential equivalent circuits. The third paper presents a design and modeling methodology for high performance transmission line devices. The session is rounded out by a paper on window-based susceptance extraction.

43.1 Algorithms in FastImp: A Fast and Wideband Impedance Extraction Program for Complicated 3-D Geometries

Zhenhai Zhu, Ben Song, Jacob White - *Massachusetts Institute of Tech., Cambridge, MA*

43.2 Vector Potential Equivalent Circuit Based on PEEC Inversion

Hao Yu, Lei He - *Univ. of California, Los Angeles, CA*

43.3s On-chip Interconnect-Aware Design and Modeling Methodology, Based on High Bandwidth Transmission Line Devices

David Goren, Michael Zelikson, Rachel Gordin, Israel A. Wagner - *IBM Haifa Reseach Lab., Haifa, Israel*

43.4s An Adaptive Window-Based Susceptance Extraction and Its Efficient Implementation

Guoan Zhong, Chengkok Koh, Venkataramanan R. Balakrishnan, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

Session 44

rm: 210AB

NOVEL APPROACHES IN TEST COST REDUCTION

CHAIR: Yervant Zorian - *Virage Logic, Fremont, CA*

ORGANIZERS: Erik Jan Marinissen, Seiji Kajihara

Larger ICs make test costs grow. Nanometer technologies require more tests and again make test costs grow. The papers in this session try to tackle these increasing test costs by reducing the test application time and test data volume.

44.1 Test Application Time and Volume Compression through Seed Overlapping

Wenjing Rao - *Univ. of California at San Diego, La Jolla, CA*

Ismet Bayraktaroglu - *Sun Microsystems, Sunnyvale, CA*

Alex Orailoglu - *Univ. of California at San Diego, La Jolla, CA*

44.2 Test Cost Reduction for SOCs Using Virtual TAMs and Lagrange Multipliers

Anuja Sehgal - *Duke Univ., Durham, NC*

Vikram Iyengar - *IBM Corp., Essex Junction, VT*

Mark D. Krasniewski, Krishnendu Chakrabarty - *Duke Univ., Durham, NC*

44.3s A Cost-Effective Scan Architecture for Scan Testing with Non-Scan Test Power and Test Application Cost

Dong Xiang, Shan Gu, Jia-guang Sun - *Tsinghua Univ., Beijing, China*

David Wu - *The Chinese Univ. of Hong Kong, Hong Kong, China*

44.4s On Test Data Compression and n-Detection Test Sets

Irith Pomeranz - *Purdue Univ., West Lafayette, IN*

Sudhakar M. Reddy - *Univ. of Iowa, Iowa City, IA*

Session 45

rm: 209AB

RETARGETABLE TOOLS FOR EMBEDDED SOFTWARE

CHAIR: Heinrich Meyr - *RWTH, Aachen, Germany*

ORGANIZERS: Anand Raghunathan, Lothar Thiele

The complexity of developing and maintaining embedded software tool flows, together with the increasing necessity to port them to new processors, is creating a push towards re-targetability. This session features advances that push the state-of-the-art towards the "holy grail" of re-targetable software tools - performance comparable to (or better than) manually written tools, with seamless re-configurability. The papers in this session focus on micro-architectural simulation, fast instruction-set simulation, and the synthesis of binary decoders that they contain.

45.1 A Retargetable Micro-Architecture Simulator

Wai Sum Mong, Jianwen Zhu - *Univ. of Toronto, Toronto, ON, Canada*

45.2 Instruction Set Compiled Simulation: A Technique for Fast and Flexible Instruction Set Simulation

Mehrdad Reshadi, Prabhat Mishra, Nikil Dutt - *Univ. of California, Irvine, CA*

45.3 Automated Synthesis of Efficient Binary Decoders for Retargetable Software Toolkits

Wei Qin, Sharad Malik - *Princeton Univ., Princeton, NJ*

Thursday
June 5

2:00
to
4:00

All speakers are denoted in **bold**

$ – denotes short paper

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Session 46

rm: Ballroom AB

SPECIAL SESSION: ASIC DESIGN IN NANOMETER ERA – DEAD OR ALIVE?

CHAIR: Nancy Nettleton - *Sun Microsystems, Palo Alto, CA*
ORGANIZERS: Abhijit Dharchoudhury, Sachin S. Sapatnekar

Cost pressures in nanometer technologies are forcing designers to push the limits of design technology to fully exploit increasingly complex and expensive technology capabilities. ASIC design and libraries must learn to deal with complex design rules, exploit a wide range of features, and contain increasing costs. In this session, the presenters describe the problems and solutions to various facets of mega-ASIC design in the nanometer era.

46.1 Designing Mega – ASICs In Nanotechnology

David Lackey, Juergen Koehl, Paul Zuchowski - *IBM Microelectronics, Essex Junction, VT*

46.2 Architecting ASIC Libraries and Flows In Nanometer Era

Clive Bittlestone, Anthony Hill - *Texas Instruments, Inc., Dallas, TX*
Vipul Singhal, Aravind NV - *Texas Instruments, Inc., Bangalore, India*

46.3 Pushing ASIC Performance In a Power Envelope

John Cohn - *IBM Microelectronics, Essex Junction, VT*
David Kung, Ruchir Puri, **Leon Stok**, - *IBM Corp., Yorktown Heights, NY*
Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*

46.4 Regular Fabrics to Optimize the Performance-Cost Trade-Off

Lawrence T. Pileggi, Herman Schmit, Andrzej Strojwas - *Carnegie Mellon Univ., Pittsburgh, PA*

Session 47

rm: 207A-D

FLOORPLANNING AND PLACEMENT

CHAIR: Carl Sechen - *Univ. of Washington, Seattle, WA*
ORGANIZERS: C. Y. Roger Chen, Ralph H.J.M. Otten

Two papers on placement and two papers on floorplanning comprise this session. The first placement paper describes a fast multigrid solver for analytical placement, providing significant speedups over the SOR method. The second paper describes a new clustering approach that takes estimated wire lengths into account, ultimately yielding better placements. The third paper describes a buffer allocation approach that is embedded in the inner loop of a floorplanner, rather than as a post-process, yielding considerably better results. The final paper presents a multi-level floorplanning framework based on a new representation termed MB*-trees.

47.1 An Algebraic Multigrid Solver for Analytical Placement with Layout Based Clustering

Hongyu Chen, Chung Kuan Cheng - *Univ. of California at San Diego, La Jolla, CA*
Nan Chi Chou - *Mentor Graphics Corp., San Jose, CA,*
Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*
John MacDonald - *Mentor Graphics Corp., San Diego, CA*
Bo Yao, Zhengyong Zhu - *Univ. of California at San Diego, La Jolla, CA*

47.2 Wire Length Prediction based Clustering and its Application in Placement

Bo Hu, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*

47.3 Dynamic Global Buffer Planning Optimization Based on Detail Block Locating and Congestion Analysis

Yuchun Ma, Xianlong Hong, Sheqin Dong, Yici Cai - *Tsinghua Univ., Beijing, China*
Chung-Kuan Cheng - *Univ. of California at San Diego, La Jolla, CA*
Jun Gu - *HKU of Science and Tech., Hong Kong, China*

47.4 Multilevel Floorplanning for Large-Scale Building-Block Design

Hsun Cheng Lee - *Synopsys, Inc., Taipei, Taiwan*
Jer Ming Hsu - *Center for High-Speed Computing, Hsinchu, Taiwan*
Yao Wen Chang - *National Taiwan Univ., Taipei, Taiwan*
Hannah H. Yang - *Intel Corp., Hillsboro, OR*

Session 48

rm: 210CD

ADVANCES IN SAT

CHAIR: Per Bjesse - *Synopsys, Inc., Hillsboro, OR*
ORGANIZERS: Karem A. Sakallah, Rajeev Ranjan

SAT technology has become a mainstream technology in design verification. The papers in this session report recent advances that extend the applicability of SAT techniques including — combining them with BDD based symbolic techniques, enhancing their expressivity by using pseudo-boolean constraints, extending their applicability to unbounded model checking, and leveraging symmetry to prune the search space.

48.1 Checking Satisfiability of a Conjunction of BDDs
Robert Damiano, James H. Kukula - *Synopsys, Inc., Hillsboro, OR*

48.2 Learning from BDDs in SAT-based Bounded Model Checking
Aarti Gupta, Malay Ganai - *NEC Corp., Princeton, NJ*
Chao Wang - *Univ. of Colorado, Boulder, CO*
Zijiang Yang, Pranav N. Ashar - *NEC Corp., Princeton, NJ*

48.3 A Fast Pseudo-Boolean Constraint Solver
Donald Chai - *Univ. of California, Berkeley, CA*
Andreas Kuehlmann - *Cadence Berkeley Labs., Berkeley, CA*

48.4s Shatter: Efficient Symmetry-Breaking for Boolean Satisfiability
Fadi A. Aloul, Igor L. Markov, Karem A. Sakallah - *Univ. of Michigan, Ann Arbor, MI*

48.5s SAT-Based Unbounded Symbolic Model Checking
Hyeong Ju Kang, In-Cheol Park - *KAIST, Daejeon, Republic of Korea*

Session 49

rm: 210AB

NOVEL DESIGN METHODOLOGIES AND SIGNAL INTEGRITY

CHAIR: Sharad Mehrotra - *Sun Microsystems, Austin, TX*
ORGANIZERS: Abhijit Dharchoudhury, Noel Menezes

Interconnect delay dominance and crosscoupling require novel design methodologies and signal integrity techniques to ensure rapid design convergence. The first two papers describe the management of a large ASIC design and a novel way to increase performance in a hierarchical ASIC design methodology, respectively. The third paper discusses the estimation of power grid voltage droops due to statistical leakage current variations. The fourth and fifth papers discuss two topics in noise analysis: the removal of noise pessimism by considering functional relationships and the propagation of noise windows.

49.1 Design of a 17-million Gate Network Processor using a Design Factory
Gilles Eric Descamps, Satish Bagalkotkar, Subramanian Ganesan, Satish Iyengar, Alain Pirson - *Silicon Access Networks, San Jose, CA*

49.2 Hybrid Hierarchical Timing Closure Methodology for a High Performance and Low Power DSP
Kaijian Shi - *Synopsys, Inc., Dallas, TX*
Craig Godwin - *Texas Instruments, Inc., Dallas, TX*

49.3s Statistical Estimation of Leakage-Induced Power Grid Voltage Drop Considering Within-Die Process Variations
Imad A. Ferzli, Farid N. Najm - *Univ. of Toronto, Toronto, ON, Canada*

49.4s Temporofunctional Crosstalk Noise Analysis
Donald Chai - *Univ. of California, Berkeley, CA*
Alex Kondratyev - *Thesus Logic, Berkeley, CA*
Yajun Ran - *Univ. of California, Santa Barbara, CA*
Kenneth H. Tseng - *Cadence Design Systems, Inc., San Jose, CA*
Yosinori Watanabe - *Cadence Berkeley Labs., Berkeley, CA*

49.5 Static Noise Analysis with Noise Windows
Kenneth H. Tseng, Vinod Kariat - *Cadence Design Systems, Inc., San Jose, CA*

Session 50

rm: 209AB

MEMORY OPTIMIZATION FOR EMBEDDED SYSTEMS

CHAIR: Marcello Lajolo - *NEC Corp., Princeton, NJ*
ORGANIZER: Anand Raghunathan

Memory is a bottleneck to achieving higher performance and lower power consumption for many embedded systems. This session presents new approaches to improve the behavior of embedded software by optimizing all parts of the memory sub-system - caches, on-chip memory, and off-chip (DRAM) memory. Presentations will cover topics including smart memories that contain computation capability, optimizing cache behavior through cache architecture and data layout in memory, and techniques to exploit off-chip DRAM access modes.

50.1 Intelligent SRAM (ISRAM) for Improved Embedded System Performance
Prabhat Jain, Edward Suh, Srinivas Devadas - *Massachusetts Institute of Tech., Cambridge, MA*

50.2 Improved Indexing for Cache Miss Reduction in Embedded Systems
Tony Givargis - *Univ. of California, Irvine, CA*

50.3 Memory Layout Technique for Variables Utilizing Efficient DRAM Access Modes in Embedded System Design
Yoonseo Choi, Taewhan Kim - *KAIST, Daejon, Republic of Korea*

50.4 Interprocedural Optimizations for Improving Data Cache Performance of Array-Intensive Embedded Applications
Wei Zhang, Guangyu Chen, Mahmut Kandemir - *Penn State Univ., University Park, PA*
Mustafa Karakoy - *Imperial College, London, UK*

Thursday
June 5

4:30
to
6:00

All speakers are denoted in **bold**

S – denotes short paper

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Session 51

rm: Ballroom AB

SPECIAL SESSION: DESIGN AUTOMATION FOR QUANTUM CIRCUITS

CHAIR: Andreas Kuehlmann - *Cadence Berkeley Labs., Berkeley, CA*
ORGANIZER: Soha Hassoun

Modern quantum computing is considered a next frontier in computing. The first paper of this session is an hour-long tutorial that introduces elementary gates for quantum computation, technology-independent quantum logic and quantum design automation. Physical implementation issues and recent experimental results will be discussed. The second paper covers quantum algorithms with an emphasis on small-scale, easily implementable examples and ROM-based computation. The third paper discusses the Quantum Information Science and Technology Roadmapping Project.

51.1 Tutorial: Basic Concepts in Quantum Circuits
John P. Hayes - *Univ. of Michigan, Ann Arbor, MI*

51.2 Designing and Implementing Small Quantum Circuits and Algorithms
Ben C. Travaglione - *Univ. of Cambridge Computer Lab., Cambridge, UK*

51.3 A Technology Roadmap for Quantum Computing and Communications
Richard J. Hughes - *Los Alamos National Lab., Los Alamos, NM*

Session 52

rm: 207A-D

ENERGY-AWARE SYSTEM DESIGN

CHAIR: Sujit Dey - *Univ. of California at San Diego, La Jolla, CA*
ORGANIZERS: Kaushik Roy, Luca Benini

The first two papers of the session are on energy-aware on-chip and off-chip communication system design. The last two papers address practical design and implementation issues for energy-aware systems for wireless and multi-media applications.

52.1 A Survey of Techniques for Energy Efficient On-Chip Communication
Vijay Raghunathan, Mani B. Srivastava - *Univ. of California, Los Angeles, CA*

52.2 Extending the Lifetime of a Network of Battery-Powered Mobile Devices by Remote Processing: A Markovian Decision-Based Approach
Peng Rong, Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

52.3s Energy-Aware MPEG-4 FGS Streaming
Kihwan Choi - *Univ. of Southern California, Los Angeles, CA*
Kwanho Kim - *Seoul National Univ., Seoul, South Korea*
Peng Rong, Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

52.4s STUDENT DESIGN CONTEST: A Low-Energy Chip-Set for Wireless Intercom
Josie Ammer, Michael Sheets, Tufan C. Karalar, Mika Kuulusa, Jan Rabaey - *Univ. of California, Berkeley, CA*

Session 53

rm: 210CD

BUDGETING, SIMULATION AND STATISTICAL TIMING

CHAIR: Krishna Belkhale - *Cadence Design Systems, Inc.,*
ORGANIZERS: Kenneth L. Shepard, Sudhakar Bobba

This session covers various aspects of budgeting, high-level simulation and statistical timing analysis. It begins with a paper on novel delay budgeting using integer programming techniques. The second paper is focused on the principles behind a simulator that obtains the performance of SystemC without sacrificing re-usability. Finally, the third paper describes a path-based statistical static timer that takes all sources of correlations into account.

53.1 Optimal Integer Delay Budgeting on Directed Acyclic Graphs

Elaheh Bozorgzadeh, Soheil Ghiasi - *Univ. of California, Los Angeles, CA*
Atsushi Takahashi - *Tokyo Institute of Tech., Tokyo, Japan*
Majid Sarrafzadeh - *Univ. of California, Los Angeles, CA*

53.2 Optimizations for a Simulator Construction System Supporting Reusable Components

David A. Penry, David I. August - *Princeton Univ., Princeton, NJ*

53.3 Statistical Timing for Parametric Yield Prediction of Digital Integrated Circuits

Jochen A. G. Jess - *Eindhoven Univ. of Tech., Eindhoven, The Netherlands*
Kerim Kalafala - *IBM Corp., Hopewell Junction, NY*
Srinath R. Naidu, Ralph H.J.M. Otten - *Eindhoven Univ. of Tech., Eindhoven, The Netherlands*
Chandu Visweswariah - *IBM Corp., Yorktown Heights, NY*

Session 54

rm: 210AB

INTERCONNECT NOISE AVOIDANCE METHODOLOGIES AND SLEW RATE PREDICTION

CHAIR: Sani R. Nassif - *IBM Corp., Austin, TX*
ORGANIZERS: Byron L. Krauter, Sachin S. Sapatnekar

This session is focused on interconnect behavior and noise avoidance. The first paper provides a pragmatic overview of the Pentium 4 interconnect and noise immunity design. The second paper examines the applicability of novel and well known noise reduction techniques in FPGAs. The third paper proposes simple metrics for RC slew rate based on two circuit moments. The final paper provides a methodology for sizing gates taking into account crosstalk.

54.1 Interconnect and Noise Immunity Design for the Pentium 4 processor

Rajesh Kumar - *Intel Corp., Portland, OR*

54.2 Crosstalk Noise in FPGAs

Yajun Ran, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*

54.3s Simple Metrics for Slew Rate of RC Circuits Based on Two Circuit Moments

Kanak B. Agarwal, Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

54.4s Post-Route Gate Sizing for Crosstalk Noise Reduction

Murat R. Becer - *Motorola, Inc., Austin, TX*
David Blaauw - *Univ. of Michigan, Ann Arbor, MI*
Ilan Algor - *Motorola, Inc., Herzelia, Israel*
Vladimir Zolotov, Chanhee Oh, Rajendran Panda - *Motorola, Inc., Austin, TX*

Session 55

rm: 209AB

ANALOG DESIGN SPACE EXPLORATION

CHAIR: Richard Shi - *Univ. of Washington, Seattle, WA*
ORGANIZER: Georges G. Gielen

Performance space exploration for analog circuits is an important technique for design and synthesis. The papers present novel contributions in this area, including performance trade-off analysis, use of support vector machines and geometric convex modeling. The final paper applies performance space modeling for architectural selection of data converters.

55.1 Performance Trade-off Analysis of Analog Circuits By Normal-Boundary Intersection

Guido Stehr, Helmut Graeb, Kurt Antreich - *Technical Univ. of Munich, Munich, Germany*

55.2 Support Vector Machines for Analog Circuit Performance Representation

Fernando De Bernardinis, Michael Jordan, Alberto L. Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

55.3s Efficient Description of the Design Space of Analog Circuits

Mar Hershenson - *Barcelona Design, Inc., Newark, CT*

55.4s Architectural Selection of A/D Converters

Martin Vogels, Georges G. Gielen - *Katholieke Univ., Leuven, Belgium*

Monday/Friday Tutorials 9:00 AM - 5:00 PM

(breakfast and lunch included in tutorial fee)

Monday, June 2, 2003 • 9:00 AM - 5:00 PM

TUTORIAL 1 - DESIGN TECHNIQUES FOR POWER REDUCTION

Rm: 210AB

ORGANIZER: Borivoje Nikolic - *Univ. of California, Berkeley, CA*
PRESENTERS: Tom Burd - *Consultant, Berkeley, CA*
Tadahiro Kuroda - *Keio Univ., Yokohama, Japan*
Renu Mehra - *Synopsys, Inc., Mountain View, CA*
Borivoje Nikolic - *Univ. of California, Berkeley, CA*

Audience: Designers and engineering managers. Circuit designers and digital system designers who are facing the problems of power-limited designs.

Description: This full-day tutorial covers techniques for reducing active and standby power consumption in desktop and portable devices. Increased number of designers today are facing the power dissipation limitations while still being required to deliver increased performance. The tutorial covers the fundamentals of dynamic and static power consumption, and presents the methods for their reduction in fixed and variable throughput systems across various levels of design hierarachy. The key topics in power reduction under throughput constraints are discussed, compared and contrasted: gate sizing, supply voltage and transistor threshold voltage optimization for dynamic power and active leakage reduction, including the use of multiple transistor thresholds and multiple supply voltages. The tutorial, furthermore, discusses the standby current control using clock gating, power rail cut-off and back-biasing. As for the variable throughput systems, the topics of energy reduction through dynamic voltage scaling and transistor back biasing and optimal scheduling for variable throughput are covered. Special attention is paid to discussion of capabilities and limitations of existing tools for power analysis and optimization.

Friday, June 6, 2003 • 9:00 AM - 5:00 PM

TUTORIAL 2 - SYSTEM-ON-CHIP TEST STRATEGIES

Rm: 205AB

ORGANIZER: Yervant Zorian - *Virage Logic, Fremont, CA*
PRESENTERS: Kwang-Ting Cheng - *Univ. of California, Santa Barbara, CA*
Erik Jan Marinissen - *Philips Research Labs., Eindhoven, The Netherlands*
Yervant Zorian - *Virage Logic, Fremont, CA*

Audience: IC designers, system architects, test and DFT engineers, and their managers, researchers, test methodology developers, and test automation tool developers.

Description: Advances in semiconductor technology enable the design and manufacturing of complex systems-on-chip. For the manufacturing test of such SoCs, we are faced with a "double-whammy" due to the increase in chip complexity on the one hand, and the emergence of new failure mechanisms in nanometer technologies on the other hand. While SoC design complexity is being combated by technologies such as IP core-based design and system-level design, the traditional "over-the-wall" approach to test, and conventional test methods threaten to break down, resulting in the test cost-per-transistor becoming comparable to, or perhaps even exceeding, the manufacturing cost.
This tutorial presents the state-of-the-art in system-level integration and addresses the challenges related to test and diagnosis of system-on-chip. Then, it highlights a range of cores-based test and diagnosis methods for embedded logic, memory, processor and analog cores. This tutorial, then concentrates on the strategies for testing the overall system-on-chip and the need for test access mechanisms. It also summarizes the role and status of industry wide standardization efforts, namely the IEEE P1500 standard for embedded core test. Finally, it demonstrates a range of current industrial experiences and future research trends in the domain of system-on-chip test.

Friday Tutorials 9:00 AM - 5:00 PM

(breakfast and lunch included in tutorial fee)

Friday, June 6, 2003 • 9:00 AM - 5:00 PM

TUTORIAL 3 - DESIGN FOR MANUFACTURING IN THE SUB-100NM ERA

Rm: 207A-D

ORGANIZER: Louis Scheffer - *Cadence Design Systems, Inc., San Jose, CA*

PRESENTERS: David Blaauw - *Univ. of Michigan, Ann Arbor, MI*
Sani Nassif - *IBM Research Division, Austin, TX*
Louis Scheffer - *Cadence Design Systems, Inc., San Jose, CA*
Andrzej Strojwas - *Carnegie Mellon Univ. Pittsburgh, PA/ PDF Solutions, Inc., San Jose, CA*

Audience: This tutorial is intended for designers, EDA developers, and researchers who are relatively familiar with today's design flows, but want to understand the techniques, tools and flows that will be required to build manufacturable chips in sub-100nm processes.

Description: Modern processes (100nm and below) require extra attention to ensure that designs are manufacturable with acceptable yield, in addition to the traditional problem of logical and physical correctness. Yield losses in these processes include functional defects, performance problems, excessive leakage, and problems with testing. Designers and tool developers need to understand each of these sources of yield loss, and devise ways to minimize their impact. This tutorial will describe in detail the problems unique to, or exaggerated by, very small devices and interconnect. These include increased process variability, increased leakage, increased electrical noise, new requirements for resolution enhancement techniques such as OPC and PSM, and new yield loss mechanisms. It will then cover various techniques that can be used to mitigate these problems. These include measurement and characterization of process variation (leading to design centering), statistical timing, yield estimation and modeling, analysis and minimization of electrical noise, OPC aware placement and routing, leakage minimization, and provisions for Iddq testing in the presence of leakage.

Friday, June 6, 2003 • 9:00 AM - 5:00 PM

TUTORIAL 4 - ASSERTION-BASED VERIFICATION

Rm: 209AB

ORGANIZER: Erich Marschner - *Cadence Design Systems, Inc., Columbia, MD*

PRESENTERS: Samuel Dellacherie - *TNI-Valiosys, Hérouville St Clair, France*
Harry Foster - *Verplex Systems, Inc., Dallas, TX*
Erich Marschner - *Cadence Design Systems, Inc., Columbia, MD*
Sitvanit Ruah - *IBM Haifa Research Lab., Haifa, Israel*
Sean Smith - *Cisco Systems, Inc., Research Triangle Park, NC*

Audience: The tutorial is intended for designers, verification engineers, and engineers responsible for verification methodologies, who want to accelerate the detection and elimination of errors during design verification.

Description: This tutorial presents assertion-based verification using the Accellera Property Specification Language (PSL), an emerging industry standard, based on IBM's Sugar 2.0 assertion language.

We begin with the general concept of assertions and an overview of various languages that have been used to express assertions. Next, we introduce PSL/Sugar. We review the temporal logic concepts upon which PSL/Sugar is based, and we present the rich layered structure of the language, in particular the layer which supports temporal assertions based on linear temporal logic (LTL).

Next, we present a methodology for applying assertions, including use of assertions for interface checking, constraint specification, internal consistency checking, and coverage monitoring, using PSL/Sugar as a vehicle to illustrate the concepts. We discuss how assertions can be used in a wide range of verification flows including static analysis, simulation, emulation, and test generation.

Next, we review developing support for PSL/Sugar in EDA tools and describe how PSL/Sugar enables an assertion-based methodology built upon interoperable tools. We demonstrate the use of assertions through assertion-based verification of a small design example. We finish with a summary of experience with the use of assertions at Cisco Systems.

Friday Tutorials 9:00 AM - 5:00 PM

(breakfast and lunch included in tutorial fee)

Friday, June 6, 2003 • 9:00 AM - 5:00 PM

TUTORIAL 5 - ASSEMBLING AN SOC: COMMUNICATION ARCHITECTURES AND PROTOCOLS

Rm: 210AB

ORGANIZER: Giovanni De Micheli - *Stanford Univ., Stanford, CA*
PRESENTERS: Luca Benini - *Univ. of Bologna, Bologna, Italy*
Giovanni De Micheli - *Stanford Univ., Stanford, CA*
Kees Goossens - *Philips Research Labs., Eindhoven, The Netherlands*
Eric Verhulst - *Eonic Systems, Ulm, Germany*

Audience: This tutorial is of interest to R&D engineers and managers involved with VLSI and System on Chip design, who are specifically interested in future technology and design trends.

Description: On-chip networks, also called micro-networks, are receiving increasingly higher attention as means to solving interconnect design problems, within a communication-centric approach to Systems on Chip (SoC) design. Techniques borrowed from the network field are evaluated on the basis of their potentials for providing on-chip high performance solutions, that satisfy quality of service (QoS) requirements under the limitations of unreliable signal transmission and non-negligible communication delays on wires. Such limitations will be typical of forthcoming nanometer-scale technologies.
We will survey several topics. We consider first the problems arising in using advanced submicron technologies for SoC communication. We will review the fundamental techniques in networking, ranging from a comparative study of network architectures to the design of control protocols. We explain how networking techniques can be used for SoC interconnect design, and we present critically some research and development work done in this area at various sites. We describe the network aspects from a software standpoint, ranging from middlewaredesign to programming models. Finally we conclude with existing examples of SoCs that support on chip micro-networks.

Friday, June 6, 2003 • 9:00 AM - 5:00 PM

TUTORIAL 6 - HIGH PERFORMANCE ASIC DESIGN

Rm: 210CD

ORGANIZERS: Kurt Keutzer - *Univ. of California, Berkeley, CA*
David Chinnery - *Univ. of California, Berkeley, CA*
PRESENTERS: Razak Hossain - *STMicroelectronics Inc., San Diego, CA*
Michael Keating - *Synopsys Inc., Mountain View, CA*
Kurt Keutzer - *Univ. of California, Berkeley, CA*
Earl Killian - *Tensilica, Inc., Santa Clara, CA*
Jagesh Sanghavi - *Tensilica, Inc., Santa Clara, CA*

Audience: This tutorial is intended for ASIC designers seeking higher performance, custom designers seeking higher productivity, EDA tool developers, and EDA researchers.

Description: The focus of this tutorial is on actual industrial applications of high-performance ASIC design methodologies. While it is traditionally held that the principal performance advantage of custom designed circuits comes from detailed custom-layout techniques, this tutorial begins by showing the true contributing factors behind custom performance: microarchitecture, clocking methodology, cell sizing, and exploiting semiconductor processing. In this tutorial we elaborate on each of these aspects. Earl Killian will share his experience on developing high-performance micro-architectures. Michael Keating will discuss Synopsys and ARM's experience migrating the ARM from a full custom design to a synthesizable ASIC design with comparable performance. Razak Hossain overviews techniques used to achieve very high performance (520MHz in 0.18um) in an ASIC microprocessor. Jagesh Sanghavi highlights putting together an entire high-performance EDA design flow, and how different options for a configurable processor can impact the speed.

Introduction to Chips and EDA for a Non-Technical Audience

Monday, June 2, 2003 • 10:00 AM - 12:00 PM

Room: 209AB

ORGANIZER/SPEAKER: Karen Bartleson, Synopsys, Inc., Mountain View, CA

This workshop provides:

- A simplified explanation for the layman of how chips are made
- A portrayal of chip design using Electronic Design Automation
- An opportunity to see and touch the parts that make up chips and electronic products
- A non-threatening, fun event with a basic, working knowledge to take away

This workshop is for:

- Non-engineering staff from technology companies
- Analysts and media people unfamiliar with EDA and semiconductor industries
- Educators and students who are curious about chip technology

Tutorial Objectives:

- Provide a basic understanding of EDA and semiconductors to non-technical people
- Present information in simple, easy-to-understand terms
- Use hands-on parts (wafers, chips, masks...) for an enhanced experience
- Encourage people to join the EDA industry
- Promote the EDA industry as a good financial investment
- Address ongoing requests to help non-technical people understand the EDA industry

Please note:

This workshop is the same one presented at DAC 2002.

The workshop is for non-technical attendees.

Maximum class size: 50

REGISTRATION INSTRUCTIONS:

No Conference Registration is required.

$10.00 Registration Fee

The 40th Design Automation Conference • June 2 - 6, 2003 • Anaheim, CA

Workshop for Women in Design Automation Monday, June 2, 2003 • 1:00 PM - 5:00 PM

Would Life be Different if Risk Were Not a Factor? Managing, Life & Career Transition

WORKSHOP CHAIR: Sonja Wilkerson, *VP of Human Resourses, Vitria Technology, Inc.*

This unique program has continued to grow each year and affords the opportunity to hear successful women speak on topics relevant to their careers. It also gives participants a chance to network with their peers and engage in an exchange of views and ideas which foster growth.

Mission Statement: To be a workshop of relevance to women in Electronic Design Automation, to providing a forum for the interchange of ideas for successful careers in the EDA profession, to address the particular needs of professional women and to provide an opportunity for peer networking.

SCHEDULE:

1:00 PM - 2:00 PM Registration and buffet lunch
2:00 P M - 3:45 P M Keynote Address and Panel
3:45 P M - 4:15 P M Achievement Award Ceremony:
Join us as we honor the recipient of this year's Marie R. Pistilli Women in EDA Achievement Award.
4:15 P M Cocktail Reception:
Sponsored by the EDA Consortium

ORGANIZERS: **Karla Reynolds** - Mgr., IBM Foundry Enablement, IBM Microelectronics
Ann Marie Rincon - Engineering Fellow, AMI Semiconductor
Telle Whitney - President and CEO, Institute for Women and Technology

STEERING COMMITTEE: **Nanette Collins** - *Publicity Chair, 40th DAC*
Marie R. Pistilli - *Co-Chair, Board of Directors, MP Associates, Inc.*
Jan Willis - *VP of Business Development, Cadence Design Systems, Inc.*

Keynote Address Penny Herscher
VP and Chief Marketing Officer, Cadence Design Systems, Inc.
Penny Herscher joined Cadence through its acquisition of Simplex Solutions, Inc., where she was Chairman and CEO. At Cadence, Penny is responsible for marketing, strategy, customer support, and design services. Before joining Simplex, Penny was a Vice President and General Manager at Synopsys. Prior to joining Synopsys, Penny held R&D and Product Marketing positions at Daisy Systems. She began her career as an R&D engineer at Texas Instruments. Penny holds a B.A. with honors in mathematics from Cambridge University in England, and sits on the board of the Entrepreneurs Foundation.

Panel: Transition and Change: How Do I Successfully Navigate My Career Through Turbulent Times?

Moderator: Denise Brouillette - *The Innovative Edge*

Don't miss the opportunity to learn how prominent professionals in the industry have made career choices to achieve a rewarding personal and professional life experience.

Vicki Andrews - *Synopsys, Inc.*
Tsugumi Fujitani - *Nihon Tera Systems, K.K.*
Pat McCarty - *Cadence Design Systems, Inc.*
Ann Marie Rincon - *AMI Semiconductor*
Telle Whitney - *Institute for Women and Technology*

Room: 205AB

REGISTRATION INSTRUCTIONS:
No Conference Registration is required.

$50.00 *ACM/IEEE Members*
$75.00 *Non-Members*

tion

Interoperability Workshop — Monday, June 2, 2003 • 12:00 PM – 5:00 PM

This year DAC will host the fourth Workshop on Interoperability, a subject of perpetual and passionate interest. Since the first meeting in 2000 there has been remarkable progress. There is now the Open Access coalition of 16 companies promoting an open standard API and open source data base, based on a contribution from Cadence. Recently, Synopsys announced their plans to open the Milkyway data base and their interest in a common API. Can multi-vendor interoperability be far away? The Workshop will consist of a brief update on these efforts followed by two sessions on how these efforts address the interoperability challenges facing the electronics industry, and close with a Panel discussion open to your questions.

ORGANIZERS: Terry Blanchard - *Dir. of EDA, Hewlett-Packard Co.*
John Darringer - *Mgr. System-Design, IBM Research*
Greg Spirakis - *VP Design Technology, Intel Corp.*

Room: 210CD

REGISTRATION INSTRUCTIONS:
No Conference Registration is required.

$50.00 *ACM/IEEE Members*
$75.00 *Non-Members*

SCHEDULE:

12:00 PM Lunch
1:00 PM Welcome: John Darringer - *Mgr. System-Design, IBM Research*
1:05 PM Open Access Coalition - Scott Peterson - *OAC Chair and Dir. Silicon Optimization, LSI Logic Corp.*
1:15 PM Open Access Development Status and Plans - Joe Santos - *Open Access Development Manager, Cadence Design Systems, Inc.*
1:30 PM Open Milkyway Status and Plans - Rich Goldman - *VP Strategic Market Development, Synopsys, Inc.*
1:45 PM Bridging and API Convergence Status and Plans
- Jim Wilmore - *Chair Golden Gate Working Group and CAD System Architect, Hewlett Packard Co.*
1:55 PM The User View - How Can We Tightly-Couple Tools from Different Suppliers?
Chair: Greg Spirakis - *Mgr. Design Technology, Intel Corp.*
John Fields - *VP Design Platform Org., Agere Systems, Inc.*
Rick Ferreri - *CAD System Architect, Hewlett Packard Co.*
Dale Hoffman - *Dir. EDA Alliances, IBM Corp.*
Philippe Magarshack - *Central R&D Group VP, Design Automation, STMicroelectronics*
2:35 PM BreaK
2:50 PM Future Interoperability Directions Chair: Terry Blanchard - *Dir. of EDA, Hewlett-Packard Co.*
- Verification Needs and Directions - Harry Foster - *Chief Architect, Verplex Systems, Inc.*
- Mixed Signal Needs and Directions - Jack Hurt - *Fellow, Tektronix*
- Design for Manufacturing Needs and Directions - Aki Fujimura - *VP R&D, Cadence Design Systems, Inc.*
- Mask Tool Supplier Perspective - Tom Grebinski - *Chair, SEMI Data Path Task Force*
- University Needs and Directions - Andrew B. Kahng - *Professor, Univ. of California at San Diego, La Jolla, CA*
- Potential for API Convergence - Raul Camposano - *Sr.VP and CTO, Synopsys, Inc.*
4:00 PM Panel - How Can We Achieve True Multi-Vendor Interoperability? Chair: Richard Goering - *Editor, EE Times*
- Panelists selected from speakers above
5:00 PM Adjourn

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Berkeley, CA

Technical Program Co-Chair, Design Methods
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Delft, The Netherlands

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Tucson, AZ

Jacob White
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of Tech.
Cambridge, MA

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Mentor Graphics Co.
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Essex Junction, VT

Deirdre Hanford
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Mountain View, CA

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CoWare, Inc.
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Gerard Mas
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Crolles Cedex, France

Shishpal S. Rawat
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Folsom, CA

Rob A. Rutenbar
Carnegie Mellon Univ.
Pittsburgh, PA

Kazuo Yano
Hitachi Central
Research Lab.
Tokyo, Japan

Exhibitor Liaison Committee/Student Design Contest Judges

Exhibitor Liaison Committee

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Cadence Design Systems, Inc.
San Jose, CA

Nanette Collins
Boston, MA

Larry Eberle
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Ian Getreu
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EDN Worldwide/
Reed Electronics Grp.
Venice, FL

Steve Pollock
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San Jose, CA

Mindy Powers
CoWare, Inc.
San Jose, CA

Lee Wood
MP Associates, Inc.
Boulder, CO

DAC/ISSCC Student Design Contest

DAC/ISSCC SDC Co-Chairs

David Greehill
Sun Microsystems
Sunnyvale, CA

Steve Levitan
Univ. of Pittsburgh
Pittsburgh, PA

Alan Mantooth
Univ. of Arkansas
Fayetteville, AR

DAC/ISSCC SDC Judges

Shane Bell
Intel Corp.
Shrewsbury, MA

Charles Chen
Univ. of Wisconsin
Madison, WI

James Goodman
Engim Canada, Inc.
Ottawa, ON Canada

Payam Heydari
Univ. of California
Irvine, CA

Rhonday Kay Gaede
Univ. of Alabama
Huntsville, AL

John Lockwood
Washington Univ.
St. Louis, MO

John Long
Delft Univ. of Tech.
Delft, The Netherlands

Grant E. Martin
Cadence Berkeley Labs.
Berkeley, CA

Siva G. Narendra
Intel Labs.
Hillsboro, OR

Patrick R. Shultz
Univ. of Mannheim
Mannheim, Germany

Kenneth Yang
Univ. of California
Los Angeles, CA

Additional Meetings

DAC/ISSCC Student Design Contest

The purpose of the Student Design Contest is to promote excellence in the design of electronic systems by providing competition between graduate and undergraduate students at universities and colleges. This year we received over 50 submissions in two categories: "Conceptual" and "Operational". Operational designs are those which have been implemented and tested. Conceptual designs have not yet been fabricated and tested but must have been thoroughly simulated. Students compete for cash prizes donated by a number of industrial sponsors, as well as the conference. Prize winners will be listed in the final program and have been invited to show their work at the University Booth on the show floor. Awards will be given at the Pavilion, on Tuesday, June 3, 2003 from 11:30 AM - 12:00 PM. In addition, three of the submissions have been included in this year's technical program (see pages 15, 26, and 34).

VSI Alliance

Do We Need SoC Standards?

Wednesday, June 4, 2003 at the Anaheim Convention Center

VSI Alliance (VSIA) will host a compelling panel of Industry and standards organization experts who will explore the "whats" and "hows" of SoC standards adoption. VSIA's much anticipated IP Quality Metric and revitalization plans will also be unveiled.

CODES ISSS 2003

CODES ISSS Program Committee Meeting will be held Monday, June 2, 2003, from 8:00 AM - 2:00 PM in the Anaheim Convention Center.

Birds-of-a-Feather (BOF) Meetings

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather". All BOF meetings are held at the Anaheim Convention Center, Wednesday, June 4, 2003, 6:30 PM - 8:00 PM. DAC will facilitate common interest group meetings to discuss DA related topics. To arrange a BOF meeting contact the DAC office at mpa@dac.com or sign up at the Information Desk at-conference. A room will only be assigned if ten or more people sign up. An overhead projector and screen will be provided on request. Check DACnet and the Birds-of-a-Feather board at the Information Desk.

SIGDA Ph.D. Forum

ACM/SIGDA will hold an open member meeting on Tuesday evening, June 3, 2003, from 6:30 PM to 9:00 PM in room 213A-C. SIGDA members are invited, as are all members of the EDA community. A buffet dinner will be served at 7:00 PM.

There will be a brief presentation on SIGDA's programs, but the main focus of the meeting will be the Ph.D. Forum. Aimed at strengthening the ties between academia and industry, students will present posters and discuss their Ph.D. dissertation research with interested attendees. The Ph.D. Forum gives the students feedback on their research, and gives the DA community a preview of work in progress. For more information, see http://www.sigda.org/programs.php.

Exhibitor List

Company

@HDL Inc.
0-In Design Automation
ACE Associated Compiler Experts bv
Acreo Socware Center
Agilent Technologies
Alba Centre (The)
Aldec, Inc.
Alternative System Concepts, Inc.
AmmoCore Technology
Anadigm, Inc.
Analog Design Automation
Anasift Technology Inc.
Ansoft Corp.
Apache Design Solutions, Inc.
Apex Design Systems, Inc.
Applied Simulation Technology
Applied Wave Research, Inc.
Aptix Corp.
Archelon Inc.
Arrow's Global Information Business
Artisan Components, Inc.
Artwork Conversion Software, Inc.
Atrenta Inc.
austriamicrosystems USA, Inc.
Avery Design Systems
Axis Systems, Inc.
AXYS Design Automation, Inc.
Barcelona Design, Inc.
Beach Solutions Ltd.
BindKey Technologies - A DuPont Photomask Co.

Company

Cadence Design Systems, Inc.
CAST, Inc.
Celoxica, Inc.
ChipVision
Chronology Div., Forte Design
Cimmetry Systems, Inc.
CMP
CMP Media LLC
Concept Engineering
CoWare, Inc.
DAC Pavilion
Dataram Corp.
DATE 04
Denali Software, Inc.
Design and Reuse
Design Workshop Technologies
DINI Group (The)
Dynalith Systems
e*ECAD
EDAptive Computing, Inc.
EDAToolsCafe.com
eInfochips Inc.
ELANIX, Inc.
Electronics Workbench
Emulation and Verification Engineering
EverCAD Navigator Corp.
Faraday Technology Corp.
FEI Co.
Fintronic USA, Inc.
Flextronics Design
Forte Design Systems

Company

FTL Systems
Fujitsu
Future Design Automation Corp.
GDA Technologies, Inc.
Genesys Testware, Inc.
Get2Chip, Inc.
Global UniChip Corp.
Golden Gate Technology Corp.
Hewlett-Packard Co.
IC Nexus Co., Ltd.
Icinergy Software
Incentia Design Systems, Inc.
InnoLogic Systems Inc.
Intel Corp.
Intellitech Corp.
InternetCAD.com, Inc.
Interra Systems, Inc.
InterWeave Tech
InTime Software
INTUSOFT
iRoC Technologies
Kluwer Academic Publishers
Korea Electronics Technology Institute
Legend Design Technology, Inc.
Library Technologies, Inc.
LogicVision
Macrovision Corp.
Magma Design Automation, Inc.
MathWorks (The)
MEMSCAP Inc.
Mentor Graphics Corp.

Exhibitor List

Company

Monterey Design Systems
Morgan Kaufmann, an imprint of Elsevier
MOSIS
MyCAD, Inc.
Nassda Corp.
Neolinear, Inc.
Nordic VLSI ASA
Novas Software, Inc.
NPTest, Inc.
ObjectStore, a division of Progress Software
Obsidian Software, Inc.
OEA International, Inc.
Open Core Protocol International Partnership
OptEM Engineering Inc.
Optimal Corp.
Oridus Inc.
Paragon IC Solutions, Inc.
PDF Solutions, Inc.
Penton Technology Media, Inc.
Prentice Hall-PTR
ProDesign Electronic & CAD Layout GmbH
Progate Group Corp.
Prolific, Inc.
Prosilog SA
Pulsic Ltd.
Q Design Automation
QThink

Company

Random Logic Corp.
Real Intent
Reed Business Information
Runtime Design Automation
Sagantec
Sandwork Design Inc.
Sequence Design, Inc.
SIGDA/DAC University Booth
Signal Integrity Software
Sigrity, Inc.
Silicon Canvas, Inc.
Silicon Design Solutions, Inc.
Silicon Forest Research, Inc.
Silicon Integration Initiative-Si2
Silicon Metrics Corp.
Silvaco International
SOISIC
StarNet Communications
Summit Design, Inc.
Sun Microsystems
Sycon Design Inc.
SynAPPS Software Corp.
SynaptiCAD Inc.
Synchronicity Inc.
Synopsys, Inc.
Synplicity, Inc.
SynTest Technologies, Inc.
Tanner EDA

Company

Target Compiler Technologies
TDA Systems, Inc.
Telecom Italia Lab.
Tempus Fugit, Inc.
Tenison EDA
Tensilica, Inc.
Tera Systems, Inc.
TransEDA
TriCN
True Circuits, Inc.
TSMC
UbiTech, Inc.
UP Media Group, Inc.
Verisity Design, Inc.
Veritools, Inc.
Verplex Systems, Inc.
Virage Logic
Virtual Silicon Technology
Voom, Inc.
Western Design Center
Wiley
X Initiative
Xpedion Design Systems, Inc.
Y Explorations, Inc.
Zenasis Technologies, Inc.
Zuken USA

Exhibiting Company Descriptions

@HDL Inc.
Find more bugs, Faster. @Verifier and @Designer deliver a unified, assertion-based verification solution for both PSL Sugar and OVA flows.

0-In Design Automation
0-In's comprehensive assertion-based verification solution delivers formal verification, verification IP and methodology enabling design teams to tape out with confidence.

ACE Associated Compiler Experts bv
ACE Associated Compiler Experts is an independent ICT-company specialized in advanced system-software and home of the CoSy compiler development system.

Acreo Socware Center
AcreoSocwareCenter does contractual R&D in the field of integrated circuit and system design for the emerging wireless communication systems.

Agilent Technologies
Agilent EEsof EDA is the leading supplier of Electronic Design Automation (EDA) software for high-frequency system, circuit, and modeling applications.

Alba Centre (The)
The Alba Centre, Scotland - developing a worldwide reputation for excellence in microelectronic product design and technology.

Aldec, Inc.
Aldec delivers high-performance, HDL-based verification solutions. Continuous innovation, superior quality and commitment to customers comprise the foundation of Aldec's strategic objectives.

Alternative System Concepts, Inc.
Nanotechnology design methods and tomorrow's tools for HDL translation, JTAG test insertion, behavioral power optimization, CDFG, ALF, and radiation hardening.

AmmoCore Technology
AmmoCore's SuperFlat™ solution for SOC designs delivers early predictability; 10X increase in productivity, and proven silicon realization through a patented, scalable architecture and methodology, real prototyping and multi-processing environment.

Anadigm, Inc.
Anadigm®, merging three powerful design trends from the digital world-design automation, field-programmable ICs, and real-time updating into a new platform for analog design.

Analog Design Automation
Analog Design Automation, Inc. (ADA) is a leading provider of high capacity optimization tools for the analog, mixed-signal, and custom integrated circuit (IC) markets.

Anasift Technology Inc.
Anasift Technology delivers optimization/synthesis tools that remove the high performance analog IC design productivity bottleneck and assure accurate silicon implementation.

Ansoft Corp.
Ansoft provides high performance solutions for IC packaging, high speed printed circuit boards (PCBs), RFICs and EMI analysis.

Apache Design Solutions, Inc.
Apache is the technology leader in power, providing complete dynamic power integrity solutions for SoC designs, reducing risk and improving yields.

Apex Design Systems, Inc.
Apex provides innovative timing closure and area reduction tools and services.

Exhibiting Company Descriptions

Applied Simulation Technology
Applied Simulation Technology is a leading provider of EDA software solutions for Signal Integrity and EMI modeling and simulation. Applications are for PCB and IC.

Applied Wave Research, Inc.
AWR is a leader in high-frequency EDA software for wireless, wireline, and electro-optical applications. AWR's mission is to accelerate time-to-market and reduce development costs.

Aptix Corp.
Aptix Corporation is a leading provider of high-performance, FPGA-based pre-silicon prototype (PSP) solutions to System-on-Chip (SoC) developers.

Archelon Inc.
Company specialized in development of software tools for micro-controllers, digital signal processors, for custom, high-performance, microcoded graphics and array processors

Arrow's Global Information Business
The Global Information Business is an Arrow Electronics, Inc. business unit focused on the creation and selling of information to the electronics industry.

Artisan Components, Inc.
Artisan's semiconductor IP, in use by IC designers at over 1,000 companies worldwide, provides quality solutions that enable design-to-silicon success.

Artwork Conversion Software, Inc.
Artwork will demonstrate our GDSII and MEBES viewers, plotting software, translators and IC package design tools.

Atrenta Inc.
Atrenta's SpyGlass performs structural analysis on RTL code to check for complex problems like clock domain crossings, synchronization, DFT, etc., early at RTL.

austriamicrosystems USA, Inc.
austriamicrosystems Full Service Foundry offers RF-CMOS, high-voltage CMOS, BiCMOS and SiGe-BiCMOS processes. Superior modeling and process support for first time right designs.

Avery Design Systems
Our intelligent HDL-based functional verification products enable dramatic simulation performance, IP reuse, and productivity improvements of the SOC verification process.

Axis Systems, Inc.
Axis Systems' mission is to dramatically increase the verification productivity of system and SoC designers by closing the verification gap.

AXYS Design Automation, Inc.
AXYS Design Automation provides fast, accurate and integrated System-level Virtual Prototyping solutions for verification of SoC platforms and embedded software.

Barcelona Design, Inc.
Barcelona's analog synthesis solutions enable the creation of full-custom, tape-out ready GDSII in a few hours, drastically improving time to market and flexibility.

Beach Solutions Ltd.
Beach Solutions is pioneering the provision of innovative design tools for IP packaging, integration and re-use in complex SoC design.

BindKey Technologies - A DuPont Photomask Co.
BindKey Technologies provides innovative physical implementation solutions enabling nanometer design for manufacture. BindKey's tools work within today's existing design flows.

Cadence Design Systems, Inc.
Cadence Design Systems is the largest supplier of electronic design automation products, methodology services, and design services.

Exhibiting Company Descriptions

CAST, Inc.
Your best source for ASIC/FPGA general purpose IP cores: 8051s and other processors, multimedia, encryption, buses, interfaces, communications, and more.

Celoxica, Inc.
Celoxica provides tools and services for the co-design, co-verification, and direct implementation of programmable systems using a C-based design methodology.

ChipVision
ChipVision offers ORINOCO™, Power Estimation at architecture level in minutes! Visualized scheduling graph with allocation and binding! COME and SEE Optimization of architecture and memories!

Chronology Div., Forte Design
Produces TimingDesigner® Professional v6.0, the de facto standard timing analysis tool used to model, analyze, and publish complex circuit interfaces.

Cimmetry Systems, Inc.
Cimmetry's AutoVue is the premier viewing and markup software, providing native support for 200+ EDA, 2D/3D CAD and Office formats. Download@ www.cimmetry.com.

CMP
CMP offers the access to advanced technologies for ICs, MCMs, and MEMS, prototyping and low volume production.

CMP Media LLC
EE Times (www.eet.com) reports the technology and business news to design engineers and technical managers in the EOEM industry worldwide.

Concept Engineering
Concept Engineering develops and markets innovative schematic generation and viewing technologies for commercial EDA vendors, in-house CAD tool developers, FPGA and IC designers.

CoWare, Inc.
As the leading supplier of system-level EDA tools, CoWare provides a platform-based methodology that cuts SoC design time in half.

DAC Pavilion
Visit the DAC Pavilion to participate in challenging Panel Debates, broadcasting of selected Technical Sessions or to relax in the lounge.

Dataram Corp.
Dataram is a worldwide leader in the manufactureof high performance memory products for the server, workstation and PC markets.

DATE 04
DATE is the single European conference and exhibition for the design, test and manufacturing of electronic systems and circuits.

Denali Software, Inc.
Denali is the world-leading memory and interface solutions provider offering market research, modeling, simulation, verification, and high-performance memory controller IP.

Design and Reuse
Design And Reuse is the leading web portal for IP /SoC exchange, and the first worldwide provider of intranet/internet reuse software infrastructure.

Design Workshop Technologies
A leader in design automation software for physical design and verification of complex microelectronic, photonic and MEMS products.

DINI Group (The)
The DINI Group is a HW/SW engineering firm specializing in FPGA/ASIC circuit design and logic emulation.

Dynalith Systems
Dynalith's iSAVE-MP and iPROVE provide simulation, emulation and HW/SW design verification solutions from the system to the cycle level for FPGA/SoC/ASIC/IP designs.

Exhibiting Company Descriptions

e*ECAD
Value added reseller of EDA tools from over 15 vendors with pay per hour and pay per month licensing options.

EDAptive Computing, Inc.
EDASTAR![SM] - Addressing the need to rapidly recertify upgraded military and space electronic systems, while decreasing the upgrade time and cost.

EDAToolsCafe.com
EDAToolsCafe.com is the premiere online destination for ASIC, IC, and FPGA designers. The portal features valuable daily and weekly news, jobs, and resources.

eInfochips Inc.
eInfochips has experience with multi-million SoC/ASIC designs and offers IPs & solutions in areas ranging from design, verification to reference-board design.

ELANIX, Inc.
SystemView by Elanix is the feature-rich and user friendly simulation tool used by leading electronics manufacturers worldwide to design, develop, and test their Communications, DSP, Signal Processing and RF/Analog systems.

Electronics Workbench
Electronics Workbench provides mainstream professional PCB designers with innovative, advanced, yet easy-to-use design software. Products include schematic capture, simulation, layout and routing.

Emulation and Verification Engineering
EVE presents ZeBu the pioneering Emulation and Prototyping Platform for MHz performance with the most complete software test environment.

EverCAD Navigator Corp.
Multi-level Mixed Mode Full Chip Circuit Simulation & Analysis EDA Solution

Faraday Technology Corp.
Faraday Technology is a leading provider of production proven SIP and full turn-key ASIC design services for UMC in all process technologies.

FEI Co.
Vectra series FIB systems deliver advanced circuit edit and debug capabilities for deep sub-micron technologies, planarized devices, and flip chip parts.

Fintronic USA, Inc.
Super FinSim is an excellent Verilog simulator, with which hundreds ofchips have been taped out. It's new features will dramatically improvetime to market.

Flextronics Design
Flextronics Design is a global provider of product design and development services from concept through product launch.

Forte Design Systems
Forte Design Systems is a leading provider of SystemC-based behavioral design and verification solutions for complex next-generation ASICs, SoCs, and systems.

FTL Systems
Unify verification and optimization using VHDL, VHDL-AMS, VHDL-RF/MW, VHDL-X, Verilog, Verilog-AMS, SPICE and C/C++ flows with Auriga's unique parallel processing.

Fujitsu
Fujitsu presents PRIMEPOWER the best high performance, reliable platform customized for EDA. PRIMEPOWER and EDA software together equals great efficiency and success.

Future Design Automation Corp.
Future Design Automation has the easiest path from ANSI-C algorithms and models to synthesizable RTL. Come see us for a SystemCenter demonstration.

GDA Technologies, Inc.
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Exhibiting Company Descriptions

Genesys Testware, Inc.
Genesys Testware provides advanced embedded memory test solutions and advanced hierarchical logic test solutions for designers of complex ICs.

Get2Chip, Inc.
Get2Chip offers multi-level synthesis technology that provides abstraction for electronic system-level (ESL) design, next-generation synthesis for multi-million gate complexity and enables complete timing closure through a unique topology-modeling capability.

Global UniChip Corp.
Global UniChip Corp. is a dedicated one-stop full service SOC Design Foundry, provides total solutions from silicon proven IPs to the challenging complex time-to-market SOC design, production, and testing services.

Golden Gate Technology Corp.
GGT provides GoPower for VDSM SoCs, including re-entrant Chip Planning and Management functions plus Interactive Power and Ground Synthesis with IR Drop and Power Consumption Analysis.

Hewlett-Packard Co.
HP is a leading global provider of products, technologies, solutions andservices spanning IT infrastructure, personal computing, global servicesand imaging and printing. www.hp.com.

IC Nexus Co., Ltd.
A leading fabless ASIC design & manufacturing services company, providing RTL to ASIC design services and silicon fabrication service.

Icinergy Software Company
Icinergy Software Company delivers pre-synthesis virtual physical prototyping solutions for early capture, analysis and optimization of complex ICs.

Incentia Design Systems, Inc.
Visit us to learn our customers success stories using Incentia's unique timing and synthesis-to-layout solutions for DSM SoC designs.

InnoLogic Systems Inc.
InnoLogic Systems increases design quality by delivering functional verification solutions for full-custom designs with complete coverage, circuit-level accuracy, and ease-of-use.

Intel Corp.
Intel® Corporation in partnership with leading EDA vendors, demonstrate high performance, cost effective 32/64bit silicon design tools on IA/Linux platforms.

Intellitech Corp.
Intellitech licenses (IP) and the Eclipse Test Development Environment to enable customers to configure their FPGAs in-system and execute embedded self-test.

InternetCAD.com, Inc.
InternetCAD.com Inc. featuring Itools, is the high quality, low cost solution for all of your IC placement and routing needs.

Interra Systems, Inc.
Interra Systems, Inc. provides EDA building blocks (analyzers, RTL-synthesis), memory development system and consulting services to EDA, Semiconductor and SOC companies.

InterWeave Tech
Improve design efficiency & project visibility - with continuous proliferation of methodology & knowledge, and methodology-centric project management.

InTime Software
InTime's RTL Timing Analysis verifies timing 20X-50X faster, with physical accuracy. RTL Floorplanning is used throughout the design cycle, while integrating with Cadence and Synopsys flows.

Exhibiting Company Descriptions

INTUSOFT
Since 1985 Intusoft has lead the industry in analog and mixed-signal CAE, featuring unparalleled products and service to 19,000 customers.

IRoC Technologies
iRoC Technologies develops and licences design and test solutions to enhance the security, quality and reliability of nanometer integrated circuits.

Kluwer Academic Publishers
KLUWER ACADEMIC PUBLISHERS, a leading publisher of Design Automation books and journals, invites attendees to visit our display and browse through our latest publications.

Korea Electronics Technology Institute
IPCoS (IP DB center of Soc) was founded as a added-value information exchange center in the field of electronic virtual component, i.e. silicon IP and SoC in Korea Electronic technology Institute

Legend Design Technology, Inc.
MemChar, SpiceCut, MSIM, Turbo-MSIM: Silicon proven EDA tools that provide an automated, layout-based characterization and verification solution for memory IP.

Library Technologies, Inc.
Timing, power, noise modeling and characterization tools, library generators, dynamic circuit optimizationfor cells and critical paths.

LISATek, Inc.
Please see CoWare, Inc.

LogicVision
LogicVision's embedded test enable efficient design and manufacture of complex semiconductors using Embedded Test design and desk top debug station - Validator.

Macrovision Corp.
E-licensing and usage tracking for software applications.Macrovision develops and markets electronic license management tools for the enterprise software markets.

Magma Design Automation, Inc.
Magma provides the fastest path from RTL to Silicon. Visit us for a demo of our complete IC implementation solutions.

MathWorks (The)
The MathWorks, makers of MATLAB® and Simulink® is used in multiple industries /applications to solve challenging design and implementation problems.

MEMSCAP Inc.
MEMSCAP provides innovative solutions based on MEMS technology, including components, modules and systems, design, prototyping (MUMPS) and manufacturing, as well as software suites (MEMS Xplorer, MEMS Pro, Inductor Compiler).

Mentor Graphics Corp.
Mentor Graphics offers innovative tools and services in the areas of IC design and Physical Verification, Functional Verification, FPGA/ PLD, Design-For-Test and PCB design.

Monterey Design Systems
Monterey provides electronic design automation software that enables IC designers to take their circuits from completed logic design to manufacturing ready output.

Morgan Kaufmann, an Imprint of Elsevier
Morgan Kaufmann publishes distinguished publications for the computer and engineering fields including the book series "Systems on Silicon."

MOSIS
IC prototyping, medium-, and low-volume production service. Offers designers worldwide access to TSMC, IBM, AMIS, austriamicrosystems, etc. without size restrictions.

MyCAD, Inc.
MyCAD provides a suite of EDA solutions to electronic system and IC designers a powerful design assistant on PC platforms at affordable price.

Exhibiting Company Descriptions

Nassda Corp.
Discover why over 170 companies use our full-chip verification and analysis software for complex analog, mixed-signal, high-performance digital and SoC designs.

Neolinear, Inc.
Neolinear's automated front-to-back design flow enables rapid design, IP capture and re-use of custom analog, RF and digital circuits.

Nordic VLSI ASA
We are a worldwide semiconductor company, providing components for wireless communication, mixed-signal SoC design services and IP cores.

Novas Software, Inc.
Novas is the leader in behavior-based and knowledge-based debug systems that reduce the functional verification costs for complex IC designs.

NPTest, Inc.
NPTest provides IC Validation, characterization and test products and services that link design to first silicon to production.

ObjectStore, a division of Progress Software
OObjectStore, a division of Progress Software, is the proven leader in the object data management space and the ideal solution for developers creating dynamic, reliable, high-performance applications.

Obsidian Software, Inc.
Obsidian Software, Inc. is an EDA verification tools company located in Austin, TX. Obsidian was founded in 1997.

OEA International, Inc.
OEA International specializes in tools for high accuracy 3D parasitic extraction and on-chip RF passive components design and analysis.

Open Core Protocol International Partnership
OCP-IP is a non-profit semiconductor industry consortium formed to administer the support, promotion and enhancement of the Open Core Protocol specification.

OptEM Engineering Inc.
Interconnect analysis and device extraction software for digital and analog designers concerned with substrate noise and frequency dependent lossy transmission lines.

Optimal Corp.
Signal Integrity, Thermal, and Mechanical Solutions for Package, PCB, and IC.

Oridus, Inc.
Oridus provides a highly secure Web collaboration to connect, communicate, and collaborate at any stage of the product design, training or support.

Paragon IC Solutions, Inc.
Paragon IC Solutions, Inc. provides a complete tool suite for Analog/Mixed Signal IC Design, on Linux and Unix platforms.

PDF Solutions, Inc.
PDF Solutions is the leading provider of Process-Design Integration technologies for manufacturing ICs. The company's DBYI™ solutions enable clients to maximize product yield and manufacturability.

Penton Technology Media, Inc.
Penton Media, Inc. (NYSE: PME) is a leading diversified business-media company that produces market-focused magazines, websites, trade shows, and conferences, and provides marketing and business-development services.

Prentice Hall-PTR
Prentice Hall Professional Technical Reference and PH Higher Education, divisions of Pearson Education, are the world's most respected book publishers.

ProDesign Electronic & CAD Layout GmbH
ProDesign offers SoC Design Verification Tools, called CHIPit. The CHIPit products are scalable FPGA-based IC emulation and high-end rapid prototyping systems.

Exhibiting Company Descriptions

Progate Group Corp.
Progate Group Corporation (PGC) is the first IC design turnkey service pioneer in Taiwan. PGC endeavors to deliver the best quality of service to our customers.

Prolific, Inc.
Prolific's ProTiming and ProGenesis products will dramatically change the way standard cell libraries are developed and deployed in the mainstream EDA flow.

Prosilog SA
PROSILOG develops, markets innovative SoC design tools to carry out on time system level designs and work at transactional level or RTL.

Pulsic Ltd.
Pulsic will be showing exciting new physical design products for complex IC designs, founded on breakthrough shaped-based routing technology.

Q Design Automation
Layout optimization for sub-wavelength VLSI design. Hierarchical migration, compaction, yield enhancement, and design rule fixing using a 2-dimensional method.

QThink
QThink is a pure-play design company with strong experience delivering front-to-back digital design and chip assembly services for mixed-signal and SOC projects.

Random Logic Corp.
Random Logic Corporation presents QuickIND™, QuickCAP®, gdsIISeries™, SvS™ and Auxiliary Tools™, for fast, accurate, and robust inductance, capacitance, and resistance extraction for interconnect circuits.

Real Intent
Leading provider of Assertion-Based Formal Verification, enabling user to verify designs early and reduce cost of verifying integrated circuits, electronic systems and SoC's.

Reed Business Information
Reed Electronics Group is the only industry resource structured to meet the information needs of the global electronics product development process.

Runtime Design Automation
RTDA is the leading design flow automation provider. Flowtracer brings you one-click simplicity to visualize, manage, and optimize your design bandwidth: people, licenses, and CPUs.

Sagantec
The market leader in compaction, process migration and layout acceleration enables custom and analog layout reuse with a seamless Cadence Virtuoso-XL integration.

Sandwork Design Inc.
The premier waveform analysis solution — with extensive Spice-centric resources, for analog and mixed-signal designs.

Sequence Design, Inc.
Sequence offers tool suites for the analysis and optimization of power, timing and signal-integrity effects of nanometer SoC designs.

SIGDA/DAC University Booth
The University Booth provides faculty and students an opportunity to showcase the results of their research on various Design Automation topics.

Signal Integrity Software
Signal Integrity Software, Inc. (SiSoft) provides leading edge EDA analysis software products and expert consulting services for high-speed system design.

Sigrity, Inc.
Sigrity is the technology leader in software tools for analyzing power and signal integrity in high performance printed circuit boards and chip packages.

Exhibiting Company Descriptions

Silicon Canvas, Inc.
Silicon Canvas is the technology leader providing full custom layout solutions. Its rule-driven technology can serve nanometer designs from analog to SoC projects.

Silicon Design Solutions, Inc.
Silicon Design Solutions (SDS) supplies advanced, embedded memory IP and design services for complex ASIC and system-on-a-chip (SoC) designs.

Silicon Forest Research, Inc.
SFR's Tesla™ software toolset, with its revolutionary Intelligent Testbench Automation™ technology, cuts your design verification time in half.

Silicon Integration Initiative-Si2
Si2 is a leading open source EDA standards consortium. Members are championing integration to enable design reuse, EDA tool choice, increased productivity.

Silicon Metrics Corp.
Silicon Metrics provides characterization and modeling tools and technology for the optimization and analysis of timing, power, and signal integrity.

Silvaco International
Silvaco International is a leading provider of electronic design automation (EDA) software for analog and mixed-signal integrated circuit design.

SOISIC
SOISIC (Silicon on Insulator Systems and Integrated Circuits) is the world's first company to focus solely on supporting SOI circuit design and SOI technology development.

StarNet Communications
Bring EDA applications to your Windows desktops with X-Win32, the most powerful PC X server for connecting UNIX and Linux servers to Windows PCs.

Summit Design, Inc.
Summit Design leads the field of electronic system-level design (ESL), providing mission critical solutions for the design, integration, analysis, verification, and management of complex electronic systems.

Sun Microsystems
Sun will demonstrate additions to our high-performance workstation and server lines based on the latest 64-bit UltraSPARC III and Intel P4 processors.

Sycon Design Inc.
Next generation performance with current manufacturing process. Contact us for a free test drive!

SynAPPS Software Corp.
SynApps provides comprehensive EDA tool infrastructure and customized advanced EDA tools. This year we are also launching a rotary clock insertion tool in partnership with MultiGig.

SynaptiCAD Inc.
VHDL, Verilog, C++, e, and OpenVera Testbench Generation! Automatically generate bus-functional models and protocol checkers from graphical timing diagrams.

Synchronicity Inc.
Synchronicity is the leader in design reuse, design collaboration and design management solutions to speed the development of electronic products.

Synopsys, Inc.
Synopsys provides best-in-class design and verification platforms for the development of complex systems-on-chip. Visit us at booth 1912.

Synplicity, Inc.
Synplicity offers synthesis, verification and physical implementationsolutions for FPGA and ASIC designers that demand the best quality of results.

Exhibiting Company Descriptions

SynTest Technologies, Inc.
SynTest provides tools for BIST (logic and memory), boundary-scan, DFT testability analysis, scan / ATPG, fault simulation, and silicon debug.

Tanner EDA
Tanner EDA is the market leader in IC physical design software for Windows® with affordable tools for analog/mixed-signal design.

Target Compiler Technologies
Target is the leading provider of retargetable tools to accelerate the design, programming and verification of flexible IP cores, from embedded processors to programmable ASICs.

TDA Systems, Inc.
TDA Systems, IConnect TDR software: efficient and easy-to-use signal integrity analysis, impedance and S-parameter measurements, eye diagram test, fault isolation.

Telecom Italia Lab.
Within TelecomItaliaLab, System On Chip Department, merging system and technology expertise, supplies customers with competitive & innovative solutions for next generation telecom equipment.

Tempus Fugit, Inc.
The only complete and formal verification solution for standard and proprietary interfaces: PCI Express, PCI-X, AGP, ARM AMBA, Serial-ATA, etc.

Tenison EDA
Tenison VTOC™ models created from RTL shorten development schedules and reduce respins, making co-development and system verification in C/C++/SystemC environments a reality.

Tensilica, Inc.
Tensilica's Xtensa configurable processor lets you generate optimized, customized processors that are so fast that no RTL coding is required.

Tera Systems, Inc.
Tera Systems, RTL Virtual-Prototype solutions, accurately predict timing, area, and congestion bottlenecks for SoC design in 1/10th the time of conventional solutions.

TransEDA
TransEDA will present ready-to-use next generation verification solutions, including dymanic property checking, for FPGA, ASIC and SoC designs.

TriCN
TriCN is a leading developer of high-performance interface intellectual property (IP) products for semiconductor developers in the communications, networking, data storage, and consumer markets.

True Circuits, Inc.
TCI offers high-quality, low-jitter, silicon-proven deskew, clock generator, low-bandwidth and spread-spectrum PLLs in a range of frequencies and multiplication factors.

TSMC
TSMC provides industry-leading IC manufacturing supported by the industry's largest portfolio of library, IP, design tools, and design services.

UbiTech, Inc.
UbiTech provides a Total S/W Solution for the Conflict of CMP Planarity and Timing closure and CMP Yield Enhancement.

UP Media Group, Inc.
Printed Circuit Design & Manufacture magazine is the premiere publication for electronic interconnect professionals. www.pcdandm.com

Verisity Design, Inc.
Functional verification automation to verify your most complex designs faster and more efficiently than ever before. Verification in Motion.

Exhibiting Company Descriptions

Veritools, Inc.
Veritools provides Verilog, VHDL and MixedMode designers with the fastest and most complete source code debug and analysis tool available.

Verplex Systems, Inc.
Verplex is the leader and independent standard in formal verification, providing the only complete solution for functional closure.

Virage Logic
Leading provider of application-optimized semiconductor IP platforms based on memory, logic, I/Os and IP development tools. Silicon proven, production ready.

Virtual Silicon Technology
Virtual Silicon is a leading supplier of semiconductor intellectual property and process technology to manufacturers and designers of complex systems-on-chip (SoC).

Voom, Inc.
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Western Design Center
The Western Design Center, Inc is the Intellectual Property owner of the patented W65C02TM technology. WDC has been licensing low power microprocessor IP since 1981.

Wiley
Wiley specializes in scientific and technical books, journals, textbooks, professional and consumer books and subscription services.

X Initiative
The X Initiative is a consortium of semiconductor industry leaders working to accelerate the availability and fabrication of the X Architecture.

Xpedion Design Systems, Inc.
Xpedion provides accurate transistor-level analysis, verification & behavioral modeling solutions to RFIC/Wireless & high frequency System-on-Chip designers.

Y Explorations, Inc.
YXI's presents ANSI-C based design and verification methodologies for SoC and embedded systems, application-specific processor design and verification, and high performance reconfigurable architecture design.

Zenasis Technologies, Inc.
Zenasis helps ASIC and SOC design teams eliminate negative slack and reach aggressive performance targets. Customer designs have gained over 500 ps in a 130 nanometer process.

Zuken USA
Zuken specializes in advanced technology EDA solutions and customized consulting services for high-speed design, System In Package, and product data management.

Wednesday Night Party

Come Along for the RIDE!

Wednesday, June 4, 2003, 7:30 PM -10:00 PM

Come join the fun at Disney's California Adventure™ park on the Paradise Pier next to the Disneyland® park. Festivities begin at 7:30 PM and include a D.J., wristbands for free games on the Board Walk, and free amusement park rides.

Disney's California Adventure™ park

To be eligible to attend you must register as a student or full conference attendee.

Hands-on Tutorials

Hands-on Tutorials General Information

Hands-on Tutorials will take place in Rooms 211AB & 213D

Hands-on Tutorials are three-hour tutorials presented by exhibitors to demonstrate their solutions to issues related to "signal and power integrity, analysis and methodology". This is an opportunity for attendees with a need to learn about or evaluate products in this area a chance to see, in an in-depth manner, a variety of solutions. Demonstrations are done with the attendees working from Sun workstations while the presenters lead the discussion. The tutorials are limited to the first 30 attendees with a student to workstation ratio of 2:1. Due to the proprietary nature of the discussions, presenting companies have the right to refuse access to employees or contractors of competitors. The cost per tutorial is $50 and attendees are encouraged to enroll in more than one tutorial. Attendees must register for a minimum of an exhibits only registration in order to be eligible to enroll in a Hands-on Tutorial.

A) What Is All This Noise About Signal and Power Integrity?

Sequence Design, Inc.

Monday 9:00 AM - 12:00 PM Room 211AB

This tutorial will present a detailed view of critical signal and power integrity issues, along with automatic detection and correction methods. These methods will be demonstrated through Sequence software running on a real design. Demonstrated capabilities will include extraction, delay calculation, cell characterization, STA, power analysis, voltage drop analysis, noise analysis and timing/noise optimization.

The tutorial will begin with an overview of trends and motivations, including underlying physics and problem formations. The first technology presentation will address SI issues. The second will focus on Power Integrity issues, covering such topics as delay effects, noise effects, packaging effects and electromigration. The tutorial will culminate in a lab that will show how the theories presented earlier are applied to practice by running the Sequence analysis tools on an actual design.

Hands-on Tutorials

B) Signal and Power Integrity Analysis and Methodology

Synplicity, Inc., IOTA Technology, Cadence Design Systems, Inc.

Monday 2:00 PM - 5:00 PM Room 211AB

As process technologies push into the realm of the nanometer, many new complex design issues are cropping up that can delay or totally throw off a tight ASIC release schedule. Some of these problems include IR drop, ground bounce, electromigration, inductance effects, glitches, transmission-line ringing, and crosstalk. The extent to which these issues are accurately modeled and their effects incorporated into timing calculations has a significant impact on reliability, timing closure and eventual time-to-market. Especially for design teams working at the bleeding edge of semiconductor technology, designers need the flexibility to choose design tools with the specific capabilities needed to solve emerging design challenges.

Synplicity, along with Cadence and IOTA Technology, will offer a front-to-back methodology that addresses the power and signal integrity issues facing today's most aggressive designs. These problems cannot be addressed unless a clear understanding of the major design bottlenecks is acquired early in the design flow. Furthermore, these problems cannot be fixed entirely without a tight coupling to synthesis-based optimizations.

This hands-on tutorial methodology will demonstrate enhanced productivity through better utilization of precious routing resources and the need for fewer design iterations. The key concepts presented are integration of power grid creation and analysis early in the flow, instance-specific back-end IR drop and EM analysis, accurate correlation of IR drop to performance degradation, and seamless integration of problem fixes into the design flow.

C) Power and Signal Integrity Simulation of PCBs and Packages • Sigrity, Inc.

Tuesday 2:00 PM - 5:00 PM Room 213D

Sigrity's patented fast electromagnetic field computation methodologies provide the primary technology advantage of the SpeedXP tool suite. These methodologies enable the dynamic electromagnetic analysis of an entire PCB or IC package.

Through simultaneous co-simulation of circuit, package and board, Sigrity's proprietary mehtodologies enable the analysis of system-level power and signal performance. This technology helps ensure integrity from die to die - through IC packages and across boards.

Additonally, Sigrity has developed proprietary techniques of automatic, accurate synthesis of SPICE circuits from N-port network parameters over broadband frequencies. These techniques effectively fill the gap between frequency domain models and time domain simulations.

Sigrity's SpeedXP tool suite includes:

SPEED2000, the first and only commercially available software tool for performing time domain electromagnetic simulation of an entire PCB or IC package.

PowerSI, optimized for frequency domain analysis, is unmatched in extracting frequency dependent multi-port network parameters for power and signal distribution systems.

Broadband SPICE, with unprecedented accuracy over broadband frequencies, synthesizes SPICE circuits from N-port network parameters at a touch of a button.

SPEED2000 and PowerSI are closely interfaced with layout tools from leading vendors such as Cadence, Mentor Graphica and Zuken.

D) Ensuring Signal and Power Integrity at Nanometer Technologies

Magma Design Automation, Inc.

Wednesday 9:00 AM - 12:00 PM Room 211AB

Attend Magma's hands-on tutorial and get up to date on the latest tools and techniques to address power and signal integrity issues. In this tutorial, attendees will run a design from netlist to GDSII, focusing on the impact of power and noise issues. Two tools will be featured: Blast Noise to address signal integrity and Blast Rail for power integrity. The emphasis is on the practical embedding of the power and noise-aware techniques into the advanced netlist-to-GDSII flow of Blast Fusion. To prevent excessive crosstalk and voltage drop problems at the end of the flow, problems must be detected and avoided early. The attendee will learn how to tune the parameters such that the design is as much correct-by-construction as possible. This minimizes iterations, and subsequently the total design time.

Attendees will utilize Blast Noise that combines signal integrity analysis with static timing analysis to analyze and adjust the design to address crosstalk noise and delay effects as well as signal electromigration effects. Magma's unified data model architecture allows the different engines to work concurrently on the most up-to-date design information and correct problems as they manifest during the flow.

Attendees will also utilize Blast Rail that performs accurate power and IR drop analysis, taking advantage of the same unified data model architecture. The integration with static timing analysis allows users to determine the voltage drop-induced delays. The attendee will view the different analysis results in the GUI, perform what-if analysis to make proper planning decisions, and implement them in the same environment.

E) 3.125 Gbps With Your Hair on Fire, Simulation-Based Signal Integrity Analysis of Digital Interconnects at Multi-Gigabit Speeds

Mentor Graphics Corp. and Xilinx, Inc.

Wednesday 2:00 PM - 5:00 PM Room 211AB

As clock frequencies and data rates soar, digital designers are being forced to account for the effects of degraded high-frequency signals, causing otherwise healthy bit streams to be potentially unrecognizable at receiver ICs.

This technical forum will focus on simulation-based signal-integrity analysis of multi-gigabit interconnects using Xilinx Virtex-II Pro™ and RocketIO™ technologies.

Methodologies for proactively dealing with multi-gigabit problems will be discussed, as well as future trends in both IC technology and simulation/virtual prototyping.

The tutorial/demonstration contains:

Simulation-based signal-integrity analysis of multi-gigabit interconnects using Xilinx - Virtex-II Pro and RocketIO technologies

- Eye-diagram and jitter analysis using multi-bit stimuli
- Lossy-line and advanced via modeling
- Inter-symbol interference
- Concurrent simulation using both HSPICE and IBIS

System verification tools used: Mentor Graphics ICX™ and HyperLynx GHz™

Hands-on Tutorials

F) Full-Chip Dynamic Power Grid Methodology from Planning to Verification

Apache Design Solutions, Inc.

Thursday 9:00 AM - 12:00 PM Room Room 211AB

Until now, power grid issues of large SoCs have been addressed by static power and static IR drop late in the design cycle. At 130nm and below, with lower supply voltages and increasing frequencies, dynamic power noise becomes the more critical issue. Full-chip dynamic effects from simultaneous switching events, on-chip and off-chip inductance, and the ad hoc nature of placing decoupling capacitance (or de-cap) are becoming the dominating challenges to the power grid integrity and the good yield of SoCs. Further, as designs get larger, faster, and more complex with memories, designers face the impossible task of generating a vector set that captures the worst-case switching scenarios.

Apache's Tomahawk cell-based power suite enables a complete methodology for full-chip dynamic power integrity from planning through verification. Tomahawk's power methodology enables design and verification to work hand in hand, by proactively preventing verification issues, and refining verification estimates (such as decoupling capacitance) as the design proceeds; thus final power grid verification is ensured and chip yields are improved.

The tutorial topics include:

· Power-grid planning and avoidance. Highlights optimal power network generation and prevention of static and dynamic floorplan errors

· Dynamic P/G design and verification. Demonstrates full-chip design and verification for static and dynamic IR drop, including the effects of package models and de-cap. Participants will go through the process of identifying dynamic "hot spots" in a live design and protecting the problem areas with de-cap.

· Full-chip dynamic analysis and signoff. Highlights new technology in dynamic timing analysis.

G) Signal and Power Integrity Validation with In-Circuit Measurements

NPTest, Inc.

Thursday 2:00 PM - 5:00 PM Room 211AB

NPTest will offer a hands-on tutorial where attendees will learn about tools and technologies that address signal and power integrity problems at first silicon. With in-circuit measurements, data taken directly from the nets and the transistors of the IC can help designers trace the root cause of failures. These can include cross-talk noise, IR drops, clock tree skew, race conditions, etc. NPTest will give a quick overview of probing technologies for waveform acquisition from both wire-bond and flip-chip devices. The technologies range from electron-beam probing to emission-based transistor timing and laser stimulation measurements. Design analysis case studies will follow demonstrating how these tools can help with:

- High speed I/O signal integrity
- PLL jitter and clock tree skew
- Speed path analysis for yield improvement
- Marginality issues, such as design and process interaction.

Following the case studies, the tutorial will introduce ideas and techniques that can be incorporated into the design process, shortening the debug cycle at first silicon. Such techniques include easy accessibility for critical signals, pre-defined probe points, preparation for timing adjustments with resistor and capacitor modifications, and compartmentalized designs for easy isolation. The tutorial will focus on generic techniques that apply to all designs.

The tutorial will allow the students at their work stations to remotely view diagnostic sessions in progress and interact based on collected in-circuit measurements on flip-chip devices. The students will also see movies of active devices for clock tree skew analysis, taken with IBM Picosecond Imaging Circuit Analysis (PICA), a photon emission-based scalable flip-chip probing technology.

Sponsors

The 40th Design Automation Conference is sponsored by IEEE/CAS (Institute of Electrical and Electronics Engineers/Circuits and Systems Society), the ACM/SIGDA (Association for Computing Machinery/Special Interest Group on Design Automation), and the EDA Consortium (Electronic Design Automation Consortium). Membership information is available on the sponsors web site or at the conference at the ACM and IEEE booths.

IEEE Circuits and Systems Society

The IEEE Circuits and Systems (CAS) Society is one of the largest societies within IEEE and in the world devoted to the analysis, design, and applications of circuits, networks, and systems. It offers its members an extensive program of publications, meetings and technical and educational activities, encouraging an active exchange of information and ideas. The Society's peer reviewed publication activities include: Trans. on CAD, Trans. on CAS (Parts I and II) and Trans. on CAS for Video Technology. In addition, the CAS Society co-publishes with other sister societies the Trans. on VLSI, Trans. on Multimedia, Trans. on Nanotechnology, Trans. on Mobile Computing and, new this year, Design and Test of Computers which is available at preferred member rates to CASS members.

CAS also sponsors or co-sponsors a number of international conferences, which include the Design Automation Conference (DAC), the Int'l Conference on Computer-Aided Design (ICCAD) and the Int'l Symposium on Circuits & Systems (ISCAS). A worldwide comprehensive program of advanced workshops including a new series on "Emerging Technologies in Circuits and Systems", as well as our continuing education short courses bring to our worldwide membership the latest developments in cutting-edge technologies of interest to industry and academia alike.

The IEEE/CAS Society has been serving its membership for over 50 years with such member benefits as:

* Discounts on all Society publications, conferences and workshops (including co-sponsored and sister society publications and conferences)
* The Society newsletter Magazine which includes short articles on emerging technologies, society news and current events
* Opportunities to network with peers and experts within our 12 focused committee meetings, the local events of over 60 chapters and more than 20 annual conferences/workshops
* Opportunity to read and review papers, write articles and participate in the Society's government
* And all the personal and professional benefits of IEEE membership

For more information, please contact the IEEE/CAS Society.

Mail: IEEE/CAS Society
15 W. Marne Ave.
PO Box 265
Beverley Shores, IN 46301-0265
Email: cas.info@ieee-cas.org
Phone: (219) 871-0210
Web: www.ieee-cas.org

Sponsors

ACM/SIGDA – The Resource for EDA Professionals

ACM/SIGDA, one of the three organizations that sponsor DAC, has a long history of supporting DAC and the EDA profession. In addition to sponsoring DAC, SIGDA sponsors ICCAD, DATE, and ASP-DAC, and many smaller EDA symposia and workshops.

SIGDA has pioneered electronic publishing of EDA literature, beginning with the DA Library in 1989, which captured 25 years of EDA literature onto an archival series of CD-ROMs. SIGDA published the first EDA conference proceedings on CD-ROMs, and now produces CD-ROM proceedings for most major EDA conferences and symposia.

SIGDA also produces an annual CD-ROM Compendium of those proceedings, sent to our members as a member benefit. SIGDA provides strong support for the ACM journal TODAES (Transactions on Design Automation of Electronic Systems).

SIGDA also publishes two electronic "newsletters". SIGDA's E-Newsletter is sent to all members twice each month, and contains information on upcoming conferences and funding opportunities. SIGDA's DA TechNews made its debut in January, and provides all SIGDA members with a summary of the latest EDA news twice each month.

In addition to electronic publishing, SIGDA provides a broad array of additional resources to its members and to the EDA profession in general. SIGDA organizes and provides partial funding for the University Booth at DAC, and funds various scholarships and awards (including the ACM/SIGDA Outstanding New Faculty Award presented at DAC). More recently, SIGDA's DA Summer School and our Ph.D. Forum at DAC have provided invaluable opportunities for graduate students in EDA. SIGDA also publishes its Monthly Planner three times per year, helping EDA professionals plan their conference activities. For further information on SIGDA's programs and resources, see http://www.sigda.org.

In addition, SIGDA members may also want to consider joining our parent organization, ACM. ACM membership provides access to a variety of ACM products and resources, including discounts on conferences, subscriptions to ACM journals and magazines, and the ACM Digital Library, an invaluable IT resource. For further details, see ACM's home page at http://www.acm.org.

As an EDA professional, isn't it time YOU joined SIGDA?

SIGDA/DAC University Booth

Each year SIGDA organizes the University Booth. The booth is an opportunity for university researchers to display their results and to interact with visitors from industry. Priority is given to presentations that complement the conference technical program. Demos that highlight benchmark results are also encouraged. The Design Contest winners will give demonstrations presenting their designs at the University Booth, Tuesday, 12:00 PM - 2:00 PM. The schedule of presentations will be published at the conference and will also be available on the SIGDA website. We thank the Design Automation Conference for its continued support of this project.

EDA Consortium

Formed in 1989 the EDA Consortium is an international association of companies engaged in the development, manufacture, and sale of design tools and services to the electronic engineering community. The Consortium Enhances the EDA Industry's Efficiency and Perceived Value by:

- Leading forums to discuss industry issues
- Maintaining a centralized web site
- Sponsoring the DAC and DATE (Europe) conferences
- Reporting revenue data on the EDA market
- Recognizing excellence through:
  - Phil Kaufman Award
  - Design Achievement Awards
- Supporting emerging EDA companies

For more information, contact EDA Consortium, 111 W. Saint John St., Ste. 220, San Jose, CA 95113, Phone: (408) 287-3322, Fax: (408) 283-5283, E-mail: info@edac.org, Web site: www.edac.org.

ACM/Proceedings

The Association for Computing Machinery (ACM)

ACM is a major force in advancing the skills of information technology professionals and students. ACM serves its global membership of 75,000 by delivering cutting edge technical information and transferring ideas from theory to practice. ACM hosts the computing industry's leading Portal to Computing Literature. With its journals and magazines, special interest groups, conferences, workshops, electronic forums, Career Resource Centre and Professional Development Centre, ACM is a primary resource to the information technology field. For more information, see www.acm.org.

In 1997, ACM launched its Digital Library, which has now evolved into the ACM Portal. The Portal is an invaluable online resource of more than one million fully searchable pages of text (including a 40+ year archive) from ACM's high quality journals and proceedings dating back to the 1950's. The Portal also reaches the entire world of computing through the fully integrated Online Guide. Additionally, ACM has 33 Special Interest Groups that focus on different computing disciplines. More than half of all ACM members join one or more of these Special Interest Groups. The SIGs publish newsletters and sponsor important conferences such as SIGGRAPH, OOPSLA, DAC, ICCAD and CHI, giving members opportunities to meet experts in their fields of interest and network with other knowledgeable members.

Become an ACM member today and join thousands of other leading professionals, researchers and academics who benefit from all ACM has to offer. Join ACM on-line at http://www.acm.org, or contact ACM directly by phone: (800) 342-6626 (US and Canada) or (212) 626-0500 (Global), by fax: (212) 944-1318, or by e-mail: acmhelp@acm.org. Hours of operation are from 8:30 AM - 4:30 PM Eastern Time.

40th DAC Proceedings

The 40th DAC proceedings will contain 177 papers, panels, and special sessions. DAC is offering each conference and student registrant 40 years of DAC proceedings on DVD. One hardbound copy of this year's proceedings, will be available to registrants for $25 at the time of registration. Should you wish to purchase additional copies, you may do so at the ACM booth. After the conference, mail orders should be sent to ACM. The address for mail orders is:

ACM Order Department
PO Box 11315
New York, NY 10286-1315
Phone: (800) 342-6626 (US and Canada)
or (212) 626-0500 (Global)
Fax: (212) 944-1318
e-mail: orders@acm.org

Wednesday Night Party, Guest Program, Weather, Information Desk, First-Aid

Wednesday Night Party

Wednesday, June 4, 2003, 7:30 PM -10:00 PM

Come join the fun at Disney's California Adventure™ park on the Paradise Pier next to the Disneyland® park. Festivities begin at 7:30 PM and include a DJ, wristbands for free games on the Board Walk, and free amusement park rides to include: California Screamin roller coaster, the Mailiboomer, the Sun Wheel, and King Tritons Carousel.

Picnic-style food will include BBQ Chicken, BBQ Beef sandwiches, grilled marinated vegetable sandwiches, baked beans, corn on the cob, potato salad, rolls and ice cream. Enjoy fun in the California sun and experience the excitement of Disney® at this year's DAC party! It is sure to be one of the best parties yet!

Don't miss the excitement!

To be eligible you must register as a student or full conference attendee. You may also register for the Guest/Family Program.

Weather

Anaheim is one of the few places in the world with a Mediterranean climate. With 355 days of sunshine every year, it is nearly guaranteed that you will experience a beautiful tropical day. Anaheim offers delightful ocean breezes, low humidity, and very little rain. The average high temperature in June is 79 degrees, cooling off at night to 59 degrees. Summer clothing is appropriate and a light jacket may be needed for the evenings.

Guest/Family Program

A $50 registration fee will admit each guest or family member to the following:

1. Wednesday night party at Disney's California Adventure™ park.
2. Use of the complimentary shuttle bus services between all DAC participating hotels and the Anaheim Convention Center.
3. Admission to the exhibit hall when accompanied by an attendee. Registration for the Guest/Family Program will be at the Conference Registration desk on Sunday, June 1 through Wednesday June 4, 2003. A badge will be provided for each registered guest or family member. This badge must be worn to participate in the above activities. Look for the Guest Registration sign in the registration area. Children under the age of 14 are not allowed in the exhibit hall or demo suite area.

On-Site Information Desk

The information desk will be located in Lobby B of the Anaheim Convention Center. (714) 765-2033.

First-Aid Room

The First-Aid Room is located in Lobby B of the Anaheim Convention Center. For assistance please call **ext. 8101**, in emergency call **ext. 8080**. A nurse will be on duty at all times while meetings and exhibits are open.

Transportation

Conference Shuttle Bus Service

Complimentary shuttle bus service is provided for all DAC registered conference attendees, exhibitors, and guest program participants. Day and evening route busing will be provided to and from the Anaheim Convention Center and all participating DAC hotels. Hours will be extended to accommodate the DAC Demo Suite attendees. At 7:00 PM Wednesday night the buses will run from all DAC hotels to Disney's California Adventure™ park until 11:30 PM.

Day Route Schedule (service every 10-15 minutes)

Sunday, June 1	1:00 PM - 5:30 PM
Monday, June 2	7:00 AM - 11:00 PM
Tuesday, June 3	7:00 AM - 11:00 PM
Wednesday, June 4	6:30 AM - 11:30 PM
Thursday, June 5	6:30 AM - 7:00 PM

Busing Routes and Designated Stops

Route #	Pick-Up Location
#1 Disneyland® Hotel	Downtown Disney® Shuttle Boarding Area
#1 Disney's Paradise Pier® Hotel	Front entrance of hotel, curbside
#1 Disney's Grand Californian Hotel®	At Disney's Paradise Pier® Hotel or Downtown Disney®
#2 Hyatt Regency Orange County	Front entrance of hotel
#2 Crowne Plaza Resort	Front entrance of hotel

Prime Time Shuttle

Please visit www.dac.com/40th/travel.html to print discount coupons and instructions for utilizing this shuttle service from local airports.

Rental Cars

Enterprise Rent-a-Car has been contracted for discount rates for DAC attendees. Sample rates are listed below. Call (800) RENTACAR or www.dac.com/40th/travel.html for reservations. Use the discount # 32H7332.

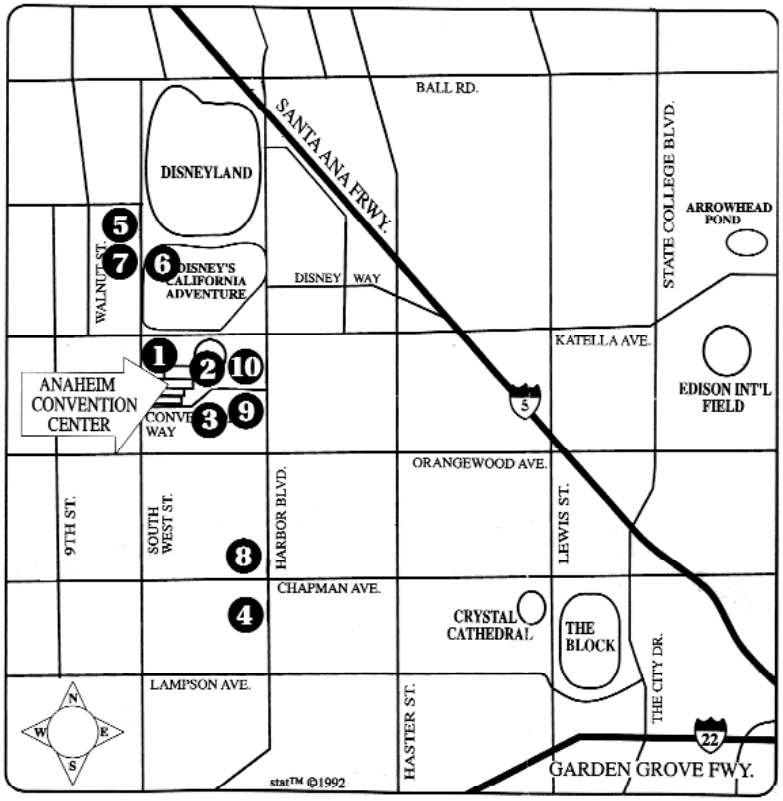
Class	Daily	Weekly
Compact	$25.99	$139.99
Intermediate	$32.99	$159.99
Full Size 2 DR	$38.99	$189.99

DAC Airlines

UNITED AIRLINES United Airlines is the official airline of the 40th DAC. If you or your travel agent call United's toll-free number (800) 521-4041 to book your reservations, you will receive a 5% discount off the lowest applicable discount fare, including First Class or a 10% discount off full fare unrestricted coach fares, purchased 7 days in advance. An additional 5% discount will apply when tickets are purchased at least 30 days in advance of your travel date. Discounts also apply on Shuttle by United and United Express. Call United's Specialized Meeting Reservations Center at (800)-521-4041 to obtain the best fares and schedule information. Make sure you refer to meeting ID Number **516GH.** Dedicated reservation agents are on duty 7 days a week from 8:00 AM to 10:00 PM EST.

SOUTHWEST MEETINGS Southwest Airlines is offering a 10% discount on most of its already low fares for air travel to and from the event. You or your travel agent may call Southwest Airlines Group and Meetings Reservations at (800) 433-5368 and reference the ID Code **MO148.** Reservation Sales Agents are available 7:00 AM - 8:00 PM Monday-Friday, or 8:30 AM - 5:30 PM Saturday and Sunday Central Standard Time. You must make reservations five or more days prior to travel to take advantage of this offer.

Anaheim Hotel Map



ANAHEIM HOTEL KEY

1) Anabella Hotel (The)
2) Anaheim Hilton & Towers *(co-headquarters)*
3) Anaheim Marriott Hotel *(co-headquarters)*
4) Crowne Plaza Resort
5) Disneyland® Hotel
6) Disney's Grand Californian Hotel®
7) Disney's Paradise Pier® Hotel
8) Hyatt Regency Orange County
9) Anaheim Resort
10) WestCoast Anaheim Hotel

Hotel reservations, changes and cancellations are handled by Anaheim/Orange County Visitor & Convention Bureau (AOCVCB) prior to May 9, 2003. Reservations will be processed by mail, phone, fax and on-line. Hours of operation are 8:30 AM - 5:30 PM (PST).

Anaheim/Orange County Visitor & Convention Bureau
PO Box 4270
Anaheim, CA 92803, USA
Phone: (714) 765-8868
Fax: (714) 776-2688
www.dac.com

Anaheim Attractions

Anaheim Attractions

Theme and amusement parks are the name of the game in Anaheim. Disneyland® park and Disney's California Adventure™ park are premiere attractions, but other theme parks are also bountiful. Knott's Soak City USA and Knott's Southern California Resort are close by in Buena Park.

Disney's California Adventure™ park, a new park, features many exciting attractions. Enter the park through the Sunshine Plaza. Visit the Golden State where one can be surrounded by different areas of California such as The Bay Area, Pacific Wharf, and the Golden Vine Winery. Proceed to Paradise Pier to experience the fun of a California boardwalk or experience the excitement of the movie industry at the Hollywood Pictures Backlot. If that is not enough, Disney's Aladdin is the current new musical stage show featured at the park.

The Downtown Disney® District area offers great restaurants, movie theaters, shopping, and entertainment areas such as the House of Blues and the ESPN Zone.

Many inexpensive restaurants are located throughout Anaheim, and most are within walking distance of the Convention Center. If more upscale restaurants appeal to you, check out Yamabuki in Disney's Paradise Pier® Hotel, Catal's in Downtown Disney® District, or Napa Rose in Disney's Grand Californian Hotel®. If you tire of walking, Anaheim Resort Transit (ART) offers visitors convenient shuttle service between attractions.

Anaheim is the home of Baseball's 2002 World Champions, the Anaheim Angels. Baseball lovers can bask in the sun and watch a game at Edison International Field, located just minutes from the Convention Center.

Some shopping centers worth frequenting are the Anaheim Indoor Marketplace, located 1/2 mile east of Disneyland® Park. The Marketplace has over 200 stores selling merchandise 50 - 70% below retail. Anaheim Plaza is a festive, open air shopping center located just 5 minutes from the Convention Center.

For those interested in a short drive, the Pacific Ocean is only 29 miles from Anaheim. Many beautiful seaside towns such as Laguna Beach and Newport Beach offer relaxing atmosphere's where one can swim, stroll the beach or take advantage of numerous restaurants, shops, art galleries, etc. Whatever your tastes, you are sure to find something unique and interesting in the Anaheim area!

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Fax & Mail-In Registration Instructions

Registration is also available on-line @ www.dac.com

Registration Hours

Sunday, June 1, 2003	1:00 PM to 5:00 PM
Monday, June 2, 2003	7:30 AM to 6:00 PM
Tuesday, June 3, 2003	7:30 AM to 6:00 PM
Wednesday, June 4, 2003	7:30 AM to 6:00 PM
Thursday, June 5, 2003	7:30 AM to 5:00 PM
Friday, June 6, 2003	7:30 AM to 6:00 PM

A. Payment MUST be included with the registration form or it WILL be discarded.
B. Registration may be charged to Visa, MasterCard or American Express. For credit card payment include the complete credit card information.
C. If payment is received from a non-US bank, the attendee will be charged a collection fee of $30.00.
D. **May 5, 2003,** is the **DEADLINE** to qualify for the advance registration rate. Payment transactions must be completed on or before May 5, 2003, in order to receive the advance registration rate. After May 5, 2003, advance registrants with incomplete payment information will be required to pay the higher conference rate.

DAC Social Events: Coffee Breaks and the Wednesday Night Party.

Students

A special student rate applies to individuals who are members of IEEE or ACM and are currently enrolled in school. Students who advance register must include a valid IEEE or ACM student membership number and a valid student ID. Students registering on-site must present a valid IEEE or ACM membership card and a Student ID. Student registration includes a copy of 40 Years of DAC Proceedings DVD and all social events.

One/Two-Day Registration

One/two-day only registration includes: the day(s) you select for the Technical Conference, all three days of the Exhibits, and 40 Years of DAC Proceedings DVD. One/two-day only registration does not include the Wednesday Night Party.

For information only, call (800) 321-4573.
Submit on-line, via fax, or mail along with payment:

40th Design Automation Conference
Attn: Registration Desk
5305 Spine Rd., Ste. A
Boulder, CO 80301

TEL: (303) 530-4333
FAX: (303) 530-4334
www.dac.com

E. The DAC office will continue to accept registrations until May 12, 2003, at the at-conference rate. After May 12, 2003, all registration must be done at conference.
F. Register ONE person per form (copy form as needed).
G. **Refund Policy:** Written requests for cancellations must be received in the DAC office by May 5, 2003, and are subject to a $25.00 processing fee. Cancellations received after May 5, 2003, will NOT be honored and all registration fees will be forfeited.
H. Membership number must be included at time of submission to receive the membership rate. No refunds will be made for change in membership status. For information on becoming an IEEE or ACM member, refer to pages 64-65.

Tutorials

Full-day tutorials are offered on Monday, June 2, and Friday, June 6, 2003. You must register for at least one day of the Technical Conference to attend a tutorial. Tutorial registration fee includes: continental breakfast, lunch, breaks, and tutorial notes. See pages 36 - 38 for tutorial descriptions. Hands-on Tutorials require a minimum of an exhibit-only registration. See page 60 for complete instructions.

Workshops

See pages 39 - 41 for workshop registration instructions.

Proceedings

Hard copy of the proceedings will be available for an additional $25 fee for all full conference, student, and one/two-day only registrants.