41 SAN DIEGO DAC
JUNE 7 - 11, 2004

41st Design Automation Conference

ADVANCE PROGRAM

San Diego Convention Center
San Diego, California
www.dac.com

Sponsored by:

ACM SIGDA EDA CONSORTIUM IEEE IEEE CASS/CANDE IEEE CIRCUITS & SYSTEMS SOCIETY

In Technical Cooperation with:

SSCS

41 SAN DIEGO DAC®
JUNE 7 - 11, 2004

WHERE EDA & DESIGNERS MEET

The Design Automation Conference is the premier event for the design of electronic circuits and systems and offers design engineers the complete package of education, networking, and the largest EDA exhibition in the world.

At DAC you'll find solutions to challenges you're facing today and you'll leave prepared to capture tomorrow's opportunities. Whether it's design tools, methodologies, verification and test, design-for-manufacturing, IP, design libraries, RF/wireless, analog and mixed-signal designs, embedded software in SoC, design tool flows or many other issues affecting designs of ICs, ASICs, SoCs and FPGAs, at DAC you will find ways to design better, faster, and more efficiently.

DAC has two exciting new programs this year. First, Tuesday, June 8th is **"Business Day at DAC"**. This is a full-day of sessions geared toward bridging technical and business issues for electronics companies. The other major new development at DAC is **the new combined booth and demo suite format on the Exhibit floor**. Booths and Suites have been combined to allow you to make your visit to the exhibitors easier and more efficient. See inside back cover for a detailed list of participating exhibitors.

Attendees have access to over 200 technical presentations, full-day and hands-on tutorials, workshops, and exhibit floor pavilion panels. You get all this education along with the exhibition featuring an entirely new format designed to increase your ability to view products from over 200 exhibitors. Don't miss it.

Detailed conference information is now available on-line: www.dac.com

DAC at a Glance...

co-located conference	The 41st Design Automation Conference Week in Review					
	Sunday, June 6	Monday, June 7	Tuesday, June 8	Wednesday, June 9	Thursday, June 10	Friday, June 11
• IWLS 2004 June 2-4, *Temecula Creek Inn,* *Temecula, CA*	• Workshop	• FREE Monday • Full-Day Tutorial • Hands-on Tutorials • Exhibits • Workshops	• Opening Session • Keynote Address *Pat Gelsinger* • Technical Sessions • Business Day at DAC • Hands-on Tutorial • Exhibits	• Technical Sessions • Hands-on Tutorials • Exhibits • DAC Party	• Keynote Address *Walden C. Rhines* • Technical Sessions • Hands-on Tutorials • Exhibits • Best Paper Awards	• Full-Day Tutorials

DAC Technical Session Highlights...

The DAC technical program was created from a record 785 paper submissions resulting in a program of the highest quality. Overall, seven different topic areas are included in the technical program this year: Business, System-Level Design and Verification, Power, Logic Design and Test, Embedded Systems, Nanometer Analysis and Simulation, and Physical Circuit Design.

The **Business topic area** is designed to encourage exchange and education on business and technology issues. "**Business Day at DAC**" is a full day of keynotes, panels and focused discussions presented by experts on business topics that effect technology decisions and directions.

In the **System-Level Design and Verification topic area**, the "hot" topic is the tightening connection and the necessary convergence between system-level design and physical design. New high-level design methods using Platforms, SoC and Transaction-Level-Modeling are gaining momentum and the adoption of languages such as SystemC and SystemVerilog is spreading. New challenges in designing secure and multi-processor SoCs are fostering interest. In verification, formal functional verification techniques are starting to make real impact on design methodologies as supplements to simulation and emulation. In parallel, the simulation environment is enhanced with faster functional simulators and sophisticated functional coverage measure.

In the **Embedded System topic area**, success stories of new design tools and flows will be reported. The importance of software code optimization in embedded systems will be demonstrated. In addition, challenges in designing Application-Specific-Instruction-Set processors and challenges in optimizing memory and network architectures will be addressed. New and exciting methods for early evaluation of embedded systems performance and power consumption will be demonstrated.

In the **Power topic area**, innovative solutions are presented to overcome growing power and, in particular, leakage problems. These solutions range from optimal selection of oxide thickness to system-level architecture. Because specialized power reduction techniques are being developed within application domains, the program contains examples from microprocessor to multimedia real-time designs.

In the **Logic Design and Test topic area** the focus this year is on new and exciting approaches in logic synthesis– techniques like pipelining and retiming that were traditionally applied to logic gates are now used to optimize wires. Also, look for presentations on Logic optimizations extended to handle quantum logic and reversible circuits, innovative synthesis of auto-correcting and asynchronous logic and FPGAs driving new classes of systems. In Test, power consumption is becoming a major player and new test techniques are presented to minimize the power consumed by the test logic; and to test power.

In the **Nanometer Analysis and Simulation topic area**, the challenge of design for manufacturability is gaining focus and many innovative ideas are presented at all design stages to ease this growing problem. New parasitic analysis techniques for 2D and 3D designs will be discussed. Exciting ideas on coupling timing and power analysis and the new CAD challenges for the development of BioMEMs application are included.

In the **Physical and Circuit Design topic area**, the importance of analog design is growing. In typical state-of-the-art SoCs the analog component is significant. Synthesis and simulation of mixed-signal circuits are hot topics this year, too. To improve manufacturing yield and cost, regular fabrics are discussed. In addition, the role and impact of floorplanning on architectural-level design is demonstrated.

This is just a sampling of the 57 sessions in the DAC technical program. Each session covers aspects of either Design Methodology (labeled M) or Design Tools (labeled T) or both. Register today and learn how to keep ahead of the curve and get your designs completed at cost, time and performance targets.

Exhibition

DAC has the world's largest and most comprehensive exhibition of EDA tools, silicon and IP solutions and embedded SoC development tools. To further improve the attendee exhibition experience, DAC has combined the booths and demo suites in 2004. The new format is designed to give you the opportunity to see more of the companies you want to see and have better access to in-depth private demos.

	Exhibit Hours
Monday-Wednesday, June 7-9, 2004	9:00am to 6:00pm
Thursday, June 10, 2004	9:00am to 1:00pm

Networking Opportunities and Industry Interaction

Be sure to attend one or all of the DAC functions! Join your colleagues on the DAC show floor, or at the Wednesday night party on June 9, 7:30-10:00pm at the San Diego Marriott Hotel and Marina. Other opportunities include the ACM/SIGDA Ph.D. Forum on Tuesday, June 8, 6:30-9:00pm and the DAC Pavilion, Booth #3733. There are also numerous opportunities to network with old friends and new, in between sessions!

41st Design Automation Conferen

41 SAN DIEGO DAC JUNE 7 - 11, 2004

UML Workshop, Sunday, June 6, 9:00 - 5:00, Room 6F

Monday, June 7

FREE MONDAY EXHIBITS, 9:00 - 6:00

	6C	11A	6D	3	1AB
9:00	**Tutorial 1** Getting Your "Cool ASIC" Up to Speed (Continental Breakfast 8:00 AM - 9:00 AM)	**Hands-on Tutorial** System-Level Power Management • *CoWare, Chip Design Systems, and PowerEscape*			
10:00					Introduction to Chips and EDA For a Non-Technical Audience Workshop, 10:00 AM - 12:00 PM
12:00	Lunch				
1:00				Lunch 1:00 PM	
2:00	**Tutorial 1 (cont.)** Getting Your "Cool ASIC" Up to Speed	**Hands-on Tutorial** Low-Power Design Methodologies and Tools • *BullDAST srl, Accent, STMicroelectronics*	The Last Interoperability Workshop 12:00 PM - 5:00 PM	Workshop for Women in Design Automation: Career and Life Drivers - "Passion vs. Ambition" 2:00 PM - 5:00 PM	
5:00					

Booth #3733
DAC Pavilion
- EDA Business Forecast 9:15 - 10:00
- Wall Street Review of EDA-2004 Update, 10:15 - 11:00
- EDA Mergers &Acquisitions: Glory or Death? 11:15 - 12:00
- Export Controls in the Age of Globalization 2:00 - 2:45
- The Semiconductor IP Business in 2004 3:00 - 3:45
- User Forums or Useless Forums? 4:00 - 4:45

Tuesday, June 8

8:30 to 10:00

Opening Session and Keynote Speaker Location: Ballroom 20ABC

Gigascale Integration for Teraops Performance–Challenges, Opportunities and New Frontiers

Pat Gelsinger - Senior Vice President & Chief Technology Officer, Intel Corp.

BREAK 10:15 - 10:30

	6A	6B	6C	6D	4
	Session 1	**Session 2**	**Session 3**	**Session 4**	**Session 5**
10:30 to 12:00	**CEO PANEL:** EDA: This is Serious Business M/T	**SPECIAL SESSION:** Management of HOT Leakage M/T	Clock Routing and Buffering M/T	Tools and Strategies for Dynamic Verification M	Timing-Driven System Synthesis M/T

LUNCH 12:00 - 2:00

	6A	6B	6C	6D	4	6F
	Session 6	**Session 7**	**Session 8**	**Session 9**	**Session 10**	**Session 100**
2:00 to 4:00	**SPECIAL SESSION:** Reliable System-on-a-Chip Design in the Nanometer Era M/T	**PANEL:** When IC Yield Missed the Target, Who is at Fault? M/T	Power Modeling and Optimization for Embedded Systems T	Performance Evaluation and Run Time Support M/T	Advances in Analog Circuit and Layout Synthesis M/T	Competitive Strategies for the Electronics Industry

BREAK 4:00 - 4:30

	6A	6B	6C	6D	4	6F
	Session 11	**Session 12**	**Session 13**	**Session 14**	**Session 15**	**Session 150**
4:30 to 6:30	Power Grid Design and Analysis Techniques T/M	**PANEL:** What Happened to ASICs? Go (Recon)figure? M/T	Methods for a Priori Feasible Layout Generation M/T	Abstraction Techniques for Functional Verification T	Memory and Network Optimization in Embedded Designs M/T	Business Models in IP, Software Licensing, and Services

Booth #3733
DAC Pavilion
- Ask the CTOs: Everything You Ever Wanted to Know But Were Afraid to Ask 2:00 - 2:45
- EDA Software Quality 3:00 - 3:45
- Does EDA Need a Roadmap for OS Support? 4:00 - 4:45

SIGDA Ph.D. Forum in Sails Pavilion from 6:30 PM - 9:00 PM **Exhibit Hours** 9:00 AM - 6:00 PM

Presenters will be available in room 3 for additional 20-minute question and answer periods after the session.

Wednesday, June 9

	6A	6B	6C	6D	4
	Session 16	**Session 17**	**Session 18**	**Session 19**	**Session 20**
8:30 to 10:00	**SPECIAL SESSION:** The Future of Timing Closure M/T	**PANEL:** Verification, What Works and What Doesn't M/T	Design Space Exploration and Scheduling for Embedded Software T	Advances in Accelerated Simulation M	Design for Manufacturability T

BREAK 10:00 - 10:30

	6A	6B	6C	6D	4
	Session 21	**Session 22**	**Session 23**	**Session 24**	**Session 25**
10:30 to 12:00	Statistical Timing and Analysis T	**PANEL:** System-Level Design: Six Success Stories in Search of an Industry M/T	New Ideas in Placement T	Model Order Reduction and Variational Techniques for Parasitic Analysis T	Compilation Techniques for Embedded Applications T

LUNCH 12:00 - 2:00

	6A	6B	6C	6D	4
	Session 26	**Session 27**	**Session 28**	**Session 29**	**Session 30**
2:00 to 4:00	**SPECIAL SESSION:** Platform-Based System Design M/T	Innovations in Logic Synthesis M/T	Yield Estimation and Optimization T	High-Level Techniques for Signal Processing M/T	Advanced Test Solutions T

BREAK 4:00 - 4:30

	6A	6B	6C	6D	4
	Session 31	**Session 32**	**Session 33**	**Session 34**	**Session 35**
4:30 to 6:30	Advances in Boolean Analysis Techniques T	**PANEL:** Were the Good Old Days all that Good? EDA Then and Now M/T	Power Optimization for Real-Time and Media Rich Embedded Systems M/T	Latency Tolerance and Asynchronous Design T	New Technologies in System Design M/T

Booth #3733
DAC Pavilion
- Standards at the International Level 10:15 - 11:00
- IPQuality: State-of-the-Art Technical Approaches and Their Business Impacts 11:15 - 12:00
- Interview with EDA's Woman of the Year 2:00 - 2:45
- Student Design Contest Award Presentations 3:00 - 3:45

Wednesday Night Party • 7:30 PM - 10:00 PM • San Diego Marriott Hotel & Marina

Exhibit Hours 9:00 AM - 6:00 PM • Presenters will be available in room 3 for additional 20-minute question and answer periods after the session.

TOPIC AREA KEY: Business, Power, Physical/Circuit Design, Nanometer Analysis & Simulation, Logic Design & Test, System-Level Design & Verification, Embedded Systems

T = Design Tools Session • M = Design Methods Session • M/T = Mixed Methods/Tools Session

ıce®, San Diego, CA, June 7 - 11, 2004

Thursday, June 10

	6A	6B	6C	6D	4	Booth #3733
	Session 36	Session 37	Session 38	Session 39	Session 40	DAC Pavilion
8:30 to 10:00	**SPECIAL SESSION:** BioMEMS M/T	**PANEL:** Will Moore's Law Rule in the Land of Analog M/T	Floorplanning T	Issues in Timing Analysis T	**SPECIAL SESSION:** ISSCC Highlights M/T	
	BREAK 10:00 - 10:30					
	Session 41	Session 42	Session 43	Session 44	Session 45	ASIC, COT, or FPGA: Which Should Your Next Chip Be? 10:15 - 11:00
10:30 to 12:00	**SPECIAL SESSION:** Multiprocessor SoC MPSoC Solutions/Nightmare M/T	**PANEL:** Is Statistical Timing Statistically Significant? M/T	Timing Issues in Placement M/T	Design Methodologies for ASIPs M	FPGA-Based Systems M	
	Keynote - *EDA Industry Growth - Are There Enough New Problems to Solve?* **12:45 - 1:45 • Room: Ballroom 20ABC** • *Walden C. Rhines* - CEO and Chairman, Mentor Graphics Corp.				**Best Paper Award Presentations**	
	Session 46	Session 47	Session 48	Session 49	Session 50	
2:00 to 4:00	**SPECIAL SESSION:** Security: A New Dimension in Embedded SystemDesign M/T	Leakage Power Optimization M/T	Interconnect Extraction M/T	New Frontiers in Logic Synthesis T	Numerical Techniques for Simulation M/T	
	BREAK 4:00 - 4:30					
	Session 51	Session 52	Session 53	Session 54	Session 55	
4:30 to 6:00	Energy and Thermal-Aware Design M	Noise-Tolerant Design and Analysis Techniques M/T	New Tools and Methods for Future Embedded SoC M/T	New Scan-Based Test Techniques M/T	CAD for Reconfigurable Computing M/T	

Exhibit Hours 9:00 AM - 1:00 PM

Presenters will be available in room 3 for additional 20-minute question and answer periods after the session.

TOPIC AREA KEY: Business, Power, Physical/Circuit Design, Nanometer Analysis & Simulation, Logic Design & Test, System-Level Design & Verification, Embedded Systems

Hands-on Tutorials — Full-Day Tutorials

	Monday, June 7		Tuesday, June 8	Wednesday, June 9	Thursday, June 10	Friday, June 11
9:00 to 12:00	HoT: System-Level Power Management • *CoWare, ChipVision Design Systems, and PowerEscape*	*Full-Day Tutorial:* 1) Getting Your "Cool ASIC" Up to Speed: Practical Techniques and Tools to Achieve Custom Like Performance in a Power-Aware Design Flow	———	HoT: Flows For Power Minimization • *Magma Design Automation, Infineon Technologies*	HoT: Physical Design of Structured ASICs • *ViASIC*	*Full-Day Tutorials:* 2) Automated Macromodeling Techniques for Design of Complex Analog, Mixed-Signal Integrated Systems 3) Buffering Interconnect: From Basics to Breakthroughs 4) Linux for Real-Time and Embedded Systems 5) Silicon Debug 6) SystemVerilog for Verification: The Unification of Design, Testbench and Assertions in a Single Language
			BREAK 12:00 - 2:00			
2:00 to 5:00	HoT: Low-Power Design Methodologies and Tools • *BullDAST s.r.l., Accent, STMicroelectronics*		HoT: Using Predictive Analysis to Guide Low-Power Design Methodology • *Atrenta*	HoT: Structured ASIC/Platform ASIC Design Methodology, • *Synplicity, LSI Logic Corp., NEC Electronics*	HoT: Designing a Structured ASIC through FPGA Prototyping • *Synopsys, Altera*	

Keynote, Tuesday, June 8- GigaScale Integration for Teraops Performance–Challenges, Opportunities, and New Frontiers

Pat Gelsinger

Senior Vice President & Chief Technology Officer
Intel Corp.
Tuesday, June 8, 8:30am - 10:00am

VLSI system performance increased by five orders of magnitude in the last three decades, made possible by continued technology scaling, improving transistor performance to increase frequency, increasing integration capacity to realize complex architectures, and reducing energy consumed per logic operation to keep power dissipation within limit. The technology treadmill will continue, providing integration capacity of billions of transistors, enabling unprecedented tera-ops levels of performance; however, with some adverse effects posing barriers. Transistor subthreshold as well as gate leakage will impact supply voltage scaling, resulting in excessive power consumption. Therefore, transistor structure will have to change from today's basic bulk transistor to a complex structure of High-K dielectric, single- or multiple-gates per transistor, and polysilicon or a metal as a gate material. The interconnect performance will continue to get worse. Variations due to process, temperature, and supply voltage will have even more prominent effects, and tighter process control will limit design flexibility once taken for granted. Therefore, performance at any cost will not be an option; future system architectures will have to maximize performance in a given power envelope, and evolve innovative architectures to cope with increasing interconnect parasitics. Variations and tighter process control will have a major impact on the design methodology, making a bold move from today's deterministic design to statistical and probabilistic design. Future design automation tools must comprehend these paradigm shifts, be ready with design technology that comprehends new transistor structures, adopt statistical design methodology to overcome variations, comprehend tighter process controls, and still provide unprecedented productivity boost with gigascale integration.

Keynote, Thursday, June 10- EDA Industry Growth - Are There Enough New Problems to Solve?

Walden C. Rhines

Chairman, EDA Consortium
CEO and Chairman
Mentor Graphics Corp.
Thursday, June 10, 12:45pm - 1:45pm

Electronic design automation became an industry when diversification of the electronics and semiconductor industries led to economies of scale for the design software industry. Although the EDA industry gives the appearance of relatively steady growth over its history, in actuality it is driven by rapid growth segments and saturation of successive waves of new design paradigms, e.g. printed circuit board layout, ASIC top-down design, physical design facilitated by silicon foundries, etc. As each of these design paradigms matured, they became slow growth segments of EDA. Future growth of the EDA industry can come only from solving new design problems. Fortunately, there is an abundance of these. Dr. Rhines will address the problems most likely to be the drivers of future industry growth, as well as some less likely possibilities. Walden C. Rhines, 57, is Chairman and Chief Executive Officer of Mentor Graphics, a leader in worldwide electronic design automation with revenue of over $675 million in 2003. Prior to joining Mentor Graphics, Rhines was Executive Vice President in charge of Texas Instruments' Semiconductor Group with responsibility for over $5 billion of revenue and over 30,000 people.

Business Day at DAC – Tuesday, June 8

DAC is a forum for both technology and business. To further encourage exchange and education on business and technology issues, DAC has dedicated a full day to keynotes, panels and special presentations by experts on business topics that affect technology decisions and directions. **Business Day at DAC** is open to all DAC Full-Conference and Tuesday-Only registrants and is targeted at executives and managers who are responsible for technology decisions.
Sessions include:

Opening Session Keynote Address

Pat Gelsinger, CTO & Senior Vice President & Chief Technology Officer, Intel Corp., *Gigascale Integration for Teraops Performance– Challenges, Opportunities, and New Frontiers*

Session 2 CEO PANEL: *EDA: This is Serious Business* - A candid discussion with the CEOs of the three largest EDA companies. Moderated by A. Richard Newton, Dean of Engineering at UC Berkeley.

Session 7 Panel: *When IC Yield Missed the Target, Who is at Fault?*

Session 12 Panel: *What Happened to ASIC? Go (Recon)figure?*

Special Business Day Session 100: *Competitive Strategies for the Electronics Industry*

Special Business Day Session 150: *Business Models in IP, Software Licensing and Services*

The focus of the two special sessions is on globalization, patent portfolio management, business models, IP software licensing models, design services and other important topics. In between sessions, you'll have time for more business networking on the show floor where over 200 exhibitors will display their products in the newly combined booth/suite exhibit area.

Tuesday is Business Day at DAC. Don't miss it!

DAC Pavilion on the Exhibit Floor

DAC has an exciting line-up of panels and presentations in the DAC Pavilion on the Exhibit Floor. The DAC Pavilion sessions are open to all attendees and feature provocative technical, business and strategy discussions.

DAC PAVILION	DAY	TIME
EDA Business Forecast	Mon., June 7	9:15am
Wall Street Review of EDA: 2004 Update	Mon., June 7	10:15am
EDA Mergers & Acquisitions: Glory or Death?	Mon., June 7	11:15am
Export Controls in the Age of Globalization (presented by the EDA Consortium)	Mon., June 7	2:00pm
The Semiconductor IP Business in 2004	Mon., June 7	3:00pm
User Forums or Useless Forums?	Mon., June 7	4:00pm
Ask the CTOs: Everything You Wanted to Know But Were Afraid to Ask	Tues., June 8	2:00pm
EDA Software Quality	Tues., June 8	3:00pm
Does EDA Need a Roadmap for OS Support? (presented by the EDA Consortium)	Tues., June 8	4:00pm
Standards at the International Level	Wed., June 9	10:15am
IP Quality: State-of-the-Art Technical Approaches and Their Business Impacts	Wed., June 9	11:15am
Interview with EDA's Woman of the Year	Wed., June 9	2:00pm
Student Design Contest Award Presentations	Wed., June 9	3:00pm
ASIC, COT or FPGA: Which Should Your Next Chip Be?	Thurs., June 10	10:15am

DAC Workshops

UML for SoC Design
UML 2.0 is nearing its final acceptance as an OMG standard and several industrial and academic groups from the EDA, embedded software and systems, and design communities around the world have started to apply it to Systems-on-Chip (SoC) designs. The DAC UML-SoC workshop is intended to coordinate those efforts, to initiate discussions, and to exchange experiences and information between those groups with a focus on UML application to SoC design and general hardware-related aspects.
Sunday, June 6, 9:00am - 5:00pm $100 (member), $150 (non-member)

Introduction to Chips and EDA for a Non-Technical Audience
Have you ever wondered what everyone is talking about at the Design Automation Conference? Do industry technical terms sound familiar but their definitions escape you? If so, then please plan to attend this workshop to gain a basic understanding of chip design and of the wonderful world of Electronic Design Automation (EDA).
Monday, June 7, 10:00am - 12:00pm $10

The Last Interoperability Workshop
This year DAC will host the fifth and final Workshop on Interoperability, a subject of perpetual and passionate interest. Since the first meeting in 2000 there has been remarkable progress in advancing interoperability. Attend this workshop to learn about the different interoperability projects and how they address challenges facing the electronics industry.
Monday, June 7, 12:00pm - 5:00pm $50 (member), $75 (non-member)

Workshop for Women in Design Automation - *Career and Life Drivers - "Passion vs. Ambition"*
The Workshop for Women in Design Automation is a highlight of DAC. This unique program continues to grow each year and affords the opportunity to hear successful women speak on topics relevant to their careers. It also gives participants a chance to network with their peers and engage in an exchange of views and ideas that foster growth.
Monday, June 7, 1:00pm - 5:00pm $50 (member), $75 (non-member)

exhibition

DAC has the industry's largest and most comprehensive exhibition and demo suites, including state-of-the-art EDA tools, silicon and IP solutions and embedded SoC development tools.

	Exhibit Hours
Monday-Wednesday, June 7-9, 2004	9:00am to 6:00pm
Thursday, June 10, 2004	9:00am to 1:00pm

Attend Free Monday, June 7 , 2004
Register today on-line
or call (800)-321-4573.

exhibiting companies

@HDL, Inc.
0-In Design Automation
AccelChip, Inc.
ACE Associated Compiler Experts
ADVEDA
Agilent Technologies
Aldec, Inc.
Alternative System Concepts
AmmoCore Technology
Analog Bits Inc.
Anasift Technology Inc.
Anchor Semiconductor, Inc.
Ansoft Corp.
Apache Design Solutions, Inc.
Apex Design Systems, Inc.
APLAC Solutions Inc.
Applied Simulation Technology
Applied Wave Research
Appro International
Aprio Technologies, Inc.
Aptix Corp.
Artisan Components, Inc.
Artwork Conversion Software, Inc.
Atrenta
austriamicrosystems USA, Inc.
Avertec Inc.
Avery Design Systems, Inc.
AXYS Design Automation, Inc.
Barcelona Design
Beach Solutions Inc.
Berkeley Design Automation, Inc.
BindKey Technologies, Inc.
Bluespec, Inc.
BULLDAST S.R.L.
CAD Design Software
CADAES GmbH
Cadence Design Systems, Inc.
CADexterity, Inc.
CapExt Corp.
Carbon Design Systems, Inc.
CAST, Inc.
CATS Co., Ltd.
Celoxica Inc.
ChipMD, Inc.
ChipVision Design Systems AG
Cimmetry Systems, Inc.
CiraNova, Inc.
Circuit Semantics, Inc.
ClioSoft, Inc.
CMP
CMP Media LLC
Concept Engineering GmbH
Convergence Promotions
CoWare, Inc.
CRC Press - A Member of Taylor & Francis Pub.
Credence
CriticalBlue
DAC Pavilion
Dataram Corp.
DATE 05
Denali Software, Inc.
Design and Reuse
DINI Group La Jolla, Inc. (The)
Dolphin Integration
Doulos Ltd.
Dynalith Systems
Dynamic Details Inc.
e*ECAD Inc.
eInfochips Inc.
ELANIX, Inc.
Electronics Workbench
EMA Design Automation, Inc.
eTop Design Technology, Inc.
EVE
Evercad Navigator Corp.
Fintronic USA, Inc.
FishTail Design Automation
Forte Design Systems
FTL Systems, Inc.
Genesys Testware, Inc.
GeTeDes Technologies SAS
Gidel
GigaScale IC, Inc.
Golden Gate Technology, Inc.
Handshake Solutions
HARDI Electronics
Hewlett-Packard Co.
Hier Design Inc.
i2 Content & Data Services
IC Editors, Inc.
IC Manage
Icinergy Software Co.
IEEE Media
Incentia Design Systems, Inc.
Intel Corp.
Intellitech Corp.
InternetCAD.com, Inc.
Interra Systems, Inc.
InterWeave Tech
InTime Software
iRoC Technologies Corp.
Jasper Design Inc.
Jeda Technologies
KETI / IP SoC Support Center
Kluwer Academic Pub.
Leda Design, Inc.
Legend Design Technology Inc.
Library Technologies, Inc.
Magma Design Automation, Inc.
Manhattan Routing Inc.
MathWorks, Inc. (The)
Meiosys, Inc.
Mentor Graphics Corp.
Monterey Design Systems
Morgan Kaufmann, an imprint of Elsevier
MOSIS
MyCAD Inc.
Nannor Technologies, Inc.
Nassda Corp.
NeoLinear, Inc.
Novas Software, Inc.
NPTest, Inc.
Obsidian Software, Inc.
OCP - IP Association, Inc.
OEA International, Inc.
OptEM Engineering Inc.
Optimal Corp.
Orora Design Technologies, Inc.
PlatformComputing Inc.
PLDApplications (PLDA)
Praesagus, Inc.
Prentice Hall-PTR (of Pearson Education)
ProDesign GmbH
Progate Group Corp.
Prolific, Inc.
Prosilog SA
Prover Technology
QThink
Quintics
RackSaver, Inc.
Real Intent
Reed Business Information
ReShape
Runtime Design Automation
Safelogic
Sagantec
Sandwork Design Inc.
Sarnoff Europe
SemanticDesigns, Inc.
Sequence Design, Inc.
Shearwater Group, Inc. (The)
Sierra Design Automation, Inc.
SIGDA/DAC University Booth
Sigrity, Inc.
Silicon Canvas, Inc.
Silicon Correlation Div. of Magma (The)
Silicon Design Chain
Silicon Design Solutions, Inc.
Silicon Design Systems, Inc
Silicon Dimensions
Silicon Forest Research, Inc.
Silicon Integration Initiative- Si2, Inc.
Silvaco International
Simantix Systems Inc.
Simucad, Inc.
SliceX, Inc.
Speeding Edge
Spike Technologies, Inc.
StarNet Communications
Summit Design, Inc.
Sun Microsystems
SynAPPS Software Corp.
Synchronicity Inc.
Synfora, Inc.
Synopsys, Inc.
Synplicity, Inc.
SynTest Technologies, Inc.
Tanner EDA
Target Compiler Technologies
Tensilica
Tera Systems Inc.
Tharas Systems Inc.
TransEDA Technology Ltd.
TriCN
Trolltech, Inc.
True Circuits, Inc.
TSMC
UbiTech, Inc.
UMC
VaST Systems Technology
VCX Software Ltd.
VeriEZ Solutions, Inc.
Verific Design Automation
Verisity Design, Inc.
Veritools Inc.
ViASIC Inc.
Virage Logic Corp.
Western Design Center
Xpedion Design Systems, Inc.
YExplorations, Inc.
Z Circuit Automation
Zenasis Technologies, Inc.
Zuken USA

(Exhibitor list current as of March 25, 2004)

Use the DAC *planner* on the DAC web site and build your personal database of sessions, meetings and exhibitors you plan on visiting while at DAC. Detailed conference and exhibition information is now available on-line: www.dac.com. *Register today!*

REGISTER TODAY!

Registration options:

- **Free Monday Exhibit-Only Pass.** Register on-line or call toll-free (800) 321-4573 before May 21, 2004, to receive a pass to visit the Exhibition, on Monday only, June 7, 2004.
- **Exhibit-Only** allows admittance to the Exhibition, Monday through Thursday.
- **Full Conference** includes all three days of the Technical Conference, access to the Exhibition Monday - Thursday, and the 41 Years of DAC Proceedings DVD, plus a ticket to the Wednesday night party.
- **Student** includes all three days of the Technical Conference, access to the Exhibition Monday - Thursday, and the 41 Years of DAC Proceedings DVD, plus a ticket to the Wednesday night party.
- **One/Two Day Registration** includes the day(s) you select for the Technical Conference, all four days of the Exhibition, and the 41 Years of DAC Proceedings DVD.
- **Full-Day Tutorials** are offered on Monday, June 7, and Friday, June 11, 2004. You must register for at least one day of the Technical Conference to attend a tutorial. Tutorial registration fee includes: continental breakfast, lunch, coffee breaks, and tutorial notes.
- **Hands-on Tutorials** are 3-hour tutorials utilizing hands-on software tools from DAC exhibitors. Attendees must register for a minimum of an Exhibit-Only registration in order to be eligible to attend a Hands-on Tutorial. Due to the proprietary nature of the discussions, presenting companies reserve the right to refuse access to employees or contractors of competitors. Space is limited.

Save on your registration two ways! Register before May 10, 2004 and save 20% on your registration. IEEE and ACM members receive an additional 25%. Not yet a member? Find out how to join on the DAC web site.

CONFERENCE	Received by May 10, 2004	After May 10, 2004 or on-site
Member ACM or IEEE	$325.00	$410.00
Non-Member	$425.00	$525.00
Students with ACM or IEEE membership	$150.00	$150.00
One-Day Only *(Tues., Wed., Thur.)*	$215.00	$215.00
Two-Day Only *(Tues., Wed., Thur.)*	$370.00	$370.00

EXHIBITS-ONLY		
Free Monday	Free	Free
Exhibits-Only (access all days)	$60.00	$60.00

TUTORIALS	member ACM or IEEE	non-member	student
Full-Day Tutorials	$270.00	$340.00	$100
Hands-on Tutorials	$75.00 (per tutorial)	$75.00 (per tutorial)	

WORKSHOPS

The Last Interoperability Workshop $50 (member) - $75 (non-member)
Introduction to Chips and EDA for a Non-Technical Audience - $10.00
UML for SoC Design - $100 (member) - $150 (non-member)
Workshop for Women in Design Automation – ***Career and Life Drivers - "Passion vs. Ambition"***, $50 (member) - $75 (non-member)

Visit the DAC web site for on-line registration, complete conference and exhibit details, travel and hotel reservations, and San Diego information at www.dac.com.

Refund Policy: Written requests for cancellations must be received on or before **May 10, 2004**, and are subject to a $25.00 processing fee. Cancellations after May 10, 2004, will NOT be honored and all registration fees will be forfeited. **No registration will be accepted after May 17, 2004 in the DAC office. After May 17, 2004, there will be at-conference registration only.**

TELEPHONE REGISTRATIONS WILL NOT BE ACCEPTED! ANY REGISTRATION WITHOUT PAYMENT WILL BE DISCARDED!

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