The 42nd Design Automation Conference • June 13 - 17, 2005 • Anaheim, CA

Best Paper Awards

Technical Program Co-Chair: **Andrew B.Kahng** - *Univ. of California at San Diego, La Jolla, CA*
Technical Program Co-Chair: **Grant E.Martin** - *Tenscilica, Inc., Santa Clara, CA*

Front-End Design and Embedded Systems Award

Paper 24.2 *A New Canonical Form for Fast Boolean Matching in Logic Synthesis and Verification*

Afshin Abdollahi, Massoud Pedram- *Univ. of Southern California, Los Angeles, CA*

Back-End Design Award

Paper 19.1 *An Efficient Algorithm for Statistical Minimization of Total Power under Timing Yield Constraints*

Murari Mani- *Univ. of Texas, Austin, TX*
Anirudh Devgan- *IBM Corp., Austin, TX*
Michael Orshansky- *Univ. of Texas, Austin, TX*

Best Paper Candidates:

8.1 **Locality-Conscious Workload Assignment for Array-Based Computations in MPSOC Architectures**
Feihui Li, Mahmut Kandemir

9.1 **Response Compression with Unlimited Number of Unknowns Using a New LFSR Architecture**
Erik H. Volkerink

10.1 **A Green Function-Based Parasitic Extraction Method for Inhomogeneous Substrate Layers**
Chenggang Xu, Kartikeya Mayaram, Ranjit Gharpurey, Terri Fiez

12.1 **Partitioning-Based Approach to Fast On-Chip Decap Budgeting and Minimization**
Hang Li, Sheldon Tan, Zhenyu Qi

13.1 **Temperature-Aware Resource Allocation and Binding in High-Level Synthesis**
Gokhan Memik, Rajarshi Mukherjee, Seda Ogrenci Memik

15.1 **Approximate VCCs: A New Characterization of Multimedia Workloads for System-level MpSoC Design**
Samarjit Chakraborty, Wei Tsang Ooi, Yanhong Liu

20.1 **Fine-grained Application Source Code Profiling for ASIP Design Gerd Ascheid, Heinrich Meyr, Kingshuk Karuri, Mohammad Al**
Faruque, Rainer Leupers, Stefan Kraemer

23.2 **Advanced Timing Analysis Based on Post-OPC Extraction of Critical Dimensions**
Dennis Sylvester, Jie Yang, Luigi Capodieci

25.2 **Simulation of the Effects of Timing Jitter in Track-and-Hold and Sample-and-Hold Circuits**
Vinita Vasudevan

25.3 **Scalable Trajectory Methods for On-Demand Analog Macromodel Extraction**
Saurabh K. Tiwary

27.2 **FPGA Technology Mapping: A Study of Optimality**
Andrew C. Ling, Deshanand P. Singh, Stephen D. Brown

28.1 **Word Level Predicate Abstraction and Refinement for Verifying RTL Verilog**
Daniel Kroening, Edmund M. Clarke, Himanshu Jain, Natasha Sharygina

34.3 **Floorplan-aware Automated Synthesis of Bus-based Communication Architectures**
Elaheh Bozorgzadeh, Mohamed Ben-Romdhane, Nikil Dutt, Sudeep Pasricha

35.4 **Multilevel Full-Chip Routing for the X-Based Architecture**
Chen-Feng Chang, Sao-Jie Chen, Tsung-Yi Ho, Yao-Wen Chang