# Call for papers...


## TOPICS OF INTEREST

Authors are invited to submit original technical papers describing recent and novel research or engineering developments in all areas of design automation. Topics of interest include, but are not limited to:

### DESIGN TOOLS TRACK:

The Design Tools track (T) is devoted to contributions to the research and development of design tools and their supporting algorithms. Focus is on innovation of specific modeling, analysis and optimization techniques.

T1.1 Electrical-level circuit and timing simulation
T1.2 Discrete simulation
T1.3 Static timing analysis and timing verification
T1.4 Power analysis and estimation
T2.1 Testing, fault modeling and simulation, TPG, test validation and DFT
T2.2 Transaction-level, RTL and gate-level modeling and validation: simulation, equivalence checking, formal (and semi-formal) verification
T3.1 RT-level design partitioning, physical floorplanning and placement
T3.2 Global and detailed routing
T3.3 Module generation, sizing and library optimizations, physical verification
T4.1 Technology-independent, combinational logic synthesis
T4.2 Technology-dependent logic synthesis, library mapping, cell-based-design, interactions between logic design and layout
T4.3 Sequential and asynchronous logic synthesis and optimization
T4.4 System, logic and physical synthesis for reconfigurable computing
T4.5 High-level synthesis
T5.1 Interconnect and package modeling and extraction
T5.2 Signal integrity and reliability analysis
T5.3 Analog, mixed-signal, MEMS and/or RF design tools
T5.4 System-in-package design and integration tools
T5.5 Design for yield; design-to-manufacturing interface
T6.1 IP protection and reuse for designs, tools, and algorithms
T6.2 Frameworks, intertool communication, design environments and databases

### DESIGN METHODS TRACK:

The Design Methods track (M) deals with innovative methodologies for the design of electronic circuits and systems, as well as creative experiences with design automation in state-of-the-art designs. Submissions for this track will be judged on how innovatively tools are combined into a new methodology that is effectively applied to real-world design problems. Papers focusing on algorithmic advances in modeling, analysis and optimization should be submitted to the design tools track.

*Design methodologies and case studies for specific design tasks*

M1.1 Design entry and specification
M1.2 Electrical-level simulation and modeling
M1.3 Discrete simulation and modeling
M1.4 Static timing and performance analysis
M1.5 Functional design verification
M1.6 Testing, test generation and debugging
M1.7 Physical design, module generation, design for manufacturing
M1.8 Logic synthesis, including interaction with physical synthesis
M1.9 High-level and architectural synthesis

*Design methodologies and case studies for specific application domains and platforms*

M2.1 Overall design flows and methodologies for specific design applications
M2.2 Configurable computing, FPGAs and rapid prototyping
M2.3 Deep sub-micron: signal integrity, interconnect modeling and extraction
M2.4 High-performance design: timing, clocking and power distribution
M2.5 Low-power design
M2.6 Analog, mixed signal, and RF design
M2.7 Process technology development, extraction, modeling and new devices
M2.8 MEMS, sensors, actuators

*Integration and management of DA systems*

M3.1 Management of DA systems, design interfaces, standards
M3.2 Distributed, networked, and collaborative design
M3.3 Intellectual property, design reuse and design libraries

### EMBEDDED SYSTEMS TOPICS:

Embedded Systems are characterized by mixed hardware and software components with limited processing, I/O and storage resources. The increasing role played by software components and their associated support introduces a host of new system design issues. To focus on these, the 42nd DAC will have embedded systems sessions covering both the "tools" and the "methods" aspects of the following topics:

E1 Low-power design: compilation, scheduling and partitioning
E2 Embedded software: retargetable compilation, memory/cache optimization, real-time single-processor scheduling
E3 HW/SW co-design: specification, modeling, co-simulation and performance analysis, system-level scheduling and partitioning
E4 Hardware and software platform design: IP-based design, communication design, embedded HW
E5 Case studies

**ALL SUBMISSIONS MUST BE MADE ELECTRONICALLY AT THE DAC WEB SITE: WWW.DAC.COM**

### REGULAR PAPERS DUE: Monday, Nov. 22, 2004, 5 PM MST

Regular paper submissions must be in PDF format only. Each paper should contain an abstract of approximately 60 words clearly stating the significant contribution, impact and results of the submission AND be no more than 6 pages (including figures, tables and references), double columned, 9pt or 10pt font (format templates are available on the DAC web site for your convenience, but are not required). To permit a blind review, do not include name(s) or affiliation(s) of the author(s) on the manuscript, abstract or bibliographic citations. Submissions exceeding the 6 page limit with fonts smaller than 9pt, or identifying the authors or their affiliations will be automatically rejected. Previously published papers, or papers simultaneously submitted to another conference, will be automatically rejected.

All regular papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage. Authors of accepted papers must sign a copyright release form for their paper. Authors must also provide MP Associates, Inc., a copy of their presentation materials and grant permission for the publication of them on the DAC web site. Notice of acceptance will be sent via email by Friday, March 11, 2005.

### SPECIAL SESSIONS DUE: Wednesday, Nov. 3, 2004, 5 PM MST

Special session submissions must include descriptions of suggested papers and speakers, and the importance of the special session to the DAC audience. DAC reserves the right to restructure all special sessions.

### PANELS and TUTORIALS DUE: Wednesday, Nov. 3, 2004, 5 PM MST

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure all panels and tutorials.

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### STUDENT DESIGN CONTEST DUE: Tuesday, Dec. 7, 2004, 5 PM MST

**Students are invited to submit descriptions of original electronic designs, either circuit level or system level. Submissions should contain the title of the project, a 60-word abstract, a complete description of the design, not exceeding 4000 words, and not more than 10 diagrams and tables. The submission should clarify the originality, distinguishing features, and measured performance of the design. Two categories of designs - operational and conceptual - are eligible for awards. For operational designs, proof-of-implementation is required, while for conceptual designs, complete simulation is necessary. Designs must have taken place as part of the students' work at the university and must have been completed after June 2004. Submitted designs should not have received awards in other contests. Winners will be presented with their award at the 42nd DAC, and will also be invited to present a poster at ISSCC in February 2005.**

# 42nd Design Automation Conference®

The Design Automation Conference (DAC) is the world's premier conference for the design of electronic circuits and systems. Leading industry experts will be presenting the latest developments in design automation tools and methodologies, silicon solutions, and embedded system-on-chip. DAC also unites EDA users and developers, silicon strategists and embedded system developers for collaboration on tools and design methodologies for effective system and IC design.

## Five types of submissions are invited:

regular papers, special sessions, student design contest, panels, and tutorials.

**VISIT OUR WEB SITE FOR INFORMATION ON THE ELECTRONIC SUBMISSION PROCESS & DEADLINES: WWW.DAC.COM**

42nd Design Automation Conference®

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## Call for papers

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