2005 Design Automation Conference
Anaheim Convention Center, Anaheim, CA

42nd DAC

ANAHEIM
JUNE 13-17, '05

ADVANCE PROGRAM

EDA Tools and Methodologies • Silicon Solutions
Embedded System-on-Chip • IP

Sponsored by:

ACM SIGDA EDA CONSORTIUM IEEE IEEE CIRCUITS & SYSTEMS SOCIETY IEEE CASS/CANDE

In Technical Cooperation with:

SSCS

Where Design Meets Your Critical Challenges

Dear Colleague:

This year, it's happening again.

Thousands of executives, managers, designers, academics, journalists and others will be coming to the Design Automation Conference, the largest and most prestigious event focused on the design of electronic circuits and systems. These people will come to learn about the latest in design tools, methodologies, verification and test, design-for-manufacturing, IP, design libraries, RF/wireless, analog and mixed-signal designs, embedded software in SoCs, and much more that affects today's critical design challenges. They'll also come to make valuable contacts and hear from the industry's most renowned thinkers. And they'll leave bursting with new ideas – ideas essential to their continuing success. We hope you are among them.

Convening in Anaheim, California, this year's event promises to be the most engaging, most energizing DAC ever. It will include more than 225 different exhibitors, more than 150 technical presentations, eight technical program panels, 18 pavilion panels, and nine special sessions – all led by widely respected industry experts.

Of particular interest to many of you will be two featured events: Management Day and Wireless Wednesday. Each offers a full day of valuable insights and information dedicated to their respective topics.

For more detailed conference information, please visit us on-line at www.dac.com.

We would be delighted if you design DAC into your June plans. And we think you'll be delighted by the experience you'll have at this year's DAC, the place where design meets your critical challenges.

Best regards,
William H. Joyner, Jr.
General Chair, 42nd DAC

Co-Located Conferences

- **IWLS**
  June 8-10,
  Lake Arrowhead, CA
- **MSE 2005**
  June 12-13,
  Anaheim Marriott

The 42nd Design Automation Conference Week in Review

Sunday, June 12	Monday, June 13	Tuesday, June 14	Wednesday, June 15	Thursday, June 16	Friday, June 17
• **UML for SoC Design Workshop**	• **FREE Monday Exhibits** • **Full-Day Tutorial** • **Hands-on Tutorials** • **Workshops** • **Exhibit Floor Happy Hour** ***(5pm - 6pm)***	• **Opening Session** • **Keynote Address** • **Technical Sessions** • **Management Day** • **Hands-on Tutorial** • **Exhibits**	• **Technical Sessions** • **Hands-on Tutorials** • **Wireless Day** • **Exhibits** • **DAC Party featuring *The Fab Four*** *(Hilton Anaheim)*	• **Keynote Address** • **Technical Sessions** • **Hands-on Tutorials** • **Exhibits** • **Best Paper Awards**	• **Full-Day Tutorials**

Networking Opportunities and Social Activities

Be sure to attend these DAC functions

- Exhibit Floor Happy Hour on Monday, 5:00pm – 6:00pm
- SIGDA Ph.D. Forum on Tuesday, 6:30pm – 8:00pm
- DAC Wednesday Night Party at the Hilton Anaheim in the Pacific Ballroom, 7:30pm – 10:00pm. Enjoy great food, libation, and *The Fab Four* – a nationally renowned Beatles tribute band.
- The DAC Pavilion in Booth 2269 on the exhibit floor – there's always something going on!

DAC Technical Session Highlights...

The DAC technical program was created from a strong set of 735 papers. One of the major innovations in the program this year is the creation of a special theme day on Wireless, to be held on the Wednesday of DAC week. Wireless is highlighted both in the technical program and on the exhibit floor. The **Wireless** topic area features the best submitted papers on wireless topics; a panel covering various implementation platforms for future wireless systems; a special session on emerging directions in wireless with key architects from TI, National, Atheros, and DARPA; and finally, the best of ISSCC Wireless papers which cover leading designs.

In addition to Wireless, there are eight topic areas in the technical program. These are Management, Power, Design for Manufacturability (DFM), System-Level Design and Verification, Nanometer Analysis and Simulation, Embedded Systems, Logic Design and Test, and Physical and Circuit Design.

The **Management** topic area is designed to encourage exchange and education on management, methodology, and technology issues. This is held on Tuesday of DAC week, and consists of the opening keynote session and the CEO panel held in the morning, the EDA Business Forum Luncheon, and two afternoon management sessions. The first discusses the choice of flows and methodologies for SoC design, with expert managers from Freescale, Prairiecom, and PMC-Sierra. The second discusses the strategic management choices and decision making for emergent solutions: ROI for yield, time to volume, low power, and soft errors.

Without doubt, **Power** is HOT at DAC in 2005. With eight power and embedded system low-power sessions, and power as a theme in sessions on system-level design, logic design and FPGAs, it is one of the key topics in design and EDA. Special sessions, panels, and paper sessions look at leakage, dynamic voltage scaling, tradeoffs and estimation, current, and closing the power gap between ASIC and custom - a sequel to a popular session in earlier DACs on closing the performance gap.

In the topic area of **System-Level Design and Verification**, a session on design flows to FPGA, ASIC and DSP using Matlab as an entry language is a key newcomer to DAC this year. Applications of ESL from a wide variety of design teams and applications will be discussed in a panel, as will application-specific architecture design tools. Finally, sessions on real use of formal verification on very large designs and verification methodology, again with an emphasis on real designer experience, round out this topic area. Reporting on real methods and tools used by real design teams on the most challenging designs is a key part of this year's DAC.

The combination of System-Level Design and Verification and the Embedded Systems topic areas offer a tremendous variety of topics to the advanced system designer. The **Embedded Systems** area has seven sessions, including architectures for secure systems and cryptography; communications architectures; multi-processor design methods; high-level energy management; and micro-architectural power optimization. Embedded software sessions focus on high level scheduling, code placement, and task estimation in complex systems.

DFM has seen a significant growth in emphasis at DAC. Seven sessions cover this emerging field, including a panel of DFM experts and a special session on variability. If three words describe DFM, they are variability, statistics, and yield. The DAC DFM sessions reflect this threesome. Getting control of DFM issues via the tools and methods described at this year's DAC is a key to further process scaling to 65 nm and beyond.

Logic Design and Test is the biggest topic area at DAC this year and focuses on DFT, synthesis, FPGAs, and DFT issues. FPGA sessions look at new architectures including nano-scale, power issues, and specialized FPGA tools and flows; power and noise issues continue to be a theme in the synthesis area. A special session also looks at error-tolerant design, giving designers insight into exploiting complexity and coping with operating issues for advanced ICs.

The **Physical and Circuit Design** topic area looks at a number of new approaches; for example, microarchitecture aware floorplanning, new algorithms for timing-driven placement and global placement, and the impact of the X architecture on routing. In the analog area, a special session looks at design space exploration research ready to emerge into industrial application, and mixed-signal optimization is one area finding industrial traction. A panel looking at design with GigaHz IO drivers with the latest FPGAs and advanced communications ICs exposes the problems in this space. Finally, a special session looking at lessons learned with advanced technology and design examples from real design groups will provide hard-won insights from leading-edge teams.

Nanometer Analysis and Simulation carries DAC to the fine detail of design structures. Modeling analog circuits is a perennial problem, and the generation and use of efficient macromodels and reduced-order models provide a slew of new techniques. The other big theme is signal integrity analysis, and recent advances provide many interesting techniques at the boundary between noise, interconnect analysis, and physical design.

This is just a sampling of the 57 sessions in the DAC technical program. Register today and learn how to keep ahead of the process scaling curve, sample wireless design, and manage system complexity and the growing software load of embedded systems.

42nd Design Automation Confere

ANAHEIM JUNE 13-17, '05 DAC

UML for SoC Design Workshop, Sunday, June 12, 9:00am - 5:00pm, Room 207AB

Monday, June 13

Free Monday Exhibit Hours 9:00am - 6:00pm

	210AB	211AB	207CD	207AB	208AB
9:00	**Tutorial 1** Statistical Performance Analysis and Optimization of Digital Circuits (Continental Breakfast 8:00am - 9:00am)	**Hands-on Tutorial** Tera Systems RTL Handoff Technology *Tera Systems*			
10:00					Introduction to Chips and EDA for a Non-Technical Audience Workshop, 10:00am - 12:00pm
12:00	**Lunch**	**Lunch**			
1:00	**Tutorial 1 (cont.)** Statistical Performance Analysis and Optimization of Digital Circuits	**Hands-on Tutorial** Enabling RTL Handoff via Predictive Development *Atrenta, Conexant*	Integrated Design Systems Workshop 12:00pm - 5:00pm	Workshop for Women in Design Automation Lunch: 1:00pm – 2:00pm Keynote and Panel: 2:00pm – 5:00pm	
2:00					
5:00					

Booth #2269

DAC Pavilion

- Dataquest at DAC with Gary Smith **9:30am - 10:30am**
- EDA: Why Invest? **11:00am - 12:00pm**
- Ask the CTO **1:00pm - 2:00pm**
- EDA Serial Acquirees: You Can Run But You Can't Hide **3:00pm - 4:00pm**
- IP Interoperability – Making the Pieces Fit **4:15pm - 5:15pm**

Tuesday, June 14

Exhibit Hours 9:00am - 6:00pm

8:30 to 10:15

Opening Session and Keynote Speaker Ballroom ABC

How Does One Define "Technology" Now That Classical Scaling Is Dead (and Has Been for Years)?

Bernard S. Meyerson - IBM Fellow, Vice President and Chief Technologist, Systems and Technology Group, IBM Corp.

BREAK 10:15am - 10:30am

	207ABC	210CD	210AB	209AB	208AB
	Session 1	**Session 2**	**Session 3**	**Session 4**	**Session 5**
10:30 to 12:00	**CEO PANEL:** Differentiate and Deliver: Leveraging Your Design and IP Partners	**SPECIAL SESSION:** Error-Tolerant Design m	Microarchitecture-Level Power Analysis and Optimization Techniques t	Leakage Analysis and Optimization t	Analog Macromodeling m

LUNCH 12:00pm - 2:00pm

	207ABC	210CD	210AB	209AB	208AB	207D
	Session 6	**Session 7**	**Session 8**	**Session 9**	**Session 10**	**Session 100**
2:00 to 4:00	**PANEL:** ESL: Tales from the Trenches m	Statistical Timing Analysis t	Embedded SW t	Advances in Design-for-Testability Methods m/t	Advances in Boundary Element Methods for Parasitic Extraction t	**MANAGEMENT:** Choosing Flows and Methodologies for SoC Design

BREAK 4:00pm - 4:30pm

	Session 11	Session 12	Session 13	Session 14	Session 15	Session 150
4:30 to 6:30	**PANEL:** DFM Rules! m	Recent Advances in Signal Integrity t	Physical Considerations in High-Level Synthesis m/t	Architectures for Cryptography and Security Applications m	Performance, Energy, and Fault-Tolerance Considerations for MPSoC Designs m	**MANAGEMENT:** How to Determine the Necessity for Emerging Solutions

Booth #2269

DAC Pavilion

- DFM: A Reality Check **10:15am - 11:00am**
- ESL: Is It Just Matlab™ and Excel Spreadsheets? **11:30am - 12:15pm**
- Women in EDA: 2005 Achievement Award **1:00pm - 1:45pm**
- Business IP: Is There No Way Out for IP Vendors? **2:00pm - 2:45pm**
- The Real Cost of Linux **4:00pm - 4:45pm**

SIGDA Ph.D. Forum in Rm 204BC from 6:30pm - 8:00pm

Presenters will be available in room 205AB for additional 20-minute question-and-answer periods after the session.

Topic Areas: **Business** **Design for Manufacturing** **Embedded Systems** **Logic Design & Test** **Nanometer Analysis and Simulation** **Physical Circuit Design** **Power** **System-Level Design and Verification** **Wireless** • **m** = methods • **t** = tools

Wednesday, June 15

Exhibit Hours 9:00am - 6:00pm

	207ABC	210CD	210AB	209AB	208AB
	Session 16	**Session 17**	**Session 18**	**Session 19**	**Session 20**
8:30 to 10:00	**SPECIAL SESSION:** Closing the Power Gap Between ASIC and Custom m	**PANEL:** My Giga Hertz: Does Yours? m	**WIRELESS SESSION:** Information Design Methodology m	Statistical Optimization and Manufacturability t	Application Specific Architecture Design Tools m/t

BREAK 10:00am - 10:30am

	Session 21	Session 22	Session 23	Session 24	Session 25
10:30 to 12:00	**SPECIAL SESSION:** The Titanic: What Went Wrong m	**WIRELESS PANEL:** Wireless Platforms: GOPS for Cents and MilliWatts m	Design Methods for Manufacturability Enhancements m/t	Methods and Representations for Logic Synthesis t	Generating Efficient Models for Analog Circuits m/t

LUNCH 12:00pm - 2:00pm

	Session 26	Session 27	Session 28	Session 29	Session 30
2:00 to 4:00	**WIRELESS SPECIAL SESSION:** Emerging Directions in Wireless m	CAD for FPGAs t	Effective Formal Verification Using Word-Level Reasoning, Bit-Level Generality, and Parallelism t	Advances in Synthesis m/t	Coping and Buffering t

BREAK 4:00pm - 4:30pm

	Session 31	Session 32	Session 33	Session 34	Session 35
4:30 to 6:30	**PANEL:** Is Methodology the Highway out of Verification Hell? m	Impact of Process Variations on Power m/t	**WIRELESS SPECIAL SESSION:** The Best of Wireless at ISSCC m	Architectural Support for Communication m/t	New Approaches to Physical Design Problems t

Booth #2269

DAC Pavilion

- Student Design Contest Award Presentations **10:00am - 10:45am**
- Verification Successes: User's Secret Sauce **11:15am - 12:00pm**
- Wireless Design: Can You Hear Me Now? **1:00pm - 2:00pm**
- Perspectives on Wireless I: Gadi Singer Sings **2:15pm - 3:15pm**
- Perspectives on Wireless II: Mike Muller Mulls **4:00pm - 4:45pm**

Wednesday Night Party • 7:30pm - 10:00pm • Hilton Anaheim Pacific Ballroom

Presenters will be available in room 205AB for additional 20-minute question-and-answer periods after the session.

Topic Areas: **Business** **Design for Manufacturing** **Embedded Systems** **Logic Design & Test** **Nanometer Analysis and Simulation** **Physical Circuit Design** **Power** **System-Level Design and Verification** **Wireless** • **m** = methods • **t** = tools

nce®, Anaheim, CA, June 13 - 17, 2005

Thursday, June 16 — Exhibit Hours 9:00am - 1:00pm

	207ABC	210CD	210AB	209AB	208AB
	Session 36	Session 37	Session 38	Session 39	Session 40
8:30 to 10:00	**SPECIAL SESSION:** Matlab™: The Other Emerging System-Design Language (m)	**PANEL:** Should Our Power Approach Be Current? (m)	Emerging Ideas in Energy Management Techniques (m/t)	Advances in Optimization of Mixed-Signal Circuits (t)	Circuit Performance Under Parameter Variation (t)
	BREAK 10:00am - 10:30am				
	Session 41	Session 42	Session 43	Session 44	Session 45
10:30 to 12:00	**SPECIAL SESSION:** Formally Verifying Your 10-Million Gate Design (m)	Embedded Hardware and System Software (m/t)	Power Estimation and Design Tradeoffs (m)	Programmable Architectures (t)	SAT: Cool Algorithms and Hot Applications (t)
	12:45pm - 1:45pm • Ballroom ABC • Keynote - ***Innovation in the EDA Business Need Not Be an Oxymoron*** *Ronald A. Rohrer* - Corporate Vice President, Advanced Research and Development, Cadence Design Systems, Inc.				**Best Paper Award Presentations**
	Session 46	Session 47	Session 48	Session 49	Session 50
2:00 to 4:00	**SPECIAL SESSION:** DFM and Variability: Theory and Practice (m/t)	Tools and Methods for the Verification of Processors and Processor-Based Systems (m/t)	Electrical Optimization for Physical Synthesis (t)	Optimization Techniques in High-Level Synthesis (t)	Testing for Process- and Timing-Related Faults (m/t)
	BREAK 4:00pm - 4:30pm				
	Session 51	Session 52	Session 53	Session 54	Session 55
4:30 to 6:00	**SPECIAL SESSION:** Hierarchical Design/DSE for Analog ICs (m)	**PANEL:** Platform ASIC Apprentices: Who Will Survive Your Boardroom? (m)	Dynamic Voltage Scaling (t)	New Directions in FPGA Technologies (m)	Reduced-Order Modeling (t)

Booth #2269
DAC Pavilion

The Business of Standards
10:00am - 10:45am

Did Assertions Help You C.Y.A. on Your Last Design?
11:00am - 11:45am

Software Piracy: Can the EDA Industry Survive It?
12:00pm - 12:45pm

Presenters will be available in room 205AB for additional 20-minute question-and-answer periods after the session.

Topic Areas: **Business** **Design for Manufacturing** **Embedded Systems** **Logic Design & Test** **Nanometer Analysis and Simulation** **Physical Circuit Design** **Power** **System-Level Design and Verification** **Wireless** • **m** = methods • **t** = tools

Hands-on Tutorials — Full-Day Tutorials

	Monday, June 13		Tuesday, June 14	Wednesday, June 15	Thursday, June 16	Friday, June 17
9:00 to 12:00	Tera Systems RTL Handoff Technology *Tera Systems*	*Full-Day Tutorial:* 1) Statistical Performance Analysis and Optimization of Digital Circuits	———	Design of Multi-Core Systems with SystemC and Retargetable Processor Tools *Mentor Graphics, Target Compiler*	Virtual System Prototypes for Core-Based SoCDesign *VaST, StarCore*	*Full-Day Tutorials:* 2) C-Based Design: Industrial Experience 3) Constraint Satisfaction Techniques for Automatic Generation of Stimuli for Functional Hardware Verification 4) Advancements in Energy-Efficient Design 5) Design for Manufacturing at 65 nm and Below 6) Design of SoC with Embedded Processors
			BREAK 12:00pm - 2:00pm			
2:00 to 5:00	Enabling RTL Handoff via Predictive Development *Atrenta, Conexant*		Designing Extendable Cores with Low-Cost Metal Programmable Technology *Magma, CoWare, MIPS, Virage Logic*	Using Configurable Processors to Replace RTL Blocks *Tensilica, Virage Logic*	Core-Based SoCDesign *Cadence, Synopsys, IBM*	

Keynote, Tuesday, June 14 • 8:30am - 10:15am • Ballroom ABC

How Does One Define "Technology" Now That Classical Scaling Is Dead (and Has Been for Years)?

Bernard S. Meyerson

IBM Fellow, Vice President and Chief Technologist, Systems and Technology Group, IBM Corp.

Over the past four decades, the IT industry has relied upon the classical scaling of semiconductor technology to drive both performance and product economics. Often confused with Moore's Law, classical scaling speaks to the science driving performance gains over the past decades, not the subset economic issue addressing the real density of transistors on a chip. In effect, classical scaling had been the "glue" binding microprocessor economics, as stated by Moore's Law, to expectations for ongoing progress in microprocessor performance. The impact of the loss of that linkage with the demise of classical scaling has yet to be fully comprehended. The discontinuity engendered by the failure of classical scaling has shaken the microprocessor and IT industry to its foundation, forcing radical shifts in product roadmaps and business focus for those unprepared. This talk will briefly review the origins of this discontinuity, but more critically emphasize new strategies, such as Holistic Design, as employed to drive continued progress in IT performance. First results of the movement to Holistic Design at chip and system levels will be reviewed, as will strategies meant to accelerate efforts in this vein.

Keynote, Thursday, June 16 • 12:45pm - 1:45pm • Ballroom ABC

Innovation in the EDA Business Need Not Be an Oxymoron

Ronald A. Rohrer

Corporate Vice President, Advanced Research and Development, Cadence Design Systems, Inc.

Innovation in EDA is often thought to happen in an isolated eureka moment experienced by a superstar. As many of us have found out the hard way, such events are all too rare, and in any case do not create business success. People with a common goal and passion often together share the breakthrough ideas and their results. To sustain the level of innovation for EDA to survive, we should first recognize that it is a team effort, and then that potential breakthroughs and even just necessary progress can be part of a managed process. A renewable model for EDA innovation that is proving successful involves five steps in progression: problem to prototype, to partnership, to product and, finally, to proliferation.

Management Day – Tuesday, June 14

DAC's Management Day is where technology and business of IC and system design intersect. This full day of sessions is designed for managers and executives of semiconductor, communications, and consumer electronics companies. Participants meet, interact with, and learn from peers who are facing the issues of how to make the right business and technology decisions, given the design flows and platforms available to companies today. The Management Day $75 registration fee includes the 10th Annual EDA Business Forum luncheon, wrap-up cocktail party, and a copy of session 100 & 150 notes. Sessions include:

Opening Session Keynote Address - *How Does One Define "Technology" Now That Classical Scaling Is Dead (and Has Been for Years)?*
Bernard S. Meyerson, IBM Fellow, Vice President and Chief Technologist, Systems and Technology Group, IBM Corp.

Session 1: CEO PANEL: *Differentiate and Deliver: Leveraging Your Design and IP Partners*

EDA Business Forum Luncheon

Session 100: *Choosing Flows and Methodologies for SoC Design*
- ***100.1*** *EDA Flows: Best of Breed or Single-Vendor Solution?*
- ***100.2*** *The Criteria to Select: ASIC vs. Foundry Model*
- ***100.3*** *How to Choose from All the Process Nodes, IP Cores, and Other SoC Suppliers*

Session 150: *How to Determine the Necessity for Emerging Solutions*
- ***150.1*** *Yield Is All That Matters: How Do You Judge Return on Investment?*
- ***150.2*** *How to Meet Time-to-Volume Requirements*
- ***150.3*** *Low-Power Design Decisions: How to Choose the Necessary Ingredients*
- ***150.4*** *Soft Errors: Do You Need to Worry and When? Which Applications Are Affected? How Can You Protect Against These Errors?*

Wireless Wednesday – Wednesday, June 15

What are the hottest new wireless trends and technologies? What impact will they have on implementation strategies, architectures, and methodologies? Where is wireless headed? This year in recognition of the world's enthusiastic embrace of wireless applications, DAC has devoted an entire day to the subject: Wireless Wednesday, June 15, featuring Technical Sessions and Pavilion Panels and Presentations. In addition, DAC has the **Wireless Showcase** on the exhibit floor that includes special displays and presentations of wireless products. Attendees are also invited to participate in the Wireless Walk and be entered to win prizes. Designers of wireless products will not want to miss all that Wireless Wednesday has to offer.

DAC Pavilion on the Exhibit Floor Booth #2269

DAC has an exciting line-up of panels and presentations in the DAC Pavilion on the exhibit floor. The DAC Pavilion sessions are open to all attendees and feature provocative technical, business, and strategy discussions.

DAC PAVILION	DAY	TIME
Dataquest at DAC with Gary Smith	Mon., June 13	9:30am - 10:30am
EDA: Why Invest?	Mon., June 13	11:00am - 12:00pm
Ask the CTO	Mon., June 13	1:00pm - 2:00pm
EDA Serial Acquirees: You Can Run But You Can't Hide	Mon., June 13	3:00pm - 4:00pm
IP Interoperability – Making the Pieces Fit	Mon., June 13	4:15pm - 5:15pm
Women in EDA: 2005 Achievement Award	Tues., June 14	10:15am - 11:00am
ESL: Is it Just Matlab™ and Excel Spreadsheets?	Tues., June 14	11:30am - 12:15pm
DFM: A Reality Check	Tues., June 14	1:00pm - 1:45pm
Business IP: Is There No Way Out for IP Vendors?	Tues., June 14	2:00pm - 2:45pm
The Real Cost of Linux	Tues., June 14	4:00pm - 4:45pm

DAC PAVILION	DAY	TIME
Student Design Contest Award Presentations	Wed., June 15	10:00am - 10:45am
Verification Successes: User's Secret Sauce	Wed., June 15	11:15am - 12:00pm
Wireless Design: Can You Hear Me Now?	Wed., June 15	1:00pm - 2:00pm
Perspectives on Wireless I: Gadi Singer Sings	Wed., June 15	2:15pm - 3:15pm
Perspectives on Wireless II: Mike Muller - The Wireless Carnac, The Magnificent	Wed., June 15	4:00pm - 4:45pm
The Business of Standards	Thur., June 16	10:00am - 10:45am
Did Assertions Help You C.Y.A. on Your Last Design?	Thur., June 16	11:00am - 11:45am
Software Piracy: Can the EDA Industry Survive It?	Thur., June 16	12:00pm - 12:45pm

DAC Workshops

UML for SoC Design

Sunday, June 12, 9:00am - 6:00pm $100 (member), $150 (non-member)

The Unified Modeling Language is a promising means to clearly specify functional and non-functional aspects of hardware and software systems, by adding text and graphics to executable specifications. The workshop's second edition is devoted to applications of the UML to complete System-on-Chip design, with reference to the recent OMG call for proposals on a profile for Modeling and Analysis of Real-Time Embedded Systems (MARTE). It includes contributions on Models of Computation for SoC; performance analysis using abstract UML models; and HW/SW interface and reconfigurable system modeling with UML.

Introduction to Chips and EDA for a Non-Technical Audience

Monday, June 13, 10:00am - 12:00pm $10

Are you new to the Electronic Design Automation (EDA) or chip industry? Have you been in the industry for a while and want to get just a little bit closer to technology? Do you wonder what everyone is talking about at the Design Automation Conference but are afraid to ask? Are you baffled by terms like "semiconductor," "yield," "synthesis," "ESL," "simulation," "design for manufacturing," and "tape-out"? If so, then please plan to attend this workshop to gain a basic understanding of chip design and of the wonderful world of Electronic Design Automation.

Integrated Design Systems Workshop

Monday, June 13, 12:00pm - 5:00pm $50 (member), $75 (non-member)

Streamlined Integrated Design Systems are essential to meet today's business demands. The era of "point tools" linked by files is long over. Custom chip designers struggle to integrate growing numbers of macros while insuring manufacturability. ASIC and SoC designers must optimize many factors simultaneously to achieve "Design Closure." Product designers are exploring 3DIC and SiP to fully exploit chip and package synergy and remain competitive. Attend this workshop to learn how Integrated System Design can work for you.

Workshop for Women in Design Automation -

Cultural Evolution: Keeping Pace with Organizational Diversity

Monday, June 13, 1:00pm - 5:00pm $50 (member), $75 (non-member)

Responding to the dramatic change in the composition of the global workforce in recent years has been a cultural challenge for many organizations. A more diverse population working at an increasingly fast pace requires an organizational culture that embraces change and continuous learning. This workshop explores ways that organizations can keep pace with changing business and workforce diversity needs through new approaches to cultural evolution. Speakers, panelists, and participants are from a variety of companies known for their strong, yet adaptable, cultures.

Exhibition — The 42nd DAC Exhibition is located in Halls B, C, & D

DAC has the world's largest and most comprehensive exhibition of EDA tools, semiconductor IP, SoC design tools, and silicon solutions. Attendees will also find an increasing number of companies offering design-for-manufacturing (DFM) and design-for-test tools, PCB and packaging solutions, and design services and training. The DAC exhibition offers its exclusive booths and suites for in-depth product demonstrations and vendor meetings, and offers attendees the most efficient method of product introductions available. See more companies and get more information at the DAC exhibition!

Attend Free Monday, June 13 , 2005
Register today on-line or call 800-321-4573.

Exhibit Hours

Monday-Wednesday, June 13-15	**9:00am - 6:00pm**
Thursday, June 16	**9:00am - 1:00pm**

Exhibiting Companies (as of March 28, 2005)

@HDL, Inc.
AccelChip, Inc.
Accelicon Technologies, Inc.
ACE Associated Compiler Experts bv
Agilent Technologies
Aldec, Inc.
Alternative System Concepts
Analog Bits Inc.
Anasift Technology Inc.
Anchor Semiconductor, Inc.
Ansoft Corp.
Apache Design Solutions, Inc.
Applied Simulation Technology
Applied Wave Research
Appro International, Inc.
Aprio Technologies, Inc.
ARM, Inc.
Artwork Conversion Software, Inc.
Athena Design Systems
Atrenta Inc.
Averant, Inc.
Avertec Inc.
Avery Design Systems, Inc.
Azuro, Inc.
Beach Solutions Inc.
Berkeley Design Automation, Inc.
BindKey Technologies, Inc.
Blue Pearl Software, Inc.
Bluespec, Inc.
Brion Technologies
BullDAST s.r.l.
BYO Solutions, Inc.
Cadence Design Systems, Inc.
Calypto Design Systems, Inc.
Cambridge Consultants Ltd.
Carbon Design Systems, Inc.
CAST, Inc.
Celoxica Inc.
Chip Design Magazine/Extension Media LLC
ChipMD, Inc.
ChipVision Design Systems AG
Clearshape Technologies, Inc.
ClioSoft, Inc.
CMP
CMP Media LLC
CommandCAD, Inc.
Concept Engineering GmbH
CoWare, Inc.
CRC Press
CriticalBlue
DAC Pavilion
DAFCA, Inc.
DATE '06
Defacto Technologies
Denali Software, Inc.
Design and Reuse
Dini Group, Inc. (The)
Dolphin Integration
Double Summit, LLC
Doulos Ltd.
Dynalith Systems Co., Ltd.
Dynamic Details Inc.
E-Z-CAD, Inc.
EDXACT
eInfochips Inc.
Elsevier
EMA Design Automation, Inc.
Entasys Design, Inc.
Europractice
EVE
Evercad Navigator Corp.
Fintronic USA, Inc.
FishTail Design Automation
Forte Design Systems
FTL Systems, Inc.
Fujitsu Microelectronics America, Inc.
Gaisler Research AB
Genesys Testware, Inc.
Gidel Ltd.
GigaScale IC, Inc.
Golden Gate Technology, Inc.
Gradient Design Automation
Handshake Solutions
HARDI Electronics AB
Hewlett-Packard Co.
IBM Corp.
IC Editors, Inc.
IC Manage
IEEE Media
Ignios Ltd.
Incentia Design Systems, Inc.
Innovative Semiconductors, Inc.
Intel Corp.
Intellitech Corp.
Internet Business Systems, Inc.
InternetCAD.com, Inc.
Interra Systems, Inc.
Jasper Design Automation, Inc.
Jeda Technologies
KETI / IP SoC Support Center
Kilopass Technology, Inc.
KLA-Tencor Corp.
Knowlent Corp.
Legend Design Technology, Inc.
Library Technologies, Inc.
LSI Logic Corp.
LTRIM Technologies Inc.
M2000
Magma Design Automation, Inc.
Manhattan Routing Inc.
MathWorks, Inc. (The)
MatrixOne
Mentor Graphics Corp.
Monster
MOSIS
Mosys, Inc.
MunEDA GmbH
MyCAD Inc.
Nangate A/S
Nannor Technologies, Inc.
Nascentric
Nassda Corp.
NEC Electronics America, Inc.
NEC Informatec Systems, Ltd.
Nordic Semiconductor ASA
Novas Software, Inc.
Obsidian Software, Inc.
OCP - IP Association, Inc.
OEA International, Inc.
Open iT, Inc.
OptEM Engineering Inc.
Optimal Corp.
Platform Computing Inc.
Polliwog USA
Poseidon Design Systems, Inc.
Praesagus, Inc.
Prentice Hall-PTR (of Pearson Education)
ProDesign Electronics Corp.
Prolific, Inc.
Prosilog SA
Pulsic Ltd.
Pyxis Technology, Inc.
QThink
Quintics
Real Intent
Reed Business Information
ReShape
Runtime Design Automation
S2C Inc.
Sagantec
Sandwork Design Inc.
Sarnoff Europe
Semantic Designs, Inc.
Sequence Design, Inc.
Shanghai Hometown Microsystems Inc.
Shearwater Group, Inc. (The)
Sierra Design Automation, Inc.
SIGDA/DAC University Booth
Sigma-C, Inc.
Sigrity, Inc.
Silicon & Software Systems Ltd. (S3 Group)
Silicon Canvas, Inc.
Silicon Design Solutions, Inc.
Silicon Design Systems, Inc.
Silicon Dimensions
Silicon Integration Initiative - Si2, Inc.
Silicon Navigator Inc.
Silvaco International
Simantix Systems, Inc.
SoftJin Infotech Pvt. Ltd.
SpiraTech Ltd.
Springer
StarNet Communications
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Summit Design, Inc.
Sun Microsystems
SynApps Software Corp.
Synfora, Inc.
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Tenison EDA
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Free Monday	Free	Free
Exhibit-Only (access all days)	$60	$60

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5405 Spine Rd., Ste. 102
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