visit the DAC web site @ www.dac.com for more details

Important Information at a Glance

Exhibit Hours

Monday, June 13.....9:00 am - 6:00 pm
Tuesday, June 14.....9:00 am - 6:00 pm
Wednesday, June 15 .....9:00 am - 6:00 pm
Thursday, June 16 .....9:00 am - 1:00 pm

Registration Hours

The registration desk is located in Lobby B of the Anaheim Convention Center and will be open at the following times:

Sunday, June 12 .....8:30 am - 5:00 pm
Monday, June 13.....7:00 am - 6:00 pm
Tuesday, June 14 .....7:00 am - 6:00 pm
Wednesday, June 15 .....7:00 am - 6:00 pm
Thursday, June 16 .....7:00 am - 6:00 pm

Tutorial Registration .....**Friday, June 17, 7:00 am - 6:00 pm**
Located on the second level outside meeting Room **205A**.

Virtual DAC (www.dac.com)

Virtual DAC offers two powerful on-line tools for attendees to make the most of their time at DAC. The DAC Floor is designed to allow attendees to plan which exhibitors they want to visit. The DAC Planner is designed for attendees to plan which technical sessions and other important DAC events they want to attend. Together, the two services allow attendees to organize their time at DAC, and can be downloaded to a Palm OS device.

DACnet-2005

DACnet stations are located in Lobby D on the street level, and outside Room **210A** on the second level of the Anaheim Convention Center.

SIGDA Ph.D. Forum/Member Meeting

Tuesday, June 14, 6:30 pm - 8:00 pm, Rm: **204BC Foyer.** See page 59.
Go to www.sigda.org/programs.php for more information .

Co-Located Conferences

- **IWLS**
  June 8-10,
  Lake Arrowhead, CA
- **MSE 2005**
  June 12-13,
  Anaheim Marriott

The 42nd Design Automation Conference Week in Review

Sunday, June 12	Monday, June 13	Tuesday, June 14	Wednesday, June 15	Thursday, June 16	Friday, June 17
• UML for SoC Design Workshop	• FREE Monday Exhibits • Full-Day Tutorial • Hands-on Tutorials • Workshops • Exhibit Floor Happy Hour *(5pm - 6pm)*	• Opening Session • Keynote Address • Technical Sessions • Management Day • Hands-on Tutorial • Exhibits • SIGDA Ph. D. Forum	• Technical Sessions • Hands-on Tutorials • Wireless Day • Exhibits • DAC Party featuring ***The Fab Four*** *(Hilton Anaheim)*	• Keynote Address • Technical Sessions • Hands-on Tutorial • Exhibits • Best Paper Awards	• Full-Day Tutorials

Program Highlights

Technical Program - details on pages 16 - 37

This year DAC is celebrating its 42nd year with a technical program that includes 181 papers, panels, tutorials, and keynote presentations covering a wide range of design issues. The program covers sessions in nine topic areas: Business, Design for Manufacturing, Embedded Systems, Logic Design & Test, Nanometer Analysis and Simulation, Physical/Circuit Design, Power, System-Level Design and Verification, and Wireless.

In each of these areas, the sessions will cover aspects of both design methodology and design tools. New this year, DAC is offering Wireless Wednesday, which is a day with sessions, panels, and exhibit floor activities dedicated to learning about design of wireless devices. Management Day on Tuesday, June 14, includes sessions and functions discussing topics at the intersection of technology and business for design management.

OPENING SESSION & KEYNOTE
Bernard S. Meyerson
Tuesday, June 14 - 8:30 am
Ballroom ABC
IBM Fellow, Vice President and Chief Technologist, Systems and Technology Group, IBM Corp.

THURSDAY KEYNOTE
Ronald A. Rohrer
Thursday, June 16 - 12:45 pm
Ballroom ABC
Corporate Vice President, Advanced Research and Development, Cadence Design Systems, Inc.

Hands-on Tutorials - details on pages 45 - 48

Hands-on Tutorials are three-hour tutorials presented by exhibitors to demonstrate their solutions to issues in two areas: "RTL Handoff" and "Core-Based SoCDesign."

Management Day - details on pages 6, 16, 19, 21

DAC has dedicated a full day of keynotes, panels, and special presentations by experts on business topics that affect technology decisions and directions.

Opening Session Keynote Address
Session 1: CEO PANEL
EDA Business Forum Luncheon
Session 100: Choosing Flows and Methodologies for SoC Design
Session 150: How to Determine the Necessity for Emerging Solutions

Wireless Wednesday - details on page 7

Wireless Wednesday consists of technical presentations and exhibit floor activities focused on design of wireless systems.

Tutorials - details on pages 38 - 40

Monday, June 13 • 9:00 am - 5:00 pm

1) Statistical Performance Analysis and Optimization of Digital Circuits

Friday, June 17 • 9:00 am - 5:00 pm

2) C-Based Design: Industrial Experience
3) Constraint Satisfaction Techniques for Automatic Generation of Stimuli for Functional Hardware Verification
4) Advancements in Energy-Efficient Design
5) Design for Manufacturing at 65 nm and Below
6) Design of SoC with Embedded Processors

Exhibit Highlights

Exhibit Floor

Monday – Wednesday, June 13-15, 9:00 am – 6:00 pm
Thursday, June 16, 9:00 am – 1:00 pm
Halls B, C, and D of the Anaheim Convention Center

Booth/Suite Format

The Design Automation Conference exhibition includes over 230 companies covering the entire spectrum of the design process from ESL tools on the extreme front-end to DFM tools and foundries on the back-end. DAC will continue to offer its unique blend of combined booths and suites designed to make your time on the exhibit floor more productive. The exhibit floor is a dynamic showplace for this year's line-up of EDA, silicon, IP and embedded system design tools and services.

Children under the age of 14 will NOT be allowed in the exhibit hall.

Exhibits-Only Registration

- Free Monday Exhibits-Only Passes - Attend the exhibition free of charge Monday, June 13.
- $60 Exhibits-Only registration will allow you to attend exhibits Monday through Thursday.

DAC Pavilion

DAC has an exciting lineup of panels and presentations in the DAC Pavilion, Booth 2269 on the exhibit floor. The DAC Pavilion sessions are open to all attendees at no charge and feature 18 provocativetechnical, business, and strategy discussions. See pages 8-11 for details.

New Exhibitors at DAC

DAC has always been the best place to see the industry's newest companies, and this year is no exception. With over 50 new exhibitors, DAC is the place to be to find out what the hot start-ups are up to. Among the companies participating in DAC for the first time are:

AMD
ARC International
Arteris
asicNorth, Inc.
Athena Design Systems
Bellum Software
Blade Technologies Inc.
Blaze DFM, Inc.
Brion Technologies
BYO Solutions, Inc.
Cambridge Consultants Ltd.
Clear Shape Technologies, Inc.
Cologne Chip AG
CommandCAD, Inc.
DAFCA, Inc.
Double Summit, LLC
EDXACT
Emerging MemoryTechnologies Inc.
Entasys Design, Inc.
Extreme DA
Gaisler Research AB
Global Engineering Solutions Ltd.
Gradient Design Automation
Hummingbird Ltd.
Ignios Ltd.
Innovative Semiconductors, Inc.
Javelin Design Automation
Kilopass Technology, Inc.
KLA-Tencor Corp.
Knowlent Corp.
Laflin Limited
M2000
Monster
Nangate A/S
Nascentric
NEC Informatec Systems, Ltd.
Pextra Corp.
Polliwog USA
Proficient Design LLC
Pyxis Technology, Inc.
QualCore Logic, Inc.
S2C Inc.
Shanghai Hometown Microsystems Inc.
Sigma-C, Inc.
Silicon & Software Systems Ltd. (S3 Group)
Silicon Image, Inc.
Silicon Navigator Inc.
Specsoft Consulting, Inc.
SynthWorks / Sunburst Design
Tata Elxsi Ltd.
TeamEDA, Inc.
Tera Route LLC
Time To Market Inc.
Triad Semiconductor, Inc.
Xoomsys, Inc.

How Does One Define "Technology" Now That Classical Scaling Is Dead (and Has Been for Years)?

Bernard S. Meyerson
IBM Fellow, Vice President and Chief Technologist, Systems and Technology Group
IBM Corp.

Abstract: Over the past four decades, the IT industry has relied upon the classical scaling of semiconductor technology to drive both performance and product economics. Often confused with Moore's Law, classical scaling speaks to the science driving performance gains over the past decades, not the subset economic issue addressing the areal density of transistors on a chip. In effect, classical scaling had been the "glue" binding microprocessor economics, as stated by Moore's Law, to expectations for ongoing progress in microprocessor performance. The impact of the loss of that linkage with the demise of classical scaling has yet to be fully comprehended.

The discontinuity engendered by the failure of classical scaling has shaken the microprocessor and IT industry to its foundation, forcing radical shifts in product roadmaps and business focus for those unprepared. This talk will briefly review the origins of this discontinuity, but more critically emphasize new strategies, such as Holistic Design, as employed to drive continued progress in IT performance. First results of the movement to Holistic Design at chip and system level will be reviewed, as will strategies meant to accelerate efforts in this vein.

Biography: Bernard Meyerson is Chief Technologist and Vice President, Technology, for IBM's Systems and Technology Group. He joined IBM Research in 1980, and led the development of silicon germanium and other high-performance mixed-signal technologies over a period of ten years, and subsequently led several large organizations within IBM focused on the development of communications technology, spanning the range from pervasive wireless enablement to high-end data transport. Dr. Meyerson currently leads IBM's Semiconductor Research and Development Center, the multi-company technology alliance located at IBM's East Fishkill semiconductor facility.

Dr. Meyerson was named IBM Fellow, the company's highest technical honor, in 1992. He is a Fellow of the American Physical Society and the IEEE and a recipient of the Materials Research Society Medal, the Electrochemical Society Electronics Division Award, the 1999 IEEE Ernst Weber Award for the body of work culminating in the commercialization of Si-Ge-based communications technology, and the IEEE Electron Devices Society J. J. Ebers Award. He was cited as "Inventor of the Year" in 1997 by the New York State Legislature, and was honored as the 1999 "United States Distinguished Inventor of the Year" by the U.S. Patent and Trademark Office. In 2002, he was elected to the National Academy of Engineering, and in 2003 he was named by EE Times as one of thirteen people "who are influencing the course of semiconductor development technology and taking it into realms that exceed the bounds set by the inventors of the transistor more than fifty years ago." He holds a Ph.D. in physics from City College of the City University of New York.

Innovation in the EDA Business Need Not Be an Oxymoron

Ronald A. Rohrer
Corporate Vice President, Advanced Research and Development
Cadence Design Systems, Inc.

Abstract: Innovation in EDA is often thought to happen in an isolated *eureka* moment experienced by a *superstar*. As many of us have found out the hard way, such events are all too rare, and in any case do not create business success. People with a common goal and passion often together share the breakthrough ideas and their results. To sustain the level of innovation for EDA to survive, we should first recognize that it is a team effort, and then that potential breakthroughs and even just necessary progress can be part of a managed process. A renewable model for EDA innovation that is proving successful involves five steps in progression: problem to prototype, to partnership, to product and, finally, to proliferation.

Biography: Dr. Ronald Rohrer has been affiliated with EDA in various capacities - in semiconductor and software companies, in start-ups and established companies, in universities and in venture capital - for more than forty years. As would anyone having spent so much time in and around EDA, he has seen, learned, accomplished ... and endured a lot. His passion for teamwork to achieve research, development, and business success has been evident throughout his career. Presently he is with Cadence, working as part of an RF IC EDA advanced research and development team.

Dr. Rohrer is a Fellow of the IEEE and a recipient of the IEEE Education Medal, the SRC Technical Excellence Award, the 1996 NEC Computer and Communication Prize, and the Electronic Design Automation Consortium 2002 Phil Kaufman Award. He was elected to the National Academy of Engineering in 1989 for his contributions to circuit simulation that have enabled deep-submicron IC design. He started his industrial career at Fairchild Semiconductor and has served as technical consultant and advisor to many leading EDA and electronics companies. Dr. Rohrer has taught at the University of Illinois at Urbana-Champaign, Southern Methodist University, the University of California at Berkeley, and Carnegie Mellon University, where he is professor emeritus of electrical and computer engineering. An entrepreneur, he was founder of Performance Signal Integrity (later acquired by Integrated Silicon Systems and merged with ArcSys to form Avant! Corporation) and was chairman of Neolinear before its acquisition by Cadence. He holds an S.B. from MIT and a Ph.D. in electrical engineering from the University of California at Berkeley.

Management Day - Tuesday, June 14

DAC's Management Day is where technology and business of IC and system design intersect. This full day of sessions is designed for managers and executives of semiconductor, communications, and consumer electronics companies. Participants meet, interact with, and learn from peers who are facing the issues of how to make the right business and technology decisions, given the design flows and platforms available to companies today. The Management Day $75 registration fee includes the 10th Annual EDA Business Forum luncheon, wrap-up cocktail party, and a copy of session 100 and 150 notes.

Management Day Sessions include:

Opening Session Keynote Address -
Ballroom ABC • 8:30 am - 10:15 am

Bernard S. Meyerson - IBM Fellow, Vice President and Chief Technologist, Systems and Technology Group, IBM Corp.
How Does One Define "Technology" Now That Classical Scaling Is Dead (and Has Been for Years)?

Session 1 CEO Panel - Rm: **207ABC** • 10:30 am - 12:00 pm

Differentiate and Deliver: Leveraging Your Design and IP Partners
Chair: Jay Vleeschhouwer - *Merrill Lynch, New York, NY*
Organizers: Rich Goldman, David Park

Panelists:
Warren East - CEO, *ARM Ltd., Cambridge, UK*
Michael J. Fister - CEO, *Cadence Design Systems, Inc., San Jose, CA*
Walden C. Rhines - CEO, *Mentor Graphics Corp., Wilsonville, OR*
Aart De Geus - CEO, *Synopsys, Inc., Mountain View, CA*
Jackson Hu - CEO, *UMC Corp., Hsinchu, Taiwan*

EDA Business Forum Luncheon - **Ballroom E** • 12:00 pm - 1:30 pm

Management Day Session 100 - Rm: **207D** - 2:00 pm - 4:00 pm
Choosing Flows and Methodologies for SoC Design
Chair: Dennis C. Wassung, Jr. - *Adams Harkness, Inc., Boston, MA*
Organizer: Yervant Zorian

100.1 EDA Flows: Best-of-Breed or Single-Vendor Solution?
Magdy Abadir - *Freescale Semiconductor, Inc., Austin, TX*

100.2 The Criteria to Select: ASIC vs. Foundry Model
Mark Bapst - *Freescale Semiconductor, Inc., Rolling Meadows, IL*

100.3 How to Choose from all the Process Nodes, IP Cores, and Other SoC Suppliers
Norbert Diesing - *PMC-Sierra, Burnaby, BC, Canada*

Management Day Session 150 - Rm: **207D** - 4:30 pm - 6:30 pm
How to Determine the Necessity for Emerging Solutions
Chair: Nic Mokhoff - *EE Times, Manhasset, NY*
Organizer: Yervant Zorian

150.1 Yield Is All That Matters: How Do You Judge Return on Investment?
Kamalesh N. Ruparel - *Cisco Systems, Inc., San Jose, CA*

150.2 How to Meet Time-to-Volume Requirements
Hao Nham - *eSilicon Corp., Bedminister, NJ*

150.3 Low-Power Design Decisions: How to Choose the Necessary Ingredients
Francesco Pessolano - *Philips Semiconductors, Eindhoven, Netherlands*

150.4 Soft Errors: Do You Need to Worry, and When? Which Applications are Affected?
Kee Sup Kim - *Intel Corp., Sacramento, CA*

Cocktail Reception - Rm: **207D** - 6:00 pm - 6:30 pm

Wireless Wednesday - June 15

New at DAC this year is "Wireless Wednesday" on Wednesday, June 15.

Wireless Wednesday offers attendees and exhibitors an opportunity to participate in a series of technical sessions, pavilion panels, special displays, and presentations highlighting wireless design. In addition to technical sessions and panels, a Wireless Showcase in Booth #1968 will display wireless products from leading IC, systems, EDA, and IP companies. DAC attendees are also invited to participate in the "Wireless Walk," which will feature exhibitors showcasing products used in the design of wireless systems, including design tools, IP, foundry services, and design services.

Look for your "Wireless Walk" passport in your attendee bag or in booth #1968. Visit participating exhibitors and receive a passport stamp. Collect enough stamps, and be entered into a drawing for a special gift. Stop by Booth #1968 for complete details.

The "Wireless Wednesday" technical sessions include a special technical session, "Emerging Directions in Wireless," featuring Bill Krenik of Texas Instruments, on cognitive radios; Jeff Gilbert of Atheros, on the MIMO approach to wireless LAN; Ahmad Bahai of National Semiconductor, on ultra-low-energy transceivers for personal area networks; and Clark Nguyen of DARPA, on RF-MEMS. Another special technical session, the annual "Best of Wireless at ISSCC," will spotlight four papers selected from the 2005 International Solid-State Circuits Conference on wireless designs.

Three presentations are scheduled on the complexity of wireless systems together with the resource constraints, such as area, power, and cost, that require the use of advanced design methods. The first, "Design Methodology for Wireless Nodes with Printed Antennas," by Jean-Samuel Chenard, McGill University, Montreal, Canada, will discuss the use of EM simulators with PCB design tools. The second presentation, "MP Core: Algorithm and Design Techniques for Efficient Channel Estimation in Wireless Applications," by Yan Meng, University of California, Santa Barbara, will describe design steps for a parameterizable IP core for a wireless channel estimation engine. The final presentation, "From Myth to Methodology: Cross-Layer Design for Energy-Efficient Wireless Communication" by Wolfgang Eberle, IMEC, will present cross-layer system design methods to combine low power with flexibility in radios.

Wireless Wednesday also includes three industry-led discussions in the DAC Pavilion. The first, "Wireless Design: Can You Hear Me Now?" features panelists John Kaewell, Interdigital Communications, Inc; Mark Kent, Broadcom Corp.; and Ken Tallo, Intel Corp., discussing how EDA is addressing wireless development needs. Two "Perspectives on Wireless" presentations feature Gadi Singer, Intel Corp., on the future of wireless technology in a wirelessly connected world and Mike Muller, CTO of ARM, as "The Wireless Carnac the Magnificent," discussing the state of the art of wireless devices and providing a vision of the wireless world of the future.

DAC Pavilion

DAC brings its technical program to the exhibit floor through live panel discussions and presentations in the DAC Pavilion. DAC attendees and exhibitors are invited to visit the DAC Pavilion in Booth 2269 to participate in these engaging technical presentations. Sessions are scheduled daily Monday, June 13 - Thursday, June 16.

Monday, June 13 • 9:30 am - 10:30 am

Dataquest at DAC with Gary Smith: EDA Trends and What's Hot at DAC?

Moderator: **Shishpal Rawat** - *Intel Corp., Folsom, CA*
Panelist: **Gary Smith** - *Gartner Dataquest, San Jose, CA*

A retrospective of the ever-popular annual Sunday Gartner Dataquest EDA and semiconductor industry presentation followed by a review of the 'Hot' products at DAC for 2005 and a Q&A.

Monday, June 13 • 11:00 am - 12:00 pm

EDA: Why Invest?

Moderator: **Kathryn Kranen** - *Jasper Design Automation, Mountain View, CA*
Panelists: **Charles Hale** - *DivestCap Management Corp., New York, NY*
Mike Schuh - *Foundation Capital, Menlo Park, CA*
Jennifer Jordan - *Wells Fargo Securities , Portland, OR*

For all the criticisms aimed at EDA, it is nonetheless a critical enabler in profit creation for its customers. The EDA ecosystem occupies the forefront of design technology, without which most of today's advanced electronic products could not exist. So, when can we expect to exceed the $4B revenue cap, and what will be the key drivers and inhibitors to such growth?

Monday, June 13 • 1:00 pm - 2:00 pm

Ask the CTO: Everything You Wanted to Know but Were Afraid to Ask

Moderator: **Kurt Keutzer** - *Univ. of California, Berkeley, CA*
Panelists: **Chris Malachowsky** - *NVIDIA Corp., Santa Clara, CA*
Raul Camposano - *Synopsys, Inc., Mountain View, CA*
Ted Vucurevich - *Cadence Design Systems, Inc., San Jose, CA*

Following last year's successful "Ask the CTO" panel, this year's group will address designers' leading-edge design issues, including design-for-yield and low power at 90 and 65 nm, ASIC vs. Structured ASIC vs. FPGA, IP integration, and the practicality of ESL design.

Monday, June 13 • 3:00 pm - 4:00 pm

EDA Serial Acquirees: You Can Run, but You Can't Hide

Moderator: **Jim Hogan** - *Telos Venture Partners, Palo Alto, CA*
Panelists: **Simon Davidmann** - *Imperas, Inc., Palo Alto, CA*
Paul Huang - *Novas Software, Inc., San Jose, CA*
Joe Sawicki - *Mentor Graphics Corp., Wilsonville, OR*
Veronica Watson - *Cadence Design Systems, Inc., San Jose, CA*

Over and over again, top entrepreneurs leave large EDA companies to found start-up companies only to be reacquired time and time again. Is this a sound strategy? Why can't they find satisfaction at a large EDA company? Why can't large EDA companies hold on to these people? Are they seeking an environment that fosters and rewards innovation? Or are they just after a fast buck? Four serial acquirees spill their guts.

Monday, June 13 • 4:15 pm - 5:15 pm

IP Interoperability - Making the Pieces Fit

Moderator: **Michael Santarini** - *EDN, San Jose, CA*
Panelists: **Joachim Kunkel** - *Synopsys, Inc., Mountain View, CA*
Drew Wingard - *Sonics, Inc., Mountain View, CA*
Wolfgang Hoeld - *National Semiconductor, Fuerstenfeldbruck, Germany*

As designers use more and more IP to create their SoCs, making it all work together is an increasingly important challenge. Who's going to address this challenge? IP vendors? Tool vendors? Both? Is the answer just bigger building blocks? What's necessary to make all this IP plug-and-play quickly and easily in SoCs?

DAC Pavilion

Tuesday, June 14 • 10:15 am - 11:00 am

DFM - A Reality Check

Moderator: **Nitin Deo** - *Ponté Solutions, Mountain View, CA*
Panelists: **Vijay Pitchumani** - *Intel Corp., Santa Clara, CA*
Gary Maier - *IBM Corp., Hopewell Junction, NY*
Karen Brotzman - *QUALCOMM, Inc., San Diego, CA*

Fabbed and fabless semiconductor companies will discuss what is truly needed from the DFM tool suppliers to solve the challenges of design for manufacturability which would improve yield and prevent catastrophic failure due to the effects of lithography or silicon variability issues. The panelists will discuss the pros and cons of commercially available DFM solutions employed at their companies and prioritize their future needs.

Tuesday, June 14 • 11:30 am - 12:15 pm

ESL: Is it Just MATLAB® and Excel Spreadsheets?

Moderator: **Grant Martin** - *Tensilica, Inc., Santa Clara, CA*
Panelists: **Charles Le** - *NASA's Jet Propulsion Lab, Pasadena, CA*
Vili Tamas - *Intel Corp., Chandler, AZ*
Maurizio Vitale - *Philips Semiconductors, Pittsburgh, PA*

Today's SoCs are deploying increasingly compute intensive algorithms that are often implemented in dedicated hardware. The need to rapidly and efficiently design from a high-level description to RTL has never been greater, but is MATLAB® really the only game in town, as Gartner Dataquest figures might suggest? Or, are there alternative methodologies challenging MATLAB's historic dominance in ESL algorithm design?

Tuesday, June 14 • 1:00 pm - 1:45 pm

A Conversation with the 2005 Recipient of the Marie R. Pistilli Women in EDA Achievement Award

Moderator: **Peggy Aycinena** - *EDA Confidential, San Mateo, CA*
Panelists: **Kathryn Kranen** - *Jasper Design Automation, Mountain View, CA*
Telle Whitney - *Anita Borg Institute for Women and Technology, Palo Alto, CA*
Alisa Yaffa - *Synplicity, Inc., Sunnyvale, CA*

Why is EDA a good place for women to succeed as leaders? How do women uniquely create cultural change in their organizations? How can a women-friendly culture be created? Peggy Aycinena will interview Kathryn Kranen, the 2005 recipient of the Marie R. Pistilli Women in EDA achievement award; Telle Whitney, the chair of WWINDA; and Alisa Yaffa for their insights, recommendations, and successes.

Tuesday, June 14 • 2:00 pm - 2:45 pm

Is There No Way Out for IP Vendors?

Moderator: **Ed Sperling** - *Electronic News, San Jose, CA*
Panelists: **Simon Segars** - *ARM Ltd., Cambridge, UK*
John Chilton - *Synopsys, Inc., Mountain View, CA*
Jordan Selburn - *iSupply Corp., San Jose, CA*

A panel of executives from the top IP companies discusses the future of IP business in a climate where designers continue to consolidate their IP purchases to a few trusted suppliers, driving vendor consolidation in the market. Where are the opportunities for growth in IP? Is consolidation the only way out for IP vendors? Is the cost of quality making it difficult for vendors to survive? Can designers afford the quality they want?

Tuesday, June 14 • 4:00 pm - 4:45 pm

The Real Cost of Linux

Moderator: **Lauren Sarno** - *Citigate Cunningham, Palo Alto, CA*
Panelists: **Mike Evans** - *Red Hat, Inc., Raleigh, NC*
Mark Noneman - *Cadence Design Systems, Inc., San Jose, CA*
Tom Fisher - *QUALCOMM, Inc., San Diego, CA*

When Linux first appeared in the EDA landscape, it posed a viable alternative to proprietary operating systems. Linux "free"dom was appealing to EDA vendors and customers alike. Initially offering a cost-effective OS for server farms, Linux popularity for EDA began to grow rapidly until it became the #1 OS for EDA applications. There are costs associated with any OS, and these costs are not just the sticker price of a license. At what price does EDA have Linux "free"dom?

DAC Pavilion

Wednesday, June 15 • 10:00 am - 10:45 am

Student Design Contest Award Presentations

Moderators: **David Greenhill** - *Sun Microsystems, Inc., Sunnyvale, CA*
Alan Mantooth - *Univ. of Arkansas, Fayetteville, AR*

Presentation of winners of the Student Design Contest, sponsored by the Design Automation Conference and the International Solid State Circuits Conference (ISSCC).

Wednesday, June 15 • 11:15 am - 12:00 pm

Verification Success: Users' Secret Sauce

Moderator: **Alan Hu** - *Univ. of British Columbia, Vancouver, Canada*
Panelists: **Somdipta Basu Roy** - *Texas Instruments, Inc., Dallas, TX*
John Andrusiak - *SunMicrosystems, Inc., San Diego, CA*
Qasim Shami - *LSI Logic, Milpitas, CA*

Today's leading chip and system companies are faced with ever increasing verification challenges. This all-user panel will discuss how testbench methodologies have been one of the key secrets to making their verification successful, as well as explore why the testbench is so important and what role coverage plays in the verification flow. Panelists will also explore other aspects of the verification process that can impact productivity, quality, and predictability.

Wednesday, June 15 • 1:00 pm - 2:00 pm

Wireless Design: Can You Hear Me Now?

Moderator: **N. Charles Podaras** - *Consultant, Portola Valley, CA*
Panelists: **John Kaewell** - *Interdigital Communications, Inc., King Of Prussia, PA*
Mark Kent - *Broadcom Corp., Irvine, CA*
Ken Tallo - *Intel Corp., Sacramento, CA*

What is the biggest challenge for today's wireless chip companies? What makes their designs unique? How do they accelerate development? How much of their intellectual property is in software versus in hardware? Is EDA offering solutions to their problems? Panelists identify and discuss their wireless development needs, how EDA is addressing these needs today, and what is needed tomorrow.

Wednesday, June 15 • 2:15 pm - 3:15 pm

Perspectives on Wireless I: Gadi Singer Sings

Moderator: **Jan Rabaey** - *Univ. of California, Berkeley, CA*
Panelist: **Gadi Singer** - *Intel Corp., Santa Clara, CA*

Communications and computing are converging at the platform level on devices such as cell phones, notebooks, and consumer electronics products. These converged platforms represent a new level of challenge in aspects of computing/communications co-design, validation, and integration in particular as it relates to wireless solutions. In addition, the need to support multiple radios increases the number of analog circuits in close proximity to potentially noisy IC circuits. High mobility - as reflected in very low power and tight form factors - creates an additional set of constraints. Tool developers and IC designers need to further their understanding of the new frontiers and create platform-oriented design solutions for the multiple emerging categories of converged devices.

Wednesday, June 15 • 4:00 pm - 4:45 pm

Perspectives on Wireless II: Mike Muller, "The Wireless Carnac The Magnificent"

Moderator: **Rich Goldman** - *Synopsys, Inc., Mountain View, CA*
Panelist: **Michael Muller** - *ARM Ltd., Cambridge, UK*

As ARM's CTO, Mike Muller is at the heart of the wireless revolution. Mike will discuss the state of the art of wireless devices, and provide a vision of the wireless world of the future. Mike's aggressive and far-reaching predictions have been proven correct time and time again. Mike will review future devices and capabilities that seem fantastic today, but will become commonplace in the not-too-distant future.

Thursday, June 16 • 10:00 am - 10: 45 am

The Business of Standards

Moderator: **Gabe Moretti** - *Consultant, Venice, FL*
Panelists: **Sean Murphy** - *PicoCraft Design Systems, Inc., San Jose, CA*
Karen Bartleson - *Synopsys, Inc., Colorado Springs, CO*
Dave Kelf - *Novas Software, Inc., San Jose, CA*

EDA consumers and EDA developers look at the problem of interoperability differently. Standards can define how you want to compete in the marketplace; i.e., what you choose to commoditize vs. what you don't. There is obviously a technical aspect to standardization, but there is also a critical business angle to consider. This panel can help the audience to look at the business problem from a range of perspectives. It can help attendees think about why you engage in standards efforts and what your objectives should be.

Thursday, June 16 • 11:00 am - 11:45 am

Did Assertions Help You C.Y.A. on Your Last Design?

Moderator: **David Maliniak** - *Electronic Design Magazine, Paramus, NJ*
Panelists: **Curt Widdoes** - *Mentor Graphics Corp., San Jose, CA*
Wolfgang Ecker - *Infineon Technologies, AG, Munich, Germany*
Carey Kloss - *Cisco Systems, Inc., San Jose, CA*

How assert i ve can designers be when using assertions? Are assertions the “holy grai l” of ver ification? Do they significantly help reduce design respins and improve first pass silicon success? Find out from industry leaders how designers are using cove rage-based verification, and the benefits and results they have seen.

Thursday, June 16 • 12:00 pm - 12:45 pm

Software Piracy: Can the EDA Industry Survive It?

Moderator: **Walden C. Rhines** - *Mentor Graphics Corp., Wilsonville, OR*
Panelists: **LaurieAtkinson** - *Business Software Alliance, Washington, DC*
Larry Disenhof - *Cadence Design Systems, Inc., Chelmford, MA*
Suresh Balasubramanian - *MacroVision , Santa Clara, CA*

It is estimated that 36% of the world’s software is pirated. With the continuing globalization of EDA software design tool use and technology advances that enables a worldwide virtual design network, the potential for EDA industry-specific software piracy increases. This panel will elicit and discuss the challenges facing the EDA and design community as it relates to piracy, and talk about what can be done to address or mitigate the issues ra i s e d .

Monday, June 13

UML for SoC Design Workshop: Sunday, June 12, 9:00 am - 6:00 pm, Rm: **207AB**

Monday, June 13 — Free Monday Exhibit Hours 9:00 am - 6:00 pm

	210AB	211AB	207D	207AB	208A	Booth #2269
9:00	**Tutorial 1** Statistical Performance Analysis and Optimization of Digital Circuits (Continental Breakfast 8:00 am - 9:00 am)	**Hands-on Tutorial** Tera Systems RTL Handoff Technology *Tera Systems, Inc.*				**DAC Pavilion**
10:00					Introduction to Chips and EDA for a Non-Technical Audience Workshop, 10:00 am - 12:00 pm	Dataquest at DAC with Gary Smith **9:30 am - 10:30 am**
12:00						EDA: Why Invest? **11:00 am - 12:00 pm**
1:00	**Lunch**		Integrated Design Systems Workshop 12:00 pm - 5:00 pm	Workshop for Women in Design Automation Lunch: 1:00 pm – 2:00 pm Keynote and Panel: 2:00 pm – 5:00 pm		Ask the CTO **1:00 pm - 2:00 pm**
2:00	**Tutorial 1 (cont.)** Statistical Performance Analysis and Optimization of Digital Circuits	**Hands-on Tutorial** Enabling RTL Handoff via Predictive Development *Atrenta, Conexant*				EDA Serial Acquirees: You Can Run, but You Can't Hide **3:00 pm - 4:00 pm**
5:00						IP Interoperability – Making the Pieces Fit **4:15 pm - 5:15 pm**

Tutorial 1: Statistical Performance Analysis and Optimization of Digital Circuits - see page 38

Hands-on Tutorial: Tera Systems RTL Handoff Technology *Tera Systems* - see page 45

Hands-on Tutorial: Enabling RTL Handoff via Predictive Development *Atrenta, Conexant* - see page 46

UML for SoC Design Workshop: - see page 41

Integrated Design Systems Workshop: - see page 42

Workshop for Women in Design Automation: Cultural Evolution: Keeping Pace with Organizational Diversity - see page 43

Introduction to Chips and EDA for a Non-Technical Audience: see page 44

visit the DAC web site @ www.dac.com for more details

Opening Session & Keynote

Opening Remarks: **William H. Joyner, Jr.** - General Chair, 42nd DAC **Ballroom ABC**

Awards Presented by: **Robert Walker**
ACM/SIGDA Representative

Al Dunlop
2005 IEEE/CASS/CANDE Representative

Awards/Scholarships

- **Marie R. Pistilli Women in EDA Achievement Award**
- **P.O. Pistilli Undergraduate Scholarships (ACSEE)**
- **DAC Graduate Scholarships**
- **ACM/TODAES Best Paper Award**
- **Phil Kaufman Award**
- **2005 IEEE Fellows**
- **IEEE/CASS Donald O. Pederson Award**
- **Darlington Award**
- **Industrial Pioneer Award**
- **Outstanding Young Author Award**
- **VLSI Transaction Best Paper Award**

Keynote Address:

How Does One Define "Technology" Now That Classical Scaling Is Dead (and Has Been for Years)?

Bernard S. Meyerson - *IBM Fellow, Vice President and Chief Technologist, Systems and Technology Group, IBM Corp.*

Tuesday June 14

8:30 to 10:15

All speakers are indicated in bold

S - indicates short paper

ß - indicates best paper candidate

session areas indicated on page 14

Tuesday June 14

10:30 to 12:00

All speakers are indicated in bold

S - indicates short paper

ß - indicates best paper candidate

session areas indicated on page 14

Session 1

Rm: **207ABC**

PANEL: DIFFERENTIATE AND DELIVER: LEVERAGING YOUR DESIGN AND MANUFACTURING PARTNERS FROM PRODUCT CONCEPT TO PRODUCTION

Chair: Jay Vleeschhouwer - *Merrill Lynch, New York, NY*
Organizers: Rich Goldman, David Park

Semiconductor companies face many key questions when developing a new product: Is there a serviceable market need? Do I have a product idea that is unique and differentiated? What parts of my design do I "make" vs. "buy"? What is the right process node for the first implementation? More so than ever before, the answers to these questions are influenced by the EDA, IP and Foundry partners with whom the semiconductor companies collaborate. Collectively, these companies must align their own core competencies with those of the semiconductor company to create a product with the optimal combination of performance, price, and time-to-market. In this panel, the CEOs of the three major EDA vendors, along with peers from the IP and manufacturing areas, discuss these fundamental questions as well as the challenges of working together to help customers successfully bring new products to market.

Panelists: **Warren East** - *ARM Ltd., Cambridge, UK*
Michael J. Fister - *Cadence Design Systems, Inc., San Jose, CA*
Walden C. Rhines - *Mentor Graphics Corp., Wilsonville, OR*
Aart De Geus - *Synopsys, Inc., Mountain View, CA*
Jackson Hu - *United Microelectronics Corp., Hsinchu, Taiwan*

Session 2

Rm: **210CD**

SPECIAL SESSION: ERROR-TOLERANT DESIGN

Chair: Sarma Vrudhula - *Univ. of Arizona, Tucson, AZ*
Organizers: Krishnendu Chakrabarty, Sarma Vrudhula

Industry presentations on various aspects of soft errors - causes, impacts, and mitigation. Highlight conclusions of upcoming workshop on soft errors.

2.1 Logic Soft Errors in sub-65 nm Technologies: Design and CAD Challenges

Subhasish Mitra, Tanay Karnik, Norbert Seifert - *Intel Corp., Hillsboro, OR*
Ming Zhang - *Intel Corp., Folsom, CA*

2.2 SEU-Tolerant Device, Circuit and Processor Design

Bill Heidergott - *General Dynamics Decision Systems, Scottsdale, AZ*

2.3 System Effects of Transient Particle Induced Upsets

Pia N. Sanda, Ethan H. Cannon, Scott Swaney, David M. Cole - *IBM Corp., White Plains, NY*

Session 3

Rm: **210AB**

MICROARCHITECTURE-LEVEL POWER ANALYSIS AND OPTIMIZATION TECHNIQUES

Chair: Mary Jane Irwin - *Penn State Univ., University Park, PA*

Organizers: Sujit Dey, Trevor Mudge

This session covers various topics related to energy optimization and modeling at the microarchitecture-architecture boundary.

3.1 Variability and Energy Awareness: A Microarchitecture-Level Perspective

Diana Marculescu, Emil Talpes - *Carnegie Mellon Univ., Pittsburgh, PA*

3.2 Energy-Efficient Physically Tagged Caches for Embedded Processors with Virtual Memory

Peter D. Petrov - *Univ. of Maryland, College Park, MD*
Daniel Tracy, Alex Orailoglu - *Univ. of California at San Diego, La Jolla, CA*

3.3s Hybrid Simulation for Embedded Software Energy Estimation

Anish Muttreja - *Princeton Univ., Princeton, NJ*
Anand Raghunathan, Srivaths Ravi - *NEC Laboratories America, Princeton, NJ*
Niraj K. Jha - *Princeton Univ., Princeton, NJ*

3.4s Cooperative Multithreading on Embedded Multiprocessor Architectures Enables Energy-Scalable Design

Patrick R. Schaumont, **Bo-Cheng Charles Lai** - *Univ. Of California, Los Angeles, CA*
Wei Qin - *Boston Univ., Boston, MA*
Ingrid Verbauwhede - *Univ. Of California, Los Angeles, CA*

Session 4

Rm: **209AB**

LEAKAGE ANALYSIS AND OPTIMIZATION

Chair: Yu Cao - *Arizona State Univ., Tempe, AZ*

Organizers: Tanay Karnik, Chandu Visweswariah

This session presents several different techniques for leakage analysis and optimization. The first paper presents a technique for total power reduction using gate sizing and multiple VT. The second paper describes a technique for reducing the short-circuit current when MTCMOS circuits transition from sleep to active state. The third paper dynamically determines the optimal reverse body bias for leakage control. The last paper shows a new technique of gate replacement for leakage reduction.

4.1 Total Power Reduction in CMOS Circuits via Gate Sizing and Multiple Threshold Voltages

Feng Gao, John P. Hayes - *Univ. of Michigan, Ann Arbor, MI*

4.2 An Effective Power Mode Transition Technique in MTCMOS Circuits

Afshin Abdollahi - *Univ. of Southern California, Los Angeles, CA*
Farzan Fallah - *Fujitsu Labs of America, Inc., Sunnyvale, CA*
Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

4.3s A Self-adjusting Scheme to Determine the Optimum RBB by Monitoring Leakage Currents

Nikhil Jayakumar - *Texas A&M Univ., College Station, TX*
Sandeep Dhar - *National Semiconductor Corp., Longmont, CO*
Sunil Khatri - *Texas A&M Univ., College Station, TX*

4.4s Enhanced Leakage Reduction Technique by Gate Replacement

Lin Yuan, Gang Qu - *Univ. of Maryland, College Park, MD*

Session 5

Rm: **208AB**

ANALOG MACROMODELING

Chair: Georges Gielen - *Katholieke Universiteit, Leuven, Belgium*

Organizers: Geert Van Der Plas, Helmut Graeb

This session presents recent advances in automatic generation of macromodels for analog circuits. The first paper shows piecewise polynomial nonlinear modeling of I/O buffers. The second paper describes a new method to create a structural model by decoupling internal feedback loops. The third paper presents a new response surface modeling technique that combines support vector machines and dynamic learning schemes.

5.1 Automated Nonlinear Macromodeling of Output Buffers for High-Speed Digital Applications

Ning Dong, Jaijeet Roychowdhury - *Univ. of Minnesota, Minneapolis, MN*

5.2 Systematic Development of Analog Circuit Structural Macromodels Through Behavioral Model Decoupling

Ying Wei, Alex Doboli - *State Univ. of New York, Stony Brook, NY*

5.3 A Combined Feasibility and Performance Macromodel for Analog Circuits

Mengmeng Ding, Ranga Vemuri - *Univ. of Cincinnati, Cincinnati, OH*

Tuesday June 14

2:00 to 4:00

All speakers are indicated in bold

S - indicates short paper

ß - indicates best paper candidate

session areas indicated on page 14

Session 6

Rm: **207ABC**

PANEL: ESL: TALES FROM THE TRENCHES

Chair: David Maliniak - *Electronic Design, Paramus, NJ*
Organizer: Francine Bacchini

ESL design has arrived - but can ESL provide the bridge from systems to silicon? Hear from real-world designers as to what works, what doesn't, and what the gaps are in the methodology and tool offerings. Panelists from military/aerospace, storage area networks (SAN), wireless communications, and consumer electronics industry segments will share their experiences, lessons learned, and further needs.

Panelists:

Terry Doherty - *Emulex Corp., Bothell, WA*
Peter McShane - *Northrop Grumman Space Technology, Redondo Beach, CA*
Suhas A. Pai - *QUALCOMM Incorporated, San Diego, CA*
Sriram Sundararajan - *Texas Instruments, Inc., Dallas, TX*
Soo-Kwan Eo - *Samsung Electronics, Yong-In, Korea*
Pascal Urard - *STMicroelectronics, Crolles, France*

Session 7

Rm: **210CD**

STATISTICAL TIMING ANALYSIS

Chair: Vinod Kariat - *Cadence Design Systems, Inc., San Jose, CA*
Organizers: Joel Phillips, Kenneth Shepard

This session describes new advances in statistical static timing analysis. In particular, these papers describe techniques to handle nonlinear and non-Gaussian parameters and preserve correlations, including both process dependence and reconvergent circuit paths.

7.1 Parameterized Block-Based Statistical Timing Analysis with Non-Gaussian Parameters and Nonlinear Delay Functions
Hongliang Chang - *Univ. of Minnesota, Minneapolis, MN*
Vladimir Zolotov, Chandu Visweswariah - *IBM Corp., Yorktown Heights, NY*
Sambasivan Narayan - *IBM Corp., Essex Jct., VT*

7.2 Correlation-Aware Statistical Timing Analysis with Non-Gaussian Delay Distributions
Yaping Zhan, Andrzej J. Strojwas, Xin Li, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*
David Newmark, Mahesh Sharma - *Advanced Micro Devices, Inc., Austin, TX*

7.3 Correlation-Preserved Non-Gaussian Statistical Timing Analysis with Quadratic Timing Model
Lizheng Zhang, Weijen Chen, Yuhen Hu, John A. Gubner - *Univ. of Wisconsin, Madison, WI*
Charlie Chung-Ping Chen - *National Taiwan Univ., Taipei , Taiwan*

7.4 A General Framework for Accurate Statistical Timing Analysis Considering Correlations
Vishal Khandelwal, Ankur Srivastava - *Univ. of Maryland, College Park, MD*

Session 8

Rm:**210AB**

EMBEDDED SOFTWARE

Chair: Rainer Leupers - *RWTH Aachen Univ., Aachen , Germany*
Organizer: Lothar Thiele

With increasing chip density and application complexity, embedded systems now include multiple processors and sophisticated memory hierarchies (caches, multiple memory banks, etc). It is imperative that embedded software fully exploits parallelism and uses the memory hierarchy to increase performance and reduce power consumption. At the same time, the applications increasingly include real-time constraints, and therefore, task scheduling and run-time estimation techniques are becoming mandatory.

ß 8.1 Locality-Conscious Workload Assignment for Array-Based Computations in MPSOC Architectures
Feihui Li, Mahmut Kandemir - *Pennsylvania State Univ., University Park, PA*

8.2s Automatic Scenario Detection for Improved WCET Estimation
Valentin S. Gheorghita, Sander Stuijk, Twan Basten, Henk Corporaal - *Eindhoven Univ. of Technology, Eindhoven, Netherlands*

8.3 Memory Access Optimization Through Combined Code Scheduling, Memory Allocation, and Array Binding in Embedded System Design
Jungeun Kim - *KAIST, Daejeon, South Korea*
Taewhan Kim - *Seoul National Univ., Seoul, South Korea*

8.4 Dynamic Slack Reclamation with Procrastination Scheduling in Real-Time Embedded Systems
Ravindra R. Jejurikar - *Univ. of California , Irvine, CA*
Rajesh Gupta - *Univ. of California at San Diego, La Jolla, CA*

Session 9

Rm: **209AB**

ADVANCES IN DESIGN-FOR-TESTABILITY METHODS

Chair: Tom Williams - *Synopsys, Inc., Boulder, CO*
Organizers: Erik Jan Marinissen, Patrick Girard

This session presents novel scan-based techniques that improve test quality, reduce test costs, and ensure secure testable ICs.

ß 9.1 Response Compression with Unlimited Number of Unknowns Using a New LFSR Architecture

Erik H. Volkerink - *Agilent Technologies, Inc., San Jose, CA*
Subhasish Mitra - *Intel Corp., Folsom, CA*

9.2 Multi-Frequency Wrapper Design and Optimization for Embedded Cores Under Average Power Constraints

Qiang Xu, Nicola Nicolici - *McMaster Univ., Hamilton, Canada*
Krishnendu Chakrabarty - *Duke Univ., Durham, NC*

9.3 N-Detection Under Transparent-Scan

Irith Pomeranz - *Purdue Univ., West Lafayette, IN*

9.4 Secure Scan: A Design-for-Test Architecture for Crypto Chips

Bo Yang - *Polytechnic Univ., Brooklyn, NY*
Kaijie Wu - *Univ. of Illinois, Chicago, IL*
Ramesh Karri - *Polytechnic Univ., Brooklyn, NY*

Session 10

Rm: **208AB**

ADVANCES IN BOUNDARY ELEMENT METHODS FOR PARASITIC EXTRACTION

Chair: J. Eric Bracken - *Ansoft Corp., Pittsburgh, PA*
Organizers: Yehea Ismail, Sachin S. Sapatneker

This session presents advances in parasitic extraction based on boundaryelement methods. The first paper presents a surface-volume method for inhomogeneous substrates. The second paper presents a full-wave technique for impedance conduction over layered substrates. The third paper presents an extraction approach for spatially distributed 3D circuit models. The fourth paper presents a direct multilevel method for fast capacitance extraction, and the fifth paper presents a reordering and transformation method for accelerating capacitance extraction.

ß 10.1 A Green Function-Based Parasitic Extraction Method for Inhomogeneous Substrate Layers

Chenggang Xu - *Oregon State Univ., Corvallis, OR*
Ranjit Gharpurey - *Univ. of Michigan, Ann Arbor, MI*
Terri Fiez, Kartikeya Mayaram - *Oregon State Univ., Corvallis, OR*

10.2 Analysis of Full-Wave Conductor System Impedance Over Substrate Using Novel Integration Techniques

Xin Hu, Jung Hoon Lee, Jacob White, Luca Daniel - *Massachusetts Institute of Tech., Cambridge, MA*

10.3 Spatially Distributed 3D Circuit Models

Michael Beattie, Hui Zheng, Byron Krauter, Anirudh Devgan - *IBM Corp., Austin, TX*

10.4s DiMES: Multilevel Fast Direct Solver Based on Multipole Expansions for Parasitic Extraction of Massively Coupled 3D Microelectronic Structures

Dipanjan Gope, Indranil Chowdhury, Vikram Jandhyala - *Univ. of Washington, Seattle, WA*

10.5s ICCAP: A Linear Time Sparse Transformation and Reordering Algorithm for Three-Dimensional BEM Capacitance Extraction

Rong Jiang, Charlie Chung-Ping Chen - *Univ. of Wisconsin, Madison, WI*
Yi-Hoa Chang - *National Taiwan Univ., Taipei, Taiwan*

Session 100

Rm: **207D**

CHOOSING FLOWS AND METHODOLOGIES FOR SOC DESIGN

Chair: Dennis C. Wassung, Jr. - *Adams Harkness, Inc., Boston, MA*
Organizer: Yervant Zorian

Moving to new semiconductor technology nodes can dramatically impact the business performance of the SoC company, and its age-old design and manufacturing flows and methodologies. It can also significantly affect its choices of suppliers. This session will provide an overview of changing needs and corresponding management decision criteria to make the right choices from a pool of alternate options.

100.1 EDA Flows: Best-of-Breed or Single-Vendor Solution?

Magdy Abadir - *Freescale Semiconductor, Inc., Austin, TX*

100.2 The Criteria to Select: ASIC vs. Foundry Model

Mark Bapst - *Freescale Semiconductor, Inc., Rolling Meadows, IL*

100.3 How to Choose from All the Process Nodes, IP Cores, and Other SoC Suppliers

Norbert Diesing - *PMC-Sierra, Burnaby, BC, Canada*

100.4 Soft Errors: Do You Need to Worry, and When? Which Applications are Affected?

Kee Sup Kim - *Intel Corp., Sacramento, CA*

Tuesday June 14

4:30 to 6:30

All speakers are indicated in bold

S - indicates short paper

ß - indicates best paper candidate

session areas indicated on page 14

Session 11

Rm: **207ABC**

PANEL: DFM RULES!

Chair: Naveed Sherwani - *Open-Silicon, Sunnyvale, CA*
Organizer: Susan Lippincott Mack

At 90 nm, yields appeared unpredictable. Two chips designed with the same methodology and design rules deliver completely different manufacturing yields. This panel will discuss the reasons for this phenomenon and talk about future trends in DFM that will need to be addressed for success below 100 nm.

Panelists:

Atul Sharan - *Clear Shape Technologies, Inc., Sunnyvale, CA*

Alex Alexanian - *Ponté Solutions, Inc., Mountain View, CA*

Harold Lehon - *KLA-Tencor Corp., San Jose, CA*

Peter Rabkin - *Xilinx, Inc., San Jose, CA*

Carlo Guardiani - *PDF Solutions, Inc., San Jose, CA*

Premal Buch - *Magma Design Automation, Inc., Santa Clara, CA*

Session 12

Rm: **210CD**

RECENT ADVANCES IN SIGNAL INTEGRITY

Chair: Eli Chiprout - *Intel Corp., Chandler, AZ*
Organizers: Dusan Petranovic, Lei He

This session describes advances in a range of topics in the signal integrity area. The first paper discusses an efficient approach to budgeting decoupling capacitance in order to improve power grid integrity. The next two papers discuss clock network optimization using register placement and a novel opposite-phase scheme to reduce peak current demands, respectively. The next paper details an effective capacitance model for fast noise analysis. The final paper presents an approach to selectively inserting hardened flip-flops in a general circuit to improve robustness while maintaining timing/area constraints.

ß 12.1 Partitioning-Based Approach to Fast On-Chip Decap Budgeting and Minimization
Hang Li, Zhenyu Qi, Sheldon Tan - *Univ. of California, Riverside, CA*

12.2 Navigating Registers in Placement for Clock Network Minimization
Yongqiang Lu - *Tsinghua Univ., Beijing, China*
C. N. Sze - *Texas A&M Univ., College Station, TX*
Xianlong Hong, Qiang Zhou, Yici Cai, Liang Huang - *Tsinghua Univ., Beijing, China*
Jiang Hu - *Texas A&M Univ., College Station, TX*

12.3s Minimizing Peak Current via Opposite-Phase Clock Tree
Yow-Tyng Nieh, **Shih-Hsu Huang** - *Chung Yuan Christian Univ., Chung Li, Taiwan*
Sheng-Yu Hsu - *Industrial Technology Research Institute, Hsin Chu, Taiwan*

12.4s A Noise-Driven Effective Capacitance Method With Fast Embedded Noise Rule Calculation for Functional Noise Analysis
Haihua Su, David J. Widiger, Chandramouli V. Kashyap, Frank Y. Liu, Byron Krauter - *IBM Corp., Austin, TX*

12.5 Constraint-Aware Robustness Insertion for Optimal Noise-Tolerance Enhancement in Digital VLSI Circuits
Chong Zhao, Yi Zhao, Sujit Dey - *Univ. of California at San Diego, La Jolla, CA*

Session 13

Rm: **210AB**

PHYSICAL CONSIDERATIONS IN HIGH-LEVEL SYNTHESIS

Chair: Steven M. Burns - *Intel Corp., Portland, OR*
Organizers: Gila Kamhi, Reinaldo Bergamaschi

This session brings together five interesting papers using physical considerations (floorplanning and layout) in high-level synthesis. The first two papers deal with temperature and power issues in high-level design; the third paper considers floorplanning together with high-level synthesis for area and power optimization; the fourth paper deals with encoding techniques for power reduction; and the fifth paper uses specific layout techniques for watermarking.

ß 13.1 Temperature-Aware Resource Allocation and Binding in High-Level Synthesis
Rajarshi Mukherjee, Seda Ogrenci Memik, Gokhan Memik - *Northwestern Univ., Evanston, IL*

13.2 Leakage Power Optimization with Dual-Vth Library in High-LevelSynthesis
Xiaoyong Tang - *Magma Design Automation, Inc., Santa Clara, CA*
Hai Zhou - *Northwestern Univ., Evanston, IL*
Prith Banerjee - *Univ. of Illinois, Chicago, IL*

13.3 Incremental Exploration of the Combined Physical and Behavioral Design Space
Zhenyu Gu, Jia Wang, Robert P. Dick, Hai Zhou - *Northwestern Univ., Evanston, IL*

13.4s Sign Bit Reduction Encoding For Low Power Applications
Mohsen Saneei, Ali Afzali-Kusha, **Zainolabedin Navabi**- *Univ. of Tehran, Tehran, Iran*

13.5s A Watermarking System for IP Protection by a Post-Layout Incremental Router
Tingyuan Nie, Tomowo Kisaka, Masahiko Toyonaga - *Kochi Univ., Kochi, Japan*

Session 14

Rm: **209AB**

ARCHITECTURES FOR CRYPTOGRAPHY AND SECURITY APPLICATIONS

Chair: Anand Raghunathan - *NEC-Labs America, Inc., Princeton, NJ*

Organizers: Adam Donlin, Peter Marwedel

Security is a new design dimension for embedded systems. This session considers the issue of secure embedded hardware and architectures. The first two papers discuss securing embedded systems against differential power analysis. The third and fourth papers tackle network security with intrusion detection and an encryption core for wireless communications. The last paper addresses security at the human interface to the embedded system with a hardware-accelerated fingerprint co-processor.

14.1 A Side-Channel Leakage Free Co-processor IC in .18um CMOS for Embedded AES-Based Cryptographic and Biometric Processing

Kris Tiri, David Hwang, Alireza Hodjat, Bo-Cheng Lai, Shenglin Yang, Patrick R. Schaumont, Ingrid Verbauwhede - *Univ. of California, Los Angeles, CA*

14.2 Simulation Models for Side-Channel Information Leaks

Kris Tiri, Ingrid Verbauwhede - *Univ. of California, Los Angeles, CA*

14.3 A Pattern Matching Co-processor for Network Security

Young H. Cho, William H. Mangione-Smith - *Univ. of California, Los Angeles, CA*

14.4s A High Performance Encryption Core for Wireless 3G Networks

Tomas Balderas, **Rene Cumplido** - *INAOE, Mexico*

14.5s Efficient and Secure Fingerprint-Based User Authentication for Embedded Systems

Pallav Gupta - *Princeton Univ., Princeton, NJ*
Srivaths Ravi, Anand Raghunathan - *NEC-Labs America, Inc., Princeton, NJ*
Niraj K. Jha - *Princeton Univ., Princeton, NJ*

Session 15

Rm: **208AB**

PERFORMANCE, ENERGY, AND FAULT-TOLERANCE CONSIDERATIONS FOR MPSOC DESIGNS

Chair: Gerd Ascheid - *RWTH Aachen Univ., Aachen, Germany*

Organizers: Radu Marculescu, Rainer Leupers

For hardware-software co-design, the evaluation and fine tuning of the architecture, software, and individual components represent a critical step toward matching the tight design constraints and providing quick feedback to system designers. The first three papers in this session deal with early analytical and simulation-based performance evaluation and cost-effective implementation. The last two papers present possible energy/fault-tolerance trade-offs relevant to both computation and communication infrastructure design.

15.1 Approximate VCCs: A New Characterization of Multimedia Workloads for System-level MpSoC Design

Yanhong Liu, Samarjit Chakraborty, Wei Tsang Ooi - *National Univ. of Singapore, Singapore*

15.2 Modular Domain-specific Implementation and Exploration Framework for Embedded Software Platforms

Christian Sauer, Matthias C. Gries, Soeren Sonntag - *Infineon Tech., Munich, Germany*

15.3 Simulation Based Deadlock Analysis for System Level Designs

Xi Chen - *Univ. of California, Riverside, CA*
Abhijit Davare - *Univ. of California, Berkeley, CA*
Harry Hsieh - *Univ. of California, Riverside, CA*
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*
Yosinori Watanabe - *Cadence Berkeley Labs, Berkeley, CA*

15.4s Fault and Energy-Aware Communication Mapping with Guaranteed Latency for Applications Implemented on NoC

Sorin Manolache, Petru Eles, Zebo Peng - *Linköping Univ., Linköping, Sweden*

15.5s High Performance Computing on Fault-Prone Nanotechnologies: Novel Microarchitecture Techniques Exploiting Reliability-Delay Trade-offs

Andrey Zykov, **Elias Mizan**, Margarida Jacome, Gustavo de Veciana, Ajay Subramanian - *Univ. of Texas, Austin, TX*

Session 150

Rm: **207D**

HOW TO DETERMINE THE NECESSITY FOR EMERGING SOLUTIONS

Chair: Nic Mokhoff - *EE Times, Manhasset, NY*

Organizer: Yervant Zorian

Different applications for today's chips require different types of optimizations and thus the need to adopt emerging products and solutions to meet such requirements. Optimizing for low power, for high yield, for reduced soft error or minimal bring-up time necessitate adequate trade-off analysis and technical/business decision making by management. The lead managers in this session will discuss today's emerging solutions and their economic impact.

150.1 Yield Is All That Matters: How Do You Judge Return on Investment?

Kamalesh N. Ruparel - *Cisco Systems, Inc., San Jose, CA*

150.2 How to Meet Time-to-Volume Requirements

Hao Nham - *eSilicon Corp., Bedminister, NJ*

150.3 Low-Power Design Decisions: How to Choose the Necessary Ingredients

Francesco Pessolano - *Philips Semiconductors, Eindhoven, Netherlands*

Wednesday June 15

8:30 to 10:00

All speakers are indicated in bold

S - indicates short paper

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session areas indicated on page 14

Session 16

Rm: **207ABC**

SPECIAL SESSION: CLOSING THE POWER GAP BETWEEN ASIC AND CUSTOM

Chair: Barry Pangrle - *Synopsys, Inc., Mountain View, CA*
Organizer: Dennis Sylvester

This session is balanced to provide a mixture of custom and ASIC perspectives, as well as to provide a mixture of academic and industrial perspectives. Similar sessions (focused on speed rather than power) at DAC 2000 and 2001 were well attended. The work of the presenters has refocused on power, and there are sufficient results now to give a mature perspective.

16.1 Closing the Power Gap between ASIC and Custom: An ASIC Perspective

David G. Chinnery, Kurt Keutzer - *Univ. of California, Berkeley, CA*

16.2 Explaining the Gap between ASIC and Custom Power: A Custom Perspective

Andrew Chang - *Cadence Design Systems, Inc., San Jose, CA*
William J. Dally - *Stanford Univ., Stanford, CA*

16.3 Keeping Hot Chips Cool

Ruchir Puri, Leon Stok, Subhrajit Bhattacharya - *IBM Corp., Yorktown Heights, NY*

Session 17

Rm: **210CD**

PANEL: MY GIGA HERTZ: DOES YOURS?

Chair: Rick Merritt - *EE Times, San Mateo, CA*
Organizer: Phil Dworsky

Nearly every SoC will have an interface that relies on high-speed interconnect technology. Today, designers are "comfortable" with connections that run at 100's of megahertz, but making the transition to standards like PCI Express will instantly bring them into the GHz range, introducing a whole new universe of design challenges. Designers will need to understand the challenges they'll face as well as what to look for in the solutions they acquire to add this kind of technology to their SoCs.

Panelists: John F. D'Ambrosia - *Tyco Electronics Corp., Harrisburg, PA*
Adam Healey - *Agere Systems, Inc., Allentown, PA*
Boris Litinsky - *RF Micro Devices, Inc., Greensboro, NC*
John T. Stonick - *Synopsys, Inc., Hillsboro, OR*
Joe Abler - *IBM Corp., Research Triangle Park, NC*

Session 18

Rm: **210AB**

WIRELESS SESSION: INFORMATION DESIGN METHODOLGY

Chair: Ingrid Verbauwhede - *Univ. of California Los Angeles, CA*

Organizer: Ingrid Verbauwhede

The complexity of wireless systems together with the resource constraints (area, power, cost) requires the use of advanced design methods. In this session three examples are given. The first paper describes how low cost, reliable antennas can be built on printed circuit boards using a combination of 2.5D and 3D EM simulators with PCB design tools. The second paper describes design steps used to design a parametrizable IP core for a wireless channel estimation engine. The third paper describes cross-layer system design methods to combine low power with flexibility in radios.

18.1 Design Methodology for Wireless Nodes with Printed Antennas

Jean-Samuel Chenard, Chun Yiu Chu, Zeljko Zilic, Milica Popovic - *McGill Univ., Montreal, Canada*

18.2 MP Core: Algorithm and Design Techniques for Efficient Channel Estimation in Wireless Applications

Yan Meng, Andrew P. Brown, Ronald A. Iltis, Ryan Kastner, Timothy Sherwood, Hua Lee - *Univ. of California, Santa Barbara, CA*

18.3 From Myth to Methodology: Cross-Layer Design for Energy-Efficient Wireless Communication

Wolfgang Eberle, Francky Catthoor, Bruno Bougard, Sofie Pollin - *IMEC, Leuven, Belgium*

Session 19

Rm: **209AB**

STATISTICAL OPTIMIZATION AND MANUFACTURABILITY

Chair: Chandramouli Kashyap - *IBM Corp., Austin, TX*

Organizers: Sani Nassif, Vivek De

The impact of variations on perfo rmance and power is becoming worse with technology scaling. The first three papers describe sizing algorithms that account for variations and perform statistical design optimizations to improve yield under power and timing constraints. The last paper describes alogorithms to avoid and fix antenna effect problems for yield improvement.

ß 19.1 An Efficient Algorithm for Statistical Minimization of Total Power under Timing Yield Constraints

Murari Mani - *Univ. of Texas, Austin, TX*
Anirudh Devgan - *IBM Corp., Austin, TX*
Michael Orshansky- *Univ. of Texas, Austin, TX*

19.2 Robust Gate Sizing by Geometric Programming

Jaskirat Singh, Vidyasagar Nookala, Zhi-Quan Luo, Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

19.3s Circuit Optimization Using Statistical Static Timing Analysis

Aseem Agarwal - *Univ. of Michigan, Ann Arbor, MI*
Vladimir Zolotov - *IBM Corp., Yorktown Heights, NY*
David Blaauw, Kaviraj S. Chopra - *Univ. of Michigan, Ann Arbor, MI*

19.4s An Optimal Jumper Insertion Algorithm for Antenna Effect Avoidance/Fixing

Bor-Yiing Su, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

Session 20

Rm: **208AB**

APPLICATION SPECIFIC ARCHITECTURE DESIGN TOOLS

Chair: Nikil Dutt - *Univ. of California, Irvine, CA*

Organizers: Joachim Gerlach, Margarida Jacome

This session addresses tools and methods to support design space exploration and specialization of embedded computing systems, critical towards achieving increasingly stringent performance and energy efficiency requirements. The first paper proposes an application source code micro-profiling approach for fast and accurate characterization of embedded applications during ASIP design. The second paper proposes physically-aware methods for simultaneous partitioning, scheduling, and placement of tasks on dynamically reconfigurable architectures. The third and fourth papers address fast early simulation taking advantage of evaluation reuse schemes and virtual synchronization techniques.

ß 20.1 Fine-grained Application Source Code Profiling for ASIP Design

Kingshuk Karuri, Mohammad Al Fasuque, Stefan Kraemer, Rainer Leupers, Gerd Ascheid, Heinrich Meyr - *RWTH Aachen Univ., Aachen, Germany*

20.2 Physically-Aware HW-SW Partitioning for Reconfigurable Architectures with Partial Dynamic Reconfiguration

Sudarshan Banerjee, Elaheh Bozorgzadeh, Nikil Dutt - *Univ. of California, Irvine, CA*

20.3s Performance Simulation Modeling for Fast Evaluation of Pipelined Scalar Processor by Evaluation Reuse

Ho Young Ki m, Tag Gon Kim - *KAIST, Daejeon, South Korea*

20.4s Trace-Driven HW/SW Cosimulation Using Virtual Synchronization Technique

Dohyung Kim, Youngmin Yi, Soonhoi Ha - *Seoul National Univ., Seoul, South Korea*

Wednesday June 15

10:30 to 12:00

All speakers are indicated in bold

S - indicates short paper

ß - indicates best paper candidate

session areas indicated on page 14

Session 21

Rm: **207ABC**

SPECIAL SESSION: THE TITANIC: WHAT WENT WRONG

Chair: Andrew B. Kahng - *Univ. of California at San Diego, La Jolla, CA*
Organizer: Sani Nassif

Four speakers will each give a 15-minute lament of their "problems," after which moderated and timed feedback from the audience and other speakers will give 1-minute solutions and other feedback. The session will contain focused talks on a Technology problem, a Power problem, a Reliability problem, and a Methodology problem. At the end, a prize will be given for the solution that the audience votes highest in value.

21.1 The Titanic: What Went Wrong in Technology
Paul Zuchowski - *IBM Corp., Essex Junction, VT*

21.2 The Titanic: What Went Wrong in Methodology
Ward A. Vercruysse - *Advanced Micro Devices, Inc., Sunnyvale, CA*

21.3 The Titanic: What Went Wrong in Reliability
Claude Moughanni - *Freescale Semiconductor, Inc., Austin, TX*

21.4 Bridging the Power Reduction and Estimation Gap in the Cell Processor Design Methodology
Stephen D. Posluszny - *IBM Corp., Round Rock, TX*

Session 22

Rm: **210CD**

PANEL: WIRELESS PLATFORMS: GOPS FOR CENTS AND MILLIWATTS

Chair: Jan Rabaey - *Univ. of California, Berkeley, CA*
Organizer: Francine Bacchini

Data communication has overtaken voice as the main force behind the growth in wireless. Opportunities offered by truly ubiquitous connectivity are tremendous, and are leading to revolutionary changes in the way computer, communication, and consumer systems operate and interact. Panelists will debate the various wireless implementation platforms that are breaking new ground, examining issues of efficiency, flexibility, and programming models.

Panelists: Rudy Lauwereins - *IMEC, Leuven, Belgium*
Frank Lane - *Flarion Technologies, Inc., Bedminster, NJ*
Allan Cox - *3Plus1 Technology, Inc., Saratoga, CA*
Ulrich Ramacher - *Infineon Technologies, Munich, Germany*
David Witt - *Texas Instruments, Inc., Dallas, TX*

Session 23

Rm: **210AB**

DESIGN METHODS FOR MANUFACTURABILITY ENHANCEMENTS

Chair: Nagib Z. Hakim - *Intel Corp., Santa Clara, CA*
Organizers: David Blaauw, Michael Orshansky

As we sink further below the 100 nm barrier, more second order effects are entering the design/ manufacturing interface. Optical Proximity Correction, Focus Variations, and other Resolution Enhancement Techniques conspire to lengthen the design and verification processes. The papers in this session attack this area from two distinct directions: from the design side using regularity - or from the CAD side developing algorithms that are aware of these effects.

23.1 Design Methodology for IC Manufacturability Based on Regular Logic-Bricks

Veerbhan Kheterpal, Vyacheslav V. Rovner, Thiago G. Hersan, Dipti Motiani, Yoichi Takegawa, Andrzej J. Strojwas, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

ß 23.2 Advanced Timing Analysis Based on Post-OPC Extraction of Critical Dimensions

Jie Yang - *Univ. of Michigan, Ann Arbor, MI*
Luigi Capodieci - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Dennis M. Sylvester - *Univ. of Michigan, Ann Arbor, MI*

23.3s Self-compensating Design for Focus Variation

Puneet Gupta - *Blaze DFM Inc., Sunnyvale, CA*
Andrew B. Kahng - *Blaze DFM Inc. & Univ. of California at San Diego, La Jolla, CA*
Youngmin Kim, Dennis M. Sylvester - *Univ. of Michigan, Ann Arbor, MI*

23.4s RADAR: RET-Aware Detailed Routing Using Fast Lithography Simulations

Joydeep Mitra, Peng Yu, David Z. Pan - *Univ. of Texas, Austin, TX*

Session 24

Rm: **209AB**

METHODS AND REPRESENTATIONS FOR LOGIC SYNTHESIS

Chair: Iris Bahar - *Brown Univ., Providence, RI*
Organizers: James Hoe, Marek Perkowski

This session presents three papers addressing classical logic synthesis issues. The first paper introduces a new representation for multiple-output, incompletely specified functions. The representation, called binary-decision diagrams for characteristic functions (BDD_for_CF), is applied to efficiently decompose a function to lookup-table cascades. The second paper proposes an efficient and compact canonical form for Boolean matching under permutation and complementation of variables. The third paper investigates the design space of branch-and-bound algorithms. The paper results in two efficient algorithms for unate and binate covering and applies them to find exact solutions to three previously unsolved ESPRESSO benchmarks.

24.1 BDD Representation for Incompletely Specified Multiple-Output Logic Functions and Its Applications to Functional Decomposition

Tsutomu Sasao, Munehiro Matsuura - *Kyushu Institute of Tech., Iizuka, Japan*

ß 24.2 A New Canonical Form for Fast Boolean Matching in Logic Synthesis and Verification

Afshin Abdollahi, Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

24.3 Effective Bounding Techniques For Solving Unate and Binate Covering Problems

Xiao Yu Li, Matthias F. Stallmann, Franc Brglez - *North Carolina State Univ., Raleigh, NC*

Session 25

Rm: **208AB**

GENERATING EFFICIENT MODELS FOR ANALOG CIRCUITS

Chair: Richard Shi - *Univ. of Washington, Seattle, WA*
Organizers: Koen Lampaert, Sandeep Shukla

This session describes various techniques for generating efficient models for analog circuits. The first paper uses a novel operator-based model-order reduction algorithm to reduce a large linear periodically time-varying system into a smaller one. The second paper analyzes input and clock jitter effects in track and hold circuits. The last paper presents a scalable trajectory-based modeling methodology for generating on-demand macromodels for analog circuits.

25.1 Operator-based Model-Order Reduction of Linear Periodically Time-Varying Systems

Yayun Wan, Jaijeet Roychowdhury - *Univ. of Minnesota, Minneapolis, MN*

ß 25.2 Simulation of the Effects of Timing Jitter in Track-and-Hold and Sample-and-Hold Circuits

Vinita Vasudevan - *Indian Institute of Tech., Madras, Chennai, India*

ß 25.3 Scalable Trajectory Methods for On-Demand Analog Macromodel Extraction

Saurabh K. Tiwary, Rob A. Rutenbar - *Carnegie Mellon Univ., Pittsburgh, PA*

Wednesday June 15

2:00 to 4:00

All speakers are indicated in bold

S - indicates short paper

ß - indicates best paper candidate

session areas indicated on page 14

Session 26

Rm: **207ABC**

SPECIAL SESSION: EMERGING DIRECTIONS IN WIRELESS

Chair: Anantha Chandrakasan - *Massachusetts Institute of Technology, Cambridge, MA*
Organizers: Anantha Chandrakasan, Jan Rabaey

This session features prominent speakers who will identify major new trends and technologies in wireless, as well as the impacts these will have on implementation strategies, architectures, and methodologies.

26.1 Cognitive Radio Techniques for Wide Area Networks
Bill Krenik - *Texas Instruments Inc., Dallas, TX*

26.2 MIMO Technology for Advanced Wireless Local Area Networks
Jeffery M. Gilbert - *Atheros Communications, Inc., Sunnyvale, CA*

26.3 Challenges of Ultra Low Power Wireless System Design
Ahmad Bahai - *National Semiconductor Corp., Santa Clara, CA*

26.4 RF-MEMS in Wireless Architectures
Clark T.-C. Nguyen - *DARPA, Arlington, VA*

Session 27

Rm: **210CD**

CAD FOR FPGAs

Chair: Steve Trimberger - *Xilinx, San Jose, CA*
Organizers: Patrick Lysaght, Steven Teig, Steve Trimberger

FPGAs are rapidly rising in importance and pose a unique set of CAD challenges. This session presents a diverse collection of new techniques from both academic and industrial researchers.

27.1 Multiplexer Restructuring for FPGA Implementation Cost Reduction
Paul Metzgen, Dominic Nancekievill - *Altera Corp., San Jose, CA*

ß 27.2 FPGA Technology Mapping: A Study of Optimality
Andrew C. Ling - *Univ. of Toronto, Toronto, Canada*
Deshanand P. Singh, Stephen D. Brown - *Altera Corp., Toronto, Canada*

27.3 Incremental Retiming for FPGA Physical Synthesis
Deshanand P. Singh, Valavan Manohararajah, Stephen D. Brown - *Altera Corp., Toronto, Canada*

27.4 Architecture-Adaptive Range Limit Windowing for Simulated Annealing FPGA Placement
Ken Eguro, Akshay Sharma, Scott Hauck - *Univ. of Washington, Seattle, WA*

Session 28

Rm: **210AB**

EFFECTIVE FORMAL VERIFICATION USING WORD-LEVEL REASONING, BIT-LEVEL GENERALITY, AND PARALLELISM

Chair: Howard Wong-Toi - *Jasper Design Automation, Inc., Mountain View, CA*

Organizers: Adnan Aziz, Pei-Hsin Ho

The papers in this session address the challenges of formally verifying real-world designs. The first two papers exploit designer intent inferred from the RT-level description. The third paper uses bit-level arithmetic to reduce the complexity of SAT-based BMC. The fourth paper presents a new low-cost approach to sequential redundancy removal. The final paper leverages parallelism to speed-up BDD-based reachability analysis.

ß 28.1 Word Level Predicate Abstraction and Refinement for Verifying RTL Verilog

Himanshu Jain - *Carnegie Mellon Univ., Pittsburgh, PA*
Daniel Kroening - *ETH Zurich, Zuerich, Switzerland*
Natasha Sharygina, Edmund M. Clarke - *Carnegie Mellon Univ., Pittsburgh, PA*

28.2 Structural Search for RTL with Predicate Learning

Ganapathy Parthasarathy, Madhu K Iyer, Kwang-Ting Cheng, Forrest Brewer - *Univ. of California, Santa Barbara, CA*

28.3 Normalization at the Arithmetic Bit Level

Markus Wedler, Dominik Stoffel, Wolfgang Kunz - *Univ. of Kaiserslautern, Kaiserslautern, Germany*

28.4s Exploiting Suspected Redundancy Without Proving It

Hari Mony, Jason R. Baumgartner, Viresh Paruthi - *IBM Corp., Austin, TX*
Robert L. Kanzelman - *IBM Corp., Rochester, NY*

28.5s Multi-threaded Reachability

Debashis Sahoo - *Stanford Univ., Stanford, CA*
Jawahar Jain - *Fujitsu Labs. Ltd., Sunnyvale, CA*
Subramanian K. Iyer - *Univ. of Texas, Austin, TX*
David L. Dill - *Stanford Univ., Stanford, CA*
Allen E. Emerson - *Univ. of Texas, Austin, TX*

Session 29

Rm: **209AB**

ADVANCES IN SYNTHESIS

Chair: David S. Kung - *IBM Corp., Yorktown Heights, NY*

Organizers: Leon Stok, Soha Hassoun

Reusable DFT IP modules can be created using a parameterized soft core generator. Integrated race condition and clock skew scheduling is performed using an efficient method. Leakage power and noise are increasingly important issues that must be addressed by logic synthesis. A unifying framework for modeling asynchronous pipelines allows systematic exploration of the design space.

29.1s Automatic Generation of Customized Discrete Fourier Transform IPs

Grace Nordin, Peter Milder, **James C. Hoe**, Markus Pueschel - *Carnegie Mellon Univ., Pittsburgh, PA*

29.2s Race-Condition-Aware Clock Skew Scheduling

Shih-Hsu Huang, Yow-Tyng Nieh, Feng-Pin Lu - *Chung Yuan Christian Univ., Chung Li, Taiwan*

29.3 Dynamic Supply Gating for Switching and Active Leakage Power Reduction

Swarup Bhunia, Nilanjan Banerjee, Qikai Chen, Hamid Mahmoodi, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

29.4 Designing Logic Circuits for Probabilistic Computation in the Presence of Noise

Kundan Nepal, Iris Bahar, Joseph Mundy, William R. Patterson, Alexander Zaslavsky - *Brown Univ., Providence, RI*

29.5 A Lattice-Based Framework for the Classification and Design of Asynchronous Pipelines

Peggy B. McGee, Steven M. Nowick - *Columbia Univ., New York, NY*

Session 30

Rm: **208AB**

COPING WITH BUFFERING

Chair: Dinesh Gaitonde - *Synopsys, Inc., Mountain View, CA*

Organizers: Dirk Stroobandt, Igor Markov

This session introduces novel methods for economical buffer insertion. The first paper presents dual-Vdd buffer tree construction for power minimization under delay constraints. The next two papers focus on minimizing the overall number of repeaters in a circuit. The fourth paper resolves overlaps between repeaters and pre-existing cells.

30.1 Power Optimal Dual-Vdd Buffered Tree Considering Buffer Stations and Blockages

King Ho Tam, Lei He - *Univ. of California, Los Angeles, CA*

30.2 Net Weighting to Reduce Repeater Counts During Placement

Brent Goplen - *Univ. of Minnesota, Minneapolis, MN*
Prashant Saxena - *Synopsys, Inc., Hillsboro, OR*
Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

30.3 Path Based Buffer Insertion

Cliff C.N. Sze - *Texas A&M Univ., College Station, TX*
Charles J. Alpert - *IBM Corp., Austin, TX*
Jiang Hu, Weiping Shi - *Texas A&M Univ., College Station, TX*

30.4 Diffusion-Based Placement Migration

Haoxing Ren, David Z. Pan - *Univ. of Texas, Austin, TX*
Charles J. Alpert, Paul Villarrubia - *IBM Corp., Austin, TX*

Wednesday June 15

4:30 to 6:30

All speakers are indicated in bold

S - indicates short paper

ß - indicates best paper candidate

session areas indicated on page 14

Session 31

Rm: **207ABC**

PANEL: IS METHODOLOGY THE HIGHWAY OUT OF VERIFICATION HELL?

Chair: Gabe Moretti - *Consultant, Venice, FL*
Organizer: Francine Bacchini

Few would disagree that verification takes the lion's share of today's project resources. Given verification's tremendous burden and its painful impact on fundamental design quality and time-to-market demands, what is our industry doing in response? This panel explores where the methodology highway is taking us—is the destination heaven or just another level of Dante's inferno?

Panelists: **Harry Foster** - *Jasper Design Automation, Mountain View, CA*
Janick Bergeron - *Synopsys, Inc., Ottawa, ON, Canada*
Masayuki Nakamura - *Sony Corp., Tokyo, Japan*
Shrenik Mehta - *Sun Microsystems, Sunnyvale, CA*
Laurent Ducousso - *STMicroelectronics, Grenoble Cedex, France*

Session 32

Rm: **210CD**

IMPACT OF PROCESS VARIATIONS ON POWER

Chair: Sunil Khatri - *Texas A&M Univ., College Station, TX*
Organizers: Naehyuck Chang, Chaitali Chakrabarti

In this session, there are four papers that examine the impact of process variations on power. The first paper computes the full chip leakage power under process variations considering intra-die, inter-die variations and spatial correlations. The second paper examines a design of a low-power parallel system based on voltage scaling considering within-die variations and temperature fluctuations. The correlation between delay and power is the subject of the third paper. Finally, the fourth paper presents a convex optimization procedure to find the exact minimum leakage considering process variations.

32.1 Full-Chip Analysis of Leakage Power Under Process Variations, Including Spatial Correlations

Hongliang Chang, Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

32.2 Variations-Aware Low-Power Design with Voltage Scaling

Navid Azizi - *Univ. of Toronto, Toronto, Canada*
Muhammad M. Khellah, Vivek De - *Intel Corp., Hillsboro, OR*
Farid N. Najm - *Univ. of Toronto, Toronto, Canada*

32.3 Accurate and Efficient Parametric Yield Estimation Considering Correlated Variations in Leakage Power and Performance

Ashish Srivastava, Saumil S. Shah, Kanak B. Agarwal, Dennis M. Sylvester, David Blaauw, Stephen Director - *Univ. of Michigan, Ann Arbor, MI*

32.4 Leakage Minimization of Nano-Scale Circuits in the Presence of Systematic and Random Variations

Sarvesh Bhardwaj, Sarma B. Vrudhula - *Arizona State Univ., Tempe, AZ*

Session 33

Rm: **210AB**

SPECIAL SESSION: THE BEST OF WIRELESS AT ISSCC

Chair: Wanda Gass - *Texas Instruments, Inc., Dallas, TX*

Organizer: Wanda Gass

This is the now-traditional Best of ISSCC session at DAC. This year, we selected the best of wireless-related papers at ISSCC to fit into the theme of Wireless Day.

33.1 A 135Mb/s DVB-S2 Compliant CODEC Based on 64,800b LDPC and BCH Codes (ISSCC Paper 24.3)

Pascal Urard, E. Yeo, L. Paumier, P. Georgelin, T. Michel, V. Lebars, E. Lantreibecq - *STMicroelectronics, Crolles, France*
B. Gupta - *W5Networks, Inc., Palo Alto, CA*

33.2 A 180Ms/s 162Mb/s Wideband Three-Channel Baseband and MAC Processor for 802.11a/b/g (ISSCC Paper 24.7)

Manish Bhardwaj, C. Briggs - *Engim, Inc., Acton, MA*
A. Chandrakasan - *Massachusetts Institute of Tech., Cambridge, MA*
C. Eldridge, J. Goodman, T. Nightingale, S. Sharma, G. Shin, D. Shoemaker, A. Sinha , R. Venkatesan, J. Winston, W. Zhou - *Engim, Inc., Acton, MA*

33.3 90 nm Low Leakage SoC Design Techniques for Wireless Applications

Philippe Royannez, V. Peiris, C. Arm, S. Bories, S. Cserveny, F. Giroud, P. Graber, S. Gyger, E. Le Roux, T. Melly - *Texas Instruments, Inc., Villeneuve Loubet, France*

33.4 A 24GHz Phased-Array Transmitter in 0.18µm CMOS (ISSCC 11.7)

Ali Hajimiri, Arun Natarajan, Abbas Komijani - *California Institute of Tech., Pasadena, CA*

Session 34

Rm: **209AB**

ARCHITECTURAL SUPPORT FOR COMMUNICATION

Chair: Petru Eles - *Linköping Univ., Linköping, Sweden*

Organizers: Marcello Coppola, Peter Marwedel

Communication is quickly becoming one of the most important problems in high-performance and system-on-chip designs. The first two papers present hardware to reduce snooping in MPSoC and adaptivity support. The third paper is on floorplan aware synthesis of communication architectures. Finally, the last two propose architectures for dynamic topology and traffic shaping.

34.1 Cache Coherence Support for Non-shared Bus Architecture on Heterogeneous MPSoCs

Taeweon Suh, Hsien-Hsin S. Lee - *Georgia Institute of Tech., Atlanta, GA*
Daehyun Kim - *Intel Corp., Santa Clara, CA*

34.2 A Low-Latency Router Supporting Adaptivity for On-Chip Interconnects

Jongman Kim, Dongkook Park, Theocharis G. Theocharides, **N. Vijaykrishnan**, Chita R. Das - *Pennsylvania State Univ., University Park, PA*

ß 34.3 Floorplan-aware Automated Synthesis of Bus-based Communication Architectures

Sudeep Pasricha, Nikil Dutt, Elaheh Bozorgzadeh - *Univ. of California, Irvine, CA*
Mohamed Ben-Romdhane - *Conexant Systems Inc., Newport Beach, CA*

34.4s FLEXBUS: A High-Performance System-on-Chip Communication Architecture with a Dynamically Configurable Topology

Krishna Sekar - *Univ. of California at San Diego, La Jolla, CA*
Kanishka Lahiri, Anand Raghunathan - *NEC-Labs America, Inc., Princeton, NJ*
Sujit Dey - *Univ. of California at San Diego, La Jolla, CA*

34.5s Traffic Shaping for an FPGA based SDRAM Controller with Complex QoS Requirements

Sven Heithecker, Rolf Ernst - *Technical Univ. of Braunschweig, Braunschweig, Germany*

Session 35

Rm: **208AB**

NEW APPROACHES TO PHYSICAL DESIGN PROBLEMS

Chair: Chung-Kuan Cheng - *Univ. of California at San Diego, La Jolla, CA*

Organizers: Louis Scheffer, Malgorzata Marek-Sadowska

Traditional physical design problems are attacked by new methods and algorithms. This includes a floorplanner that considers micro-architecture, two new core placement algorithms, and an implementation of the recent X routing ideas.

35.1 Microarchitecture-Aware Floorplanning Using a Statistical Design of Experiments Approach

Vidyasagar Nookala, Ying Chen, David Lilja, Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

35.2 Timing-Driven Placement by Grid-Warping

Zhong Xiu, Rob A. Rutenbar - *Carnegie Mellon Univ., Pittsburgh, PA*

35.3 Faster and Better Global Placement by a New Transportation Algorithm

Ulrich Brenner, Markus Struzyna - *Universität Bonn, Bonn, Germany*

ß 35.4 Multilevel Full-Chip Routing for the X-Based Architecture

Tsung-Yi Ho, Chen-Feng Chang, Yao-Wen Chang, Sao-Jie Chen - *National Taiwan Univ., Taipei, Taiwan*

Thursday June 16

8:30 to 10:00

All speakers are indicated in bold

S - indicates short paper

ß - indicates best paper candidate

session areas indicated on page 14

Session 36

Rm: **207ABC**

SPECIAL SESSION: MATLAB® - THE OTHER EMERGING SYSTEM-DESIGN LANGUAGE

Chair: Randy Allen - *Catalytic, Inc., Palo Alto, CA*
Organizer: Steven Tjiang

This special session addresses the requirements to make MATLAB® suitable for real implementation. It will demonstrate design and verification flows starting with MATLAB® for DSPs, FPGAs and ASICs.

36.1 MATLAB® as a Design Environment for Wireless ASIC Design

Erik Lindskog - *Beceem Communications, Inc., Santa Clara, CA*

36.2 MATLAB® Extensions for the Development, Testing, and Verification of Real-Time DSP Program Development

David P. Magee - *Texas Instruments, Inc., Dallas, TX*

36.3 MATLAB® as a Development Environment for FPGA Design

Tejas Bhatt, Dennis McCain - *Nokia Americas, Irving, TX*

Session 37

Rm: **210CD**

PANEL: SHOULD OUR POWER APPROACH BE CURRENT?

Chair: Tim Fox - *Deutsche Bank, Baltimore, MD*
Organizers: Lou Covey, Susan Lippincott Mack

The metric for success has changed from performance and area to power consumption in nanometer SoC designs, especially in the huge market for handheld/wireless consumer electronics. Although "power" is often the stated concern, current is the real issue. Leaders from across the silicon design chain discuss how they cope with leakage current today and their vision to address the problem in order for the electronics industry to successfully move below 90 nm.

Panelists: David Heacock - *TexasInstruments, Inc., Dallas, TX*
Vess Johnson - *Nascentric, Inc., Austin, TX*
Andrew Yang - *Apache Design Solutions, Inc., Mountian View, CA*
Ed Huijbregts - *Magma Design Automation, Inc., Eindhoven, Netherlands*
Paul Zuchowski - *IBM Corp., Essex Junction, NJ*
Avner Kornfeld - *Intel Corp., Hillsboro, OR*

Session 38

Rm: **210AB**

EMERGING IDEAS IN ENERGY MANAGEMENT TECHNIQUES

Chair: Rajesh Gupta - *Univ. of California at San Diego, San Diego, CA*

Organizers: Diana Marculescu, Taewhan Kim

This collection of papers explores some of the new ideas for energy management in a wide variety of scenarios.

38.1 DTM: Dynamic Tone Mapping for Backlight Scaling

Ali Iranli, Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

38.2 Application/Architecture Power Co-Optimization for Embedded Systems Powered by Renewable Sources

Dexin Li, Pai H. Chou - *Univ. of California, Irvine, CA*

38.3s User-Perceived Latency Driven Voltage Scaling for Interactive Applications

Le Yan, Lin Zhong, Niraj K. Jha - *Princeton Univ., Princeton, NJ*

38.4s System-Level Energy-Efficient Dynamic Task Scheduling

Jianli Zhuo, **Chaitali Chakrabarti** - *Arizona State Univ., Tempe, AZ*

Session 39

Rm: **209AB**

ADVANCES IN OPTIMIZATION OF MIXED-SIGNAL CIRCUITS

Chair: Koen Lampaert - *Mindspeed Technologies, Inc., Newport Beach, CA*

Organizers: Geert Van Der Plas, Sandeep Shukla

This session reports recent advances in optimization of mixed-signal circuits. The session starts with a paper on optimization with ellipsoidal uncertainty for robust analog circuit design. In the second paper, a unified framework for the optimization of FIR equalization filters is presented. In the third paper, template-driven layout optimization with inclusion of parasitics is presented. In the last paper, an approach for inductor synthesis is presented that includes global and local optimization.

39.1 OPERA: OPtimization with Ellipsoidal Uncertainty for Robust Analog IC design

Yang Xu - *Carnegie Mellon Univ., Pittsburgh, PA*
Kan-Lin Hsiung - *Stanford Univ., Stanford, CA*
Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*
Ivan Nausieda - *Harvard Univ., Cambridge, MA*
Stephen Boyd - *Stanford Univ., Stanford, CA*
Larry T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

39.2 A Unified Optimization Framework for Equalization Filter Synthesis

Jihong Ren, Mark R. Greenstreet - *Univ. of British Columbia, Vancouver, BC, Canada*

39.3s Parasitic-Aware Template-Driven Optimization of Analog Integrated Circuit Layouts

Sambuddha Bhattacharya, Nuttorn Jangkrajarng, J. Richard Shi - *Univ. of Washington, Seattle, WA*

39.4s Multi-Level Approach for Integrated Spiral Inductor Optimization

Arthur Nieuwoudt, Yehia Massoud - *Rice Univ., Houston, TX*

Session 40

Rm: **208AB**

CIRCUIT PERFORMANCE UNDER PARAMETER VARIATION

Chair: L. Miguel Silveira - *INESC-ID/IST/Cadence Labs, Lisbon, Portugal*

Organizers: Charlie Chung-Ping Chen, Joel Phillips

This session contains a variety of contributions motivated by circuit analysis under process variation. The first paper argues that in practical applications, adequate statistical analysis of timing can be performed with relatively simple path-based methods. The second paper surveys variability modeling for circuit applications. The final paper discusses sensitivity analysis in the context of power grid modeling.

40.1 Statistical Static Timing Analysis: How Simple Can We Get?

Chirayu S. Amin - *Northwestern Univ., Evanston, IL*
Noel Menezes, Kip Killpack, Florentin Dartu - *Intel Corp., Hillsboro, OR*
Yehea Ismail - *Northwestern Univ., Evanston, IL*
Umakanta Choudhury, Nagib Hakim - *Intel Corp., Hillsboro, OR*

40.2 Mapping Statistical Process Variations Toward Circuit Performance Variability: An Analytical Modeling Approach

Yu Cao, Lawrence T. Clark - *Arizona State Univ., Tempe, AZ*

40.3 Power Grid Simulation Via Efficient Sampling-Based Sensitivity Analysis and Hierarchical Symbolic Relaxation

Peng Li - *Texas A&M Univ., College Station, TX*

Thursday June 16

10:30 to 12:00

All speakers are indicated in bold

S - indicates short paper

ß - indicates best paper candidate

session areas indicated on page 14

Session 41

Rm: **207ABC**

SPECIAL SESSION: FORMALLY VERIFYING YOUR 10-MILLION GATE DESIGN

Chair: Robert Damiano - *Synopsys, Inc., Hillsboro, OR*
Organizer: Pei-Hsin Ho

In this special session verification practitioners from IBM, NVIDIA and STMicroelectronics share their best known methods and success stories of employing formal property verification to achieve better design quality and shorter design cycle.

41.1 Formal Verification: Is It Real Enough?
Yaron Wolfsthal - *IBM Corp., Haifa, Israel*
Rebecca M. Gott - *IBM Corp., Poughkeepsie, NY*

41.2 Can We Really Do Without the Support of Formal Methods in the Verification of Large Designs?
Umberto Rossi - *STMicroelectronics, Milano, Italy*

41.3 Streamline Verification Process with Formal Property Verification to Meet Highly Compressed Design Cycle
Prosenjit Chattterjee - *NVIDIA Corp., Santa Clara, CA*

Session 42

Rm: **210CD**

EMBEDDED HARDWARE AND SYSTEM SOFTWARE

Chair: Eugenio Villar - *Universidad de Cantabria, Santander, Spain*
Organizers: Chi-Ying Tsui, Pai Chou

This session includes four papers describing embedded system hardware and software closely linked to that hardware. The first paper proposes an architecture which is relevant for fast internet routing. It is followed by a paper presenting an approach for speech recognition that takes the limited performance of portable devices into account. The third paper comprises algorithms for low-overhead fault-tolerant execution of Java programs. The final paper addresses multiprocessor embedded systems which often have processor-local caches and a shared memory. If the system's code is available at design time, we can maximize cache hits by rearranging code in memory.

42.1 TCAM Enabled On-Chip Logic Minimization
Seraj Ahmad, **Rabi Mahapatra** - *Texas A&M Univ., College Station, TX*

42.2 Hardware Speech Recognition for User Interfaces in Low Cost, Low Power Devices
Sergiu Nedevschi, Rabin K. Patra, Eric A. Brewer - *Univ. of California, Berkeley, CA*

42.3 Improving Java Virtual Machine Reliability for Memory-Constrained Embedded Systems
Guangyu Chen, Mahmut Kandemir - *Pennsylvania State Univ., University Park, PA*

42.4s Frequency-Based Code Placement for Embedded Multiprocessors
Corey M. Goldfeder - *Columbia Univ., New York, NY*

Session 43

Rm: **210AB**

POWER ESTIMATION AND DESIGN TRADEOFFS

Chair: Kimiyoshi Usami - *Shibaura Institute of Technology, Saitama, Japan*
Organizers: Jerry Frenkil, Amitava Majumdar

This session contains papers that address low power design at several levels. The first paper describes a novel and fast power estimation using hardware emulation. The second paper explores tradeoffs in power and performance in configurable processors. Power control in a network processor using clock gating is decribed in the third paper. The fourth paper presents a technique that overcomes delay variation by bulk voltage control.

43.1 Power Emulation: A New Paradigm for Power Estimation

Joel D. Coburn, Srivaths Ravi, Anand Raghunathan - *NEC-Labs America, Princeton, NJ*

43.2 Implementing Low-Power Configurable Processors - Practical Options and Tradeoffs

Ashish Dixit, John H. Wei, Chris Rowen - *Tensilica, Inc., Santa Clara, CA*

43.3s Low Power Network Processor Design Using Clock Gating

Yan Luo, Jia Yu, Jun Yang, Laxmi Bhuyan - *Univ. of California, Riverside, CA*

43.4s A Variation-Tolerant Sub-Threshold Design Approach

Nikhil Jayakumar, Sunil Khatri - *Texas A&M Univ., College Station, TX*

Session 44

Rm: **209AB**

PROGRAMMABLE ARCHITECTURES

Chair: Pedro Diniz - *USC Information Sciences Institute, Marina Del Rey, CA*
Organizers: Ryan Kastner, Steven Teig

The exploration of programmable architectures, particularly for low power, is an active area of contemporary research. This session addresses three distinct topics: power management, dynamic reconfiguration, and IP mapping.

44.1 Leakage Efficient Chip-Level Dual-Vdd Assignment with Time Slack Allocation for FPGA Power Reduction

Yan Lin, Lei He - *Univ. of California, Los Angeles, CA*

44.2 Logic Block Clustering of Large Designs for Channel Width Constrained FPGAs

Marvin Tom, Guy Lemieux - *Univ. of British Columbia, Vancouver, BC, Canada*

44.3 Dynamic Reconfiguration with Binary Translation: Breaking the ILP barrier with Software Compatibility

Antonio Carlos S. Beck, **Luigi Carro** - *UFRGS, Porto Alegre, Brazil*

Session 45

Rm: **208AB**

SAT: COOL ALGORITHMS AND HOT APPLICATIONS

Chair: Carl Pixley - *Synopsys, Inc., Hillsboro, OR*
Organizers: Harry Foster, Rajeev Ranjan

Recent advances in SAT have taken formal verification capabilities to a new level. The first paper shows a novel method for extending SAT techniques for liveness properties. The next two papers describe advanced learning techniques. The last paper improves the performance of abstraction refinement for property checking.

45.1 Beyond Safety: Customized SAT-based Model Checking

Malay Ganai, Aarti Gupta - *NEC-Labs America, Inc., Princeton, NJ*
Pranav Ashar - *Real Intent, Inc., Santa Clara, CA*

45.2 Efficient SAT Solving: Beyond Supercubes

Domagoj Babic, Jesse D. Bingham, **Alan J. Hu**- *Univ. of British Columbia, Vancouver, BC, Canada*

45.3s Prime Clauses for Fast Enumeration of Satisfying Assignments to Boolean Circuits

Hoonsang Jin, Fabio Somenzi - *Univ. of Colorado, Boulder, CO*

45.4s Dynamic Abstraction Using SAT-based BMC

Liang Zhang - *Cadence Design Systems, Inc., San Jose, CA*
Mukul R. Prasad - *Fujitsu Labs Ltd., Sunnyvale, CA*
Michael S. Hsiao - *Virginia Polytechnic Inst., Blacksburg, VA*, Thomas Sidle - *Fujitsu Labs Ltd., Sunnyvale, CA*

Thursday June 16

2:00 to 4:00

All speakers are indicated in bold

S - indicates short paper

ß - indicates best paper candidate

session areas indicated on page 14

Session 46

Rm: **207ABC**

SPECIAL SESSION: DFM AND VARIABILITY: THEORY AND PRACTICE

Chair: Chandu Visweswariah - *IBM Corp., Yorktown Heights, NY*
Organizers: Michael Orshansky, Tanay Karnik

This session will present a series of short (15-minute) talks that consider multiple facets of the design for manufacturability paradigm. The topics include (1) measuring interconnect variability and its effect on parasitic extraction, (2) challenges of implementing a library-based DFM strategy and the interaction between foundry and designer, (3) new circuit design techniques for robust operation, (4) the need for statistical timing analysis, (5) CAD solution for variation-aware timing analysis and optimization, and finally (6) the economic justification of implementing a DFM flow. The talks will be followed by a 30-minute Q&A with a panel of authors. On the theory side, the key focus is circuit and CAD solutions to deal with variability, and updated assessments of the impact of BEOL variations. Commercial EDA is incrementally extending existing platforms. On the practice side, the focus is on economic justification of DFM, as well as the interaction between foundry and designer.

46.1s BEOL Variabiity and Impact on RC Extraction
Nagaraj NS - *Texas Instruments, Inc., Dallas, TX*

46.2s An Effective DFM Strategy Requires Accurate Process and IP Pre-Characterization
Carlo Guardiani, Massimo Bertoletti, Christoph Dolainsky, Nicola Dragone, Marco Malcotti, Patrick McNamara - *PDF Solutions, Inc., San Jose, CA*

46.3s Variation-Tolerant Circuits: Circuit Solutions and Techniques
Vivek De - *Intel Corp., Hillsboro, OR*

46.4s On the Need for Statistical Timing Analysis
Farid N. Najm - *Univ. of Toronto, Toronto, Canada*

46.5s CAD Tools for Variation Tolerance
David Blaauw, Kaviraj S. Chopra - *Univ. of Michigan, Ann Arbor, MI*

46.6s Are There Economic Benefits in DFM?
Matt Nowak, **Riko Radojcic** - *QUALCOMM Incorporated, San Diego, CA*

Session 47

Rm: **210CD**

TOOLS AND METHODS FOR THE VERIFICATION OF PROCESSORS AND PROCESSOR-BASED SYSTEMS

Chair: Raghuram Tupuri - *AMD, Austin, TX*
Organizers: Avi Ziv, Erich Marschner

Modern systems are increasingly becoming microprocessor-based. Functional verification of microprocessors has long been recognized as the toughest challenge in verification. The papers in this session stress the need for proper verification planning, highlight the need for test plan automation, and illustrate the use of sophisticated test generation techniques to thoroughly cover corner cases. Case studies highlight the application of a combination of verification techniques to successfully verify these complex systems.

47.1 A Generic Micro-Architectural Test Plan Approach for Microprocessor Verification
Allon Adir, Hezi Azatchi, **Eyal Bin**, Ofer Peled, Kirill Shoikhet - *IBM Corp., Haifa, Israel*

47.2s IODINE: A Tool to Automatically Infer Dynamic Invariants for Hardware Designs
Sudheendra Hangal, Naveen Chandra - *Sun Microsystems, Bangalore, India*
Sridhar Narayanan - *P.A. Semi Inc., Santa Clara, CA*, Sandeep Chakravorty - *Sun Microsystems, Bangalore, India*

47.3s VLIW ? A Case Study of Parallelism Verification
Allon Adir, Yaron Arbetman - *IBM Corp., Haifa, Israel*
Massimo A Calligaro, Andrew Cofler - *STMicroelectronics, Grenoble Cedex, France*
Bella Dubrov - *IBM Corp., Haifa, Israel*
Gabriel Duffy - *STMicroelectronics, Grenoble Cedex, France*
Yossi Lichtenstein, **Michal Rimon**, Michael Vinov - *IBM Corp., Haifa, Israel*

47.4 StressTest: An Automatic Approach to Test Generation via Activity Monitors
Ilya Wagner, Valeria Bertacco, Todd Austin - *Univ. of Michigan, Ann Arbor, MI*

47.5 Smart Diagnostics for Configurable Processor Verification
Sadik Ezer, Scott Johnson - *Tensilica, Inc., Santa Clara, CA*

Session 48

Rm: **210AB**

ELECTRICAL OPTIMIZATION FOR PHYSICAL SYNTHESIS

Chair: Gi-Joon Nam - *IBM Corp., Austin, TX*
Organizers: Patrick Groeneveld, Phiroze Parakh

This session deals with novel power and delay optimization techniques in placement. The first paper presents a method that that reduces power by clustering registers. The following paper performs placement using a new differential timing analysis model. The final two papers both attack the optimization through novel analytical methods.

48.1 Power Aware Placement

Yongseok Cheon, Pei-Hsin Ho - *Synopsys, Inc., Portland, OR*
Andrew B. Kahng, Sherief Reda, **Qinke Wang**, - *Univ. of California at San Diego, La Jolla, CA*

48.2 How Accurately Can We Model Timing in A Placement Engine?

Amit Chowdhary, Karthik Rajagopal, Satish Venkatesan, Tung Cao, Vladimir Tiourin - *Intel Corp., Santa Clara, CA*
Yegna Parasuram - *Sierra Design Automation, Inc., Santa Clara, CA*
Bill Halpin - *Synplicity, Inc., Sunnyvale, CA*

48.3 Efficient and Accurate Gate Sizing with Piecewise Convex Delay Models

Hiran K. Tennakoon, Carl Sechen - *Univ. of Washington, Seattle, WA*

48.4 Freeze: Engineering a Fast Repeater Insertion Solver for Power Minimization Using the Ellipsoid Method

Yuantao Peng, **Xun Liu** - *North Carolina State Univ., Raleigh, NC*

Session 49

Rm: **209AB**

OPTIMIZATION TECHNIQUES IN HIGH-LEVEL SYNTHESIS

Chair: Matt Moe - *Forte Design Systems, Pittsburgh, PA*
Organizers: John Sanguinetti, Stephen Edwards

High Level Synthesis is fundamentally about optimizing the resulting design. The papers in this session cover a variety of optimization techniques from minimizing the bit width of data values to creating fault-tolerant biochips. Papers include a technique to minimize buffer requirements and a technique to efficiently analyze pointers in C source code.

49.1 Minimising Buffer Requirements of Synchronous Dataflow Graphs with Model-Checking

Marc Geilen, Twan Basten, **Sander Stuijk**- *Eindhoven Univ. of Technology, Eindhoven, Netherlands*

49.2 Unified High-Level Synthesis and Module Placement for Defect-Tolerant Microfluidic Biochips

Fei Su, Krishnendu Chakrabarty - *Duke Univ., Durham, NC*

49.3 Towards Scalable Flow and Context Sensitive Pointer Analysis

Jianwen Zhu - *Univ. of Toronto, Toronto, ON, Canada*

49.4s MiniBit: Bit-Width Optimization via Affine Arithmetic

Dong-U Lee, Altaf Abdul Gaffar, Oskar Mencer, Wayne Luk - *Imperial College, London, UK*

49.5s A Non-Parametric Approach for Dynamic Range Estimation of Nonlinear Systems

Bin Wu, Jianwen Zhu, Farid N. Najm - *Univ. of Toronto, Toronto, Canada*

Session 50

Rm: **208AB**

TESTING FOR PROCESS- AND TIMING-RELATED FAULTS

Chair: Nicola Nicolici - *McMaster University, Hamilton, Canada*
Organizers: Gordon Roberts, Kazumi Hatayama

This session considers the impact of process variations and defects on various test algorithms and techniques, such as path delay test compaction, digital-to-analog converter type tests, memory tests and transient fault type tests.

50.1 Path Delay Test Compaction with Process Variation Tolerance

Seiji Kajihara, Masayasu Fukunaga, **Xiaoqing Wen**- *Kyushu Institute of Tech., Iizuka, Japan*
Toshiyuki Maeda, Shuji Hamada, Yasuo Sato - *STARC, Yokohama, Japan*

50.2 A DFT Approach for Diagnosis and Process Variation-Aware Structural Test of Thermometer Coded Current Steering DACs

Rasit O. Topaloglu, Alex Orailoglu - *Univ. of California at San Diego, La Jolla, CA*

50.3 Resistive-Open Defect Injection in SRAM Core-Cell: Analysis and Comparison between 0.13 µm and 90 nm Technologies

Luigi Dilillo, **Patrick Girard**, Serge Pravossoudovitch, Arnaud Virazel - *LIRMM, Montpellier, France*
Magali Bastian Hage-Hassan - *Infineon Tech., Sophia-Antipolis, France*

50.4 Asynchronous Circuits Transient Faults Sensitivity Evaluation

Yannick Monnet, Marc Renaudin, Regis Leveugle - *TIMA Lab., Grenoble, France*

Thursday June 16

4:30 to 6:00

All speakers are indicated in bold

S - indicates short paper

ß - indicates best paper candidate

session areas indicated on page 14

Session 51

Rm: **207ABC**

SPECIAL SESSION: HIERARCHICAL DESIGN AND DESIGN SPACE EXPLORATION OF ANALOG INTEGRATED CIRCUITS

Chair: Erich Barke - *Univ. of Hannover, Hannover, Germany*
Organizer: Helmut Graeb

This session presents the leading work in analog design space exploration which is an important prerequisite for top-down synthesis flows. The research presented is grounded in real industrial design problems and has practical application.

51.1 Deterministic Approaches to Analog Performance Space Exploration

Daniel Mueller, Guido Stehr, Helmut Graeb, Ulf Schlichtmann - *Tech. Univ. of Munich, Munich, Germany*

51.2 Mixed-Signal Design Space Exploration Through Analog Platforms

Fernando De Bernardinis - *Univ. of California, Berkeley, CA*
Pierluigi Nuzzo - *Univ. of Pisa, Pisa, Italy*
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

51.3 Performance Space Modeling for Hierarchical Synthesis of Analog Integrated Circuits

Georges Gielen, Trent McConaghy, Tom Eeckelaert - *Katholieke Universiteit Leuven, Leuven, Belgium*

Session 52

Rm: **210CD**

PANEL: PLATFORM ASIC APPRENTICES: WHO WILL SURVIVE YOUR BOARDROOM?

Chair: Ron Wilson - *EE Times, San Mateo, CA*
Organizer: Joe Gianelli

Moore's law delivers higher performance and lower cost for FPGAs and ASICs alike, but at the 90 nm process node and below, design schedules using the traditional cell-based ASIC design methodology hit a wall of uncertainty. At 90 nm and below an emerging alternative, or apprentice, ASIC design platform is either PlatformASIC or FPGAs. Which alternativewill survive your board room?

Panelists: Christopher L. Hamlin - *LSI Logic Corp., Milpitas, CA*
Ivo Bolsens - *Xilinx, Inc., San Jose, CA*
Richard Tobias - *Toshiba Corp., San Jose, CA*
Ken McElvain - *Synplicity, Inc., Sunnyvale, CA*
Raul Camposano - *Synopsys, Inc., Mountain View, CA*
Steve Leibson - *Tensilica, Inc., Santa Clara, CA*

Session 53

Rm: **210AB**

DYNAMIC VOLTAGE SCALING

Chair: Kris Flautner - *ARM Ltd., Cambridge, UK*
Organizers: Diana Marculescu, Trevor Mudge

Dynamic Voltage Scaling has become one of the most popular topics for research. This session brings together some of the best recent work in the area.

53.1 Quasi-Static Assignment of Voltages and Optional Cycles for Maximizing Rewards in Real-Time Systems with Energy Constraints

Luis A. Cortes, Petru Eles, Zebo Peng - *Linköping Univ., Linköping, Sweden*

53.2 DC-DC Converter-Aware Power Management for Battery-Operated Embedded Systems

Yongseok Choi, Naehyuck Chang, Taewhan Kim - *Seoul National Univ., Seoul, Republic of Korea*

53.3s Energy Optimal Speed Control of Devices with Discrete Speed Sets

Ravishankar Rao, Sarma Vrudhula - *Arizona State Univ., Tempe, AZ*

53.4s Optimal Procrastinating Voltage Scheduling for Hard Real-Time Systems

Yan Zhang Zhang, **Zhijian Lu**, Mircea R. Stan, John C. Lach, Kevin Skadron - *Univ. of Virginia, Charlottesville, VA*

Session 54

Rm: **209AB**

NEW DIRECTIONS IN FPGA TECHNOLOGIES

Chair: Andre DeHon - *California Institute of Technology, Pasadena, CA*
Organizers: Jens Palsberg, Ryan Kastner

Scaling trends require new ideas to keep up with the relentless pace of Moore's Law. This session presents both new device technologies and innovations for existing fabrics.

54.1 Flexible ASIC: Shared Masking for Multiple Media Processors

Jennifer L. Wong, Farinaz Koushanfar, Miodrag Potkonjak - *Univ. of California, Los Angeles, CA*

54.2 Device and Architecture Co-Optimization for FPGA Power Reduction

Lerong Cheng, Phoebe Wong, Fei Li, Yan Lin, Lei He - *Univ. of California, Los Angeles, CA*

54.3 Exploring Technology Alternatives for Nano-Scale FPGA Interconnects

Aman Gayasen, Vijaykrishnan Narayanan, Mary Jane Irwin - *Pennsylvania State Univ., University Park, PA*

Session 55

Rm: **208AB**

REDUCED-ORDER MODELING

Chair: Janet Wang Roveda - *Univ. of Arizona, Tucson, AZ*
Organizers: Byron Krauter, Vikram Jandhyala

This session overviews the latest developments in reduced order modeling. The first paper presents a fast technique for analyzing the time-domain response of interconnects, using an elegantly simple method based on piecewise linear waveform models. The second paper uses convex optimization techniques for model-order reduction, using an approach similar to rational approximation. Next, a procedure that incorporates the skin effect to build an Arnoldi-based passivity preserving model is presented. The final paper in the session describes a new algorithm for fast reduced order full-wave models.

55.1 Piece-Wise Approximations of RLCK Circuit Responses using Moment Matching

Chirayu S. Amin, Yehea Ismail - *Northwestern Univ., Evanston, IL*
Florentin Dartu - *Intel Corp., Hillsboro, OR*

55.2 A Quasi-Convex Optimization Approach to Parameterized Model-Order Reduction

Kin Cheong Sou, Luca Daniel, Alexandre Megretski - *Massachusetts Institute of Tech., Cambridge, MA*

55.3s Structure Preserving Reduction of Frequency Dependent Interconnect

Quming Zhou, Kartik Mohanram, Athanasios C. Antoulas - *Rice Univ., Houston, TX*

55.4s Segregation by Primary Phase Factors: A Full-Wave Algorithm for Model-Order Reduction

Thomas J. Klemas, Luca Daniel, Jacob K. White - *Massachusetts Institute of Tech., Cambridge, MA*

Tutorials

Tutorial Breakfast • **8:00 am - 9:00 am** • **Monday,** Rm: **210CD** • **Friday,** Rm: **204ABC**
Tutorial Lunch • **12:00 pm - 1:00 pm** • **Monday,** Rm: **210CD** • **Friday,** Rm: **204ABC**

Monday, June 13 • 9:00 am - 5:00 pm

TUTORIAL 1 - STATISTICAL PERFORMANCE ANALYSIS AND OPTIMIZATION OF DIGITAL CIRCUITS

Rm: **210AB**

Organizer: **Ruchir Puri** - *IBM Corp., Yorktown Heights, NY*
Presenters: **Sachin Sapatnaker** - *Univ. of Minnesota, Minneapolis, MN*
Vivek De - *Intel Corp., Portland, OR*
Michael Orshansky - *Univ. of Texas, Austin, TX*
Nagib Hakim - *Intel Corp., Santa Clara, CA*

On-chip variations have become an increasing concern in integrated circuits as circuit sizes continue to increase and feature sizes continue to shrink. As device and interconnect parameters such as physical dimensions show variability, the prediction of circuit performance, both in terms of delay and power, has become a challenging task. Conventional approaches that handle the problem of variability using multiple process corners must be replaced by a statistical paradigm that incorporates the complexities of intra-die variations, inter-die variations, deterministic variations, random variations, correlated variations, etc.

This tutorial will present a comprehensive overview of methods that are required to move to a truly statistically-based performance framework, focusing on designs with high timing and power yield. The presentation is directed towards researchers and practitioners in industry working on cutting-edge nanometer-scale designs. It will consist of several parts that cover issues from fabrication to design to CAD: roughly speaking, the segments will deal with the extraction of fab information into distributions for analysis; circuit structures and techniques to reduce on-chip variability; and CAD for the analysis and optimization of timing and power.

Friday, June 17 • 9:00 am - 5:00 pm

TUTORIAL 2 - C-BASED DESIGN: INDUSTRIAL EXPERIENCE

Rm: **210AB**

Organizer: **Carl Pixley** - *Synopsys, Inc., Hillsboro, OR*
Srimat Chakradhar - *NEC-Labs America, Inc., Princeton, NJ*
Presenters: **Rajesh Gupta** - *Univ. of California at San Diego, La Jolla, CA*
Kazutoshi Wakabayashi - *NEC Corp., Tokyo, Japan*
Ramanathan Sethuraman - *Philips Research Labs, Eindhoven, Netherlands*
Andres Takach - *Mentor Graphics Corp., Wilsonville, OR*

This tutorial will provide an introduction to C-based design, and discuss the design techniques in use in the industry. C-based design reduces overall turn-around time, deals well with design complexity, supports optimization based on various objective functions (e.g., area, power consumption), and improves HW/SW co-design. C-based design also facilitates the creation of re-usable behavioral IP in contrast to RTL design where re-use of traditional RTL IPs has been poor. This tutorial showcases C-based design techniques in use in two companies: Philips, and NEC. The tutorial covers C-based design fundamentals, motivation for C-based design, industry need, and why the timing is right for C-based design. After discussion of C-based design fundamentals, we move on to support technologies (power, verification) that are necessary for realizing the full potential of C-based design. EDA response to a call for C-based design is also covered.

TUTORIAL 3 - CONSTRAINT SATISFACTION TECHNIQUES FOR AUTOMATIC GENERATION OF STIMULI FOR FUNCTIONAL HARDWARE VERIFICATION

Rm: **210CD**

Organizer: **Roy Emek** - *IBM Corp., Haifa, Israel*
Presenters: **Toby Walsh** - *National ICT Australia and UNSW, Sydney, Australia*
Shashidhar Thakur - *Synopsys, Inc., Mountain View, CA*
Mahesh Iyer - *Synopsys, Inc., Mountain View, CA*
Hanli Joseph Zhang - *Cisco Systems, Inc., San Jose, CA*
Yehuda Naveh - *IBM Corp., Haifa, Israel*

The development and usage of constraint satisfaction techniques for the automatic generation of stimuli has increased dramatically in recent years, and is currently at the basis of many functional verification platforms. The theoretical fields of constraint satisfaction and constraint programming are at the front of present-day research. In this tutorial, the speakers will discuss various aspects of constraint-based stimuli generation, including:

- The theoretical fields of Constraint Satisfaction Problems (CSP) and Constraint Programming (CP).
- The rationale behind constraint-based stimuli generation and the methods for doing so in the context of an industrial verification platform.
- A user's viewpoint on the adaptation of constraint-based methods to real-life projects.
- Advanced topics that arise from the usage of constraints in the context of the verification of high-end processors and systems.

TUTORIAL 4 - ADVANCEMENTS IN ENERGY-EFFICIENT DESIGN

Rm: **208AB**

Organizer: **Barry Pangrle** - *Synopsys, Inc., Mountain View, CA*
Presenters: **David Flynn** - *ARM Ltd., Cambridge, UK*
David Tamura - *National Semiconductor, Santa Clara, CA*
David Blaauw - *Univ. of Michigan, Ann Arbor, MI*
Barry Pangrle - *Synopsys, Inc., Mountain View, CA*

Key trends in power management for energy-efficient design will be described along with the latest research techniques that address them.

Key Trends

- Lower Voltages
- Lower Threshold Voltages
- Multiple Threshold Voltages
- Dynamic Voltage Scaling
- Dynamic Frequency Scaling
- Adaptive Voltage Scaling

Power Management Areas

- Analysis and Minimization Techniques for Total Leakage
- Power Optimization Using Multiple Supply and Threshold Voltages
- Asynchronous Level Converters and Level Converting Logic Circuits for Multi-VDD Design
- Analysis and Design of Level-Converting Flip-Flops for Dual-VDD/Vth Integrated Circuits
- Voltage-scalable SRAM with Timing Speculation and Error Correction
- Dual Vth, Dual VDD, and sizing optimization
- A New Algorithm for Improved VDD Assignment in Dual VDD Systems

Tutorials - Friday June 17, 2005

TUTORIAL 5 - DESIGN FOR MANUFACTURING AT 65 NM AND BELOW

Rm: **209AB**

Organizer: **Lou Scheffer** - *Cadence Design Systems, Inc., San Jose, CA*
Presenters: **Lou Scheffer** - *Cadence Design Systems, Inc., San Jose, CA*
Sani Nassif - *IBM Corp., Austin, TX*
Andrzej Strojwas - *PDF Solutions, Inc, San Jose, CA*
Bernd Koenemann - *Mentor Graphics Corp., San Jose, CA*
Nagaraj NS - *Texas Instruments, Inc., Dallas, TX*

Modern processes (65 nm and below) require extra attention to ensure that designs are manufacturable with acceptable yield, in addition to the traditional problem of logical and physical correctness. Yield losses in these processes include functional defects, performance problems, excessive leakage, and problems with testing. Designers and tool developers need to understand each of these sources of yield loss, and devise ways to minimize their impact. This tutorial will describe in detail the problems unique to, or exaggerated by, very small devices and interconnect. These include increased process variability, increased leakage, increased electrical noise, new requirements for resolution enhancement techniques such as OPC and PSM, and new yield loss mechanisms. It will then cover various techniques that can be used to mitigate these problems. These include measurement and characterization of process variation (leading to design centering), statistical timing, yield estimation and modeling, testing specialized to uncover and diagnose DFM issues, and analysis and minimization of electrical noise, OPC aware placement and routing, leakage minimization, and provisions for Iddq testing in the presence of leakage.

TUTORIAL 6 - DESIGN OF SOC WITH EMBEDDED PROCESSORS

Rm: **207ABC**

Organizer: **Ahmed Jerraya** - *TIMA Lab, Grenoble, France*
Presenters: **Wayne Wolf** - *Princeton Univ. , Princeton, NJ*
Chris Rowen - *Tensilica, Inc., Santa Clara, CA*
Kees Vissers - *Xilinx Research Labs, San Jose, CA*
Vojin Zivojnovic - *ARM Ltd., Irvine, CA*
Santanu Dutta - *nVIDIA, San Jose, CA*

Embedded processors are ubiquitous in today's chips. 90% of new ASICs in 130 nm technology already include a CPU. Heterogeneous cores are exploited to meet the tight performance and cost constraints. Multimedia platforms already use several different kinds of programmable processors (DSPs and microcontrollers). As we move to advanced processes, multiprocessor SoCs (MPSoC) will be designed for a wide range of applications.
These SoCs will be composed of multiple, possibly highly parallel processors and will contain very sophisticated communication networks-on-chips (NoC). Additionally SoC design also requires complex software development including I/O drivers, operating systems, and service-oriented middleware.
The design methodologies required to develop these chips will use (dedicated or programmable) processors as basic components instead of logic modules (gate, operator) used by the current methods. The processor executing tasks concurrently will become the key design component.
This tutorial will cover new design techniques that can help system-on-chip designers successfully:

- Developing specific SoC hardware platforms including architecture exploration and performances validations
- Developing the embedded software including the development of specific I/O drivers and memory management routines
- Debugging the overall HW-SW system including the simulation of long input sequences

UML for SoC Design Workshop

Sunday, June 12 • 9:00 am - 6:00 pm

Rm: **207AB**

The program for the workshop on the Unified Modeling Language™ (UML) 2.0 for System-on-Chip (SoC) design includes papers from design teams and researchers around the globe. A keynote by Yves Vanderperren from the department of electrical engineering at Katholiek Universiteit in Belgium will open the workshop. His talk will describe SysML and systems engineering applied to SoC design. Other presentations will explore UML for SoC and embedded systems, UML synthesis, modeling and hardware and software design methodologies. As UML 2.0 nears acceptance as an Object Modeling Group™ (OMG) standard, industrial and academic groups from Electronic Design Automation (EDA), embedded software, systems and design communities have started to apply it to SoC design. The workshop, open to anyone interested in learning more about UML for SoC design, is meant to initiate discussion and to exchange information.

REGISTRATION INSTRUCTIONS

No Conference Registration is required.

$100 ACM/IEEE Members

$150 Non-Members

Opening and Keynote Address

9:00 ***Welcome and Introduction by the Workshop Organizers***
L. Lavagno- *Cadence Berkeley Labs*
W. Mueller- *Paderborn Univ.*

9:15 ***SysML and Systems Engineering Applied to SoC Design***
Y. Vanderperren - *Katholiek Univ., Leuven, Belgium*

Emerging OMG Profiles for SoCs and Embedded Systems

9:45 ***MARTE: A New OMG Profile RFP for the Modeling and Analysis of Real-Time Embedded Systems***
Charles Andr´e, Robert De Simone, Yves Sorel, Fr´ed´eric Mallet - *INRIA/I3S*
Arnaud Cuccuru, Jean-Luc Dekeyser, C´edric Dumoulin - *INRIA/LIFL*
Julien Forget, Thierry Gautier - *INRIA*
S´ebastien G´erard, Ansgar Radermacher - *CEA*
Laurent Rioux, Thierry Saunier - *Thales*

10:15 ***UML Profile for System-on-Chip (SoC)***
Sreeranga Rajan - *Fujitsu Laboratories of America, Sunnyvale, CA*
Takashi Hasegawa, Minoru Shoji, Q. Zhu, and Nakata Tsuneo - *Fujitsu Limited, Kanagawa, Japan*

10:45 **Break**

Synthesis and Execution of UML Models

11:00 ***Interface Problems: What We Have Here is a Failure to Communicate***
S. Mellor, J.R. Wolfe, C. McCausland - *Accelerated Technology*

11:30 ***Synthesis of UML-Models for Reconfigurable Hardware***
Ch. Dorotska, D. Froehlich, B. Steinbach - *Technische Univ. Bergakademie Freiberg, Germany*

12:00 ***Using UML Activities for Synthesis on Reconfigurable Hardware***
T. Schattkowsky, J.H. Hausmann, A. Rettberg - *Paderborn Univ., Germany*

12:30 **Lunch** - Rm: **205B**

Models of Computation for SoC Design

2:00 ***On the Integration of UML Sequence Diagrams and Actor-Oriented Simulation Models***
L.S. Indrusiak, A. Thuy, M. Glesner - *TU Darmstadt, Germany*

2:30 ***Interacting Process Classes: Modeling and Simulation***
A. Goel, K.D. Nguyen, A. Roychoudhury, P.S. Thiagarajan - *Univ. of Singapore, Singapore*

3:00 **Break**

HW/SW Design Methodologies

3:30 ***Design and Synthesis of Reusable Platforms with Programmable Interconnects***
A.S. Basu, M. Lajolo - *NEC-Labs America, USA*
M. Prevostini - *Univ. of Lugano, Switzerland*

4:00 ***An SoC Design Flow Based on UML 2.0 and SystemC***
S. Bocchio- *STMicroelectronics,* **E. Riccobene** - *Univ. di Milano, Italy*
A. Rosti - *STMicroelectronics,* **P. Scandurra** - *Univ. di Catania, Italy*

4:30 **Break**

Performance Analysis Based on Abstract UML Modeling

5:00 ***Performance Analysis of Sequence Diagrams for SoC Design***
A. Viehl, O. Bringmann- *FZI, Karlsruhe, Germany*
W. Rosenstiel - *Univ. of Tübingen, Germany*

5:30 ***Embedded SW Design Exploration Using UML-Based Estimation Tools***
M.F.da S. Oliveira, L. Brisolara, F.R. Wagner, L. Carro - *Federal Univ. of Rio Grande do Sul (UFRGS), Brazil*

Closing

6:00 ***Workshop Wrap-up by the Organizers***
L. Lavagno, W. Mueller

First Integrated Design Systems Workshop

Monday, June 13 • 12:00 pm - 5:00 pm

Rm: **207D**

Organizers: **John Darringer** - *IBM Corp.*, **Rahul Goyal** - *Intel Corp.*, **Alva Barney** - *Hewlett-Packard Co.*, **Scott Peterson** - *LSI Logic Corp.*

REGISTRATION INSTRUCTIONS
No Conference Registration is required.
$50.00
ACM/IEEE Members
$75.00
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Objective - The era of "point tools" linked by files is long over. Streamlined Integrated Design Systems are essential to meet today's business demands. Custom chip designers struggle to integrate growing numbers of macros while ensuring manufacturability. ASIC and SoC designers must optimize many factors simultaneously to achieve "Design Closure." Product designers are exploring 3D IC and SiP to fully exploit chip and package synergy and remain competitive. What does it take to develop effective Integrated Design Systems? Vendors provide solutions for parts of a methodology, but most users want to exploit the best tools from multiple vendors and add proprietary applications to gain a competitive advantage. Progress has been made on standard APIs for sharing data, but much more is needed to enable design systems to keep pace with the industry.
Agenda - This workshop brings together design system managers and design system providers from industry leading companies to assess the state of integrated design systems today and identify the remaining challenges that need to be addressed. In addition, representatives from academia, related standards groups, and industry "gurus" will participate with their views. A panel session will bring the speakers together to address your questions and let your comments be heard. Overall, the goal is to focus attention to one of the most important issues facing the electronics industry.

12:00 pm **Lunch**
1:00 pm **Welcome:** **John Darringer** - Research Manager, *IBM Corp.*
1:20 pm **User Views** Chair: **Alva Barney** - CAD Manager *Hewlett-Packard Co.*

- **Siva Yerramilli** - *GM Design Technology, Intel Corp.*
- **David Kung** - *Sr. Manager, Design Automation, IBM Corp.*
- **Lambert van den Hoven** - *VP and GM Design Technology, Philips*
- **Yoshio Inoue** - *Group Manager EDA Methodology Renesas Technology Corp.*

2:10 pm **Vendor Views** Chair: **Rahul Goyal** - *Dir. EDA Business, Intel Corp.*

- **Aurangzeb Khan** - *Corporate VP and GM, Design Foundries, Cadence Design Systems, Inc.*
- **Eshel Haritan** - *VP Engineering, CoWare, Inc.*
- **Premal Buch** - *GM Design Implementation, Magma Design Automation*
- **Greg Hackney** - *Program Manager Strategic Partnerships Mentor Graphics Corp.*
- **Rich Goldman** - *VP Strategic Market Development, Synopsys, Inc.*

3:00 pm **Other Views** Chair: **Scott Peterson** - *Dir. Rapid Chip Methodology, LSI Logic Corp.*

- **Gary Smith** - *Chief Analyst, Gartner Dataquest*
  The Automation of RTL Design
- **Steve Schulz** - *CEO, Si2, Inc.*
  How Standards Can Help
- **Andreas Kuehlmann** - *Dir., Cadence Berkeley Labs*
  University Research on Integrated Design Systems
- **Jim Solomon** - *CEO, Xulu Entertainment*
  The Role of Start-ups

3:50 pm **Break**

4:10 pm **PANEL: What's Next?** Chair: **Richard Goering** - *Editor, EE Times*

5:00 pm **Adjourn**

ogic Corp.

visit the DAC web site @ www.dac.com for more details

Workshop for Women in Design Automation

Cultural Evolution: Keeping Pace with Organizational Diversity

Monday, June 13 • 1:00 pm - 5:00 pm

Rm: **207AB**

Workshop Chair: **Telle Whitney** - (pictured)
Anita Borg Institute for Women in Technology

Steering Committee:

Nanette Collins - *Publicity Chair, 42nd DAC*
Marie R. Pistilli - *Co-Chair, Board of Directors, MP Associates, Inc.*
Ann Marie Rincon - *Engineering Fellow, AMI Semicondutor*

SCHEDULE

1:00 pm - 2:00 pm	**Registration and Lunch**
2:00 p m - 3:45 p m	**Keynote Address and Panel**
3:45 p m - 4:15 p m	**Achievement Award Ceremony**
	Join us as we honor Kathryn Kranen as this year's Marie R. Pistilli Women in EDA Achievement Award.
4:15 p m	**Wine/Cheese Reception**

Keynote **Jane Margolis** - *Ed. D., Research Educationist, Univ. of California, Los Angeles Graduate School of Education and Information Studies*

Jane Margolis is co-author of the award-winning book *Unlocking the Clubhouse* (MIT Press, 2002). This book resulted from a four-year study of the gender gap at Carnegie Mellon University School of Computer Science. Her work focuses on inequity in education. She is currently involved in a three-year study in Los Angeles public schools, which examines why so few African-American and Latino students are learning computer science at the high school level. She received her doctorate from the Harvard Graduate School of Education in 1990, where she studied with feminist psychologist Carol Gilligan. Margolis has discussed her research on radio, at universities, and at industries around the country.

Panel Discussion

Don't miss the opportunity to learn how prominent professionals in the industry have made career choices to achieve a rewarding personal and professional life experience. Each of us has the chance to influence our organization in fundamental ways if we have the tools. Building on the work described in the keynote, which resulted in significant cultural changes at Carnegie Mellon Univ., the panelists will describe their own experience about the impact they have made on their organizations. We are pleased to have panelists from companies and organizations of very different sizes, product lines, and focus. You can expect to walk away with concrete examples of changes that work.

Moderator: **Jim Lipman** - *Cain Communications*
Panelists: **Limor Fix** - *Intel Corp.*
Kathryn Kranen - *Jasper Design Automation, Inc.*
Daya Nadamuni - *Gartner Dataquest*
Tajana Simunic Rosing - *Univ. of California at San Diego*
Terri Timberman - *AMI Semiconductor*

REGISTRATION INSTRUCTIONS

No Conference Registration is required.

$50.00 ACM/IEEE Members
$75.00 Non-Members

Sponsored by:

Introduction to Chips and EDA for a Non-Technical Audience

Monday, June 13 • 10:00 am - 12:00 pm

Rm: **208A**

ORGANIZER: **Pamela McDaniel** - *Synopsys, Inc., Mountain View, CA*
SPEAKER: **Karen Bartleson** - *Synopsys, Inc., Mountain View, CA*

REGISTRATION INSTRUCTIONS
No Conference Registration is required.
$10.00 **Registration Fee**

Are you new to the Electronic Design Automation (EDA) or chip industry? Have you been in the industry for a while and want to get just a little bit closer to technology? Do you wonder what everyone is talking about at the Design Automation Conference but are afraid to ask? Are you baffled by terms like "semiconductor," "yield," "synthesis," "ESL," "simulation," "design for manufacturing," and "tape-out"? If so, then please plan to attend this workshop to gain a basic understanding of chip design and of the wonderful world of Electronic Design Automation.

This workshop provides

- A simplified explanation for the non-technical person of how chips are designed and manufactured
- An understanding of how essential Electronic Design Automation is to chip design
- An opportunity to see and touch the parts that make up chips and electronic products
- A non-threatening, fun event with working knowledge to take away

This workshop is for

- Non-engineering staff from technology companies
- Analysts and media people unfamiliar with EDA and semiconductor industries
- Educators and students who are curious about chip technology and design automation
- Friends and relatives of technical people

Workshop objectives

- Provide a basic understanding of EDA and semiconductors to non-technical people
- Present information in simple, easy-to-understand terms
- Use hands-on parts (wafers, chips, masks…) for enhanced experience
- Encourage people to join and invest in the EDA industry
- Address ongoing requests to help non-technical people understand the EDA industry.

Please note

- This workshop is similar to the one presented at DAC 2004
- The workshop is for non-technical attendees
- Maximum class size: 50

Hands-on Tutorials

General Information

Hands-on Tutorials are three-hour tutorials presented by exhibitors to demonstrate their solutions to a particular issue. This year DAC is offering two Hands-on Tutorials on RTL Handoff and four Hands-on Tutorials on Core-Based SoC Design. This is an opportunity for attendees with a need to learn about or evaluate products in these areas a chance to see, in an in-depth manner, a variety of solutions. Demonstrations are done with the attendees working from workstations while the presenters lead the discussion. The tutorials are limited to the first 30 attendees with a student to workstation ratio of 2:1. Due to the proprietary nature of the discussions, presenting companies have the right to refuse access to employees or contractors of competitors.

Registration Information: The cost per tutorial is $75 and attendees are encouraged to enroll in more than one tutorial. Attendees must register for a minimum of an exhibits-only registration to be eligible to enroll in a Hands-on Tutorial.

TERA SYSTEMS RTL Handoff Technology

(TERA SYSTEMS, INC.)

Monday, June 13 **9:00 am - 12:00 pm** Rm: **211AB**

The keys to enable RTL handoff include thorough code analysis, early constraint analysis, reduction of gate level complexity, correct physical floorplan early-on in the design, and rapid evaluation. Ease of integration with existing design flows and ease of use are corollary needs.

RTL handoff runs on existing Verilog or VHDL RTL and utilizes a higher level of abstraction, like TeraForms Tera Gates which can reduce chip complexity (number of instances) by 10x-100x. TeraForm supports rapid floorplanning, routing and analysis. Unique cross-probing between RTL, the TeraGate netlist and physical layout enables problem correction at the RTL level. A clean RTL design results in successful design closure through subsequent place, route and design rule checks.

What DAC Tutorial Attendees Will Do:

After an introductory lecture, attendees will run TeraForm using an example case (a 32-bit processor, 350K gates, in a 90-nm process). They will explore TeraSystem's unique cross probing between RTL, TeraGate netlist and the chip layout. Attendees will run analyses, identify a design problem and make design changes to relieve the problem. They will re-run the modified design, and observe the results.

Expected Educational Benefits:

Attendees will get an introduction to real RTL handoff and the benefits of early correction of logical and physical problems early in the design. Attendees will experience the unique benefits of the TeraSystems approach (speed, high-level iteration, early physical estimation, etc.). They will learn what the TeraGate and TeraForm technology tools can do, and how TeraForm can solve real world design problems.

Enabling RTL Handoff via Predictive Development

(Atrenta, Inc. and Conexant Systems, Inc.)

Monday, June 13 **2:00 pm - 5:00 pm** Rm: **211AB**

With shrinking process geometries, design sizes and complexities continue their relentless march along the Moore's Law curve. The time taken to capture and verify RTL descriptions is keeping pace with the complexity curve, while the time spent ripping up and repeating work already completed during detailed implementation phase is increasing faster yet. Long wide logic cones make it difficult to meet timing objectives. Debugging test issues at the gate-level is an extremely lengthy and cumbersome process. Circuit modifications to insert RTL clock gating result in sub-optimal solutions that complicate functional verification, while the insertion of power and voltage domains is another potential error injection point. Without well-structured and optimal RTL, latent design issues crop up during implementation, requiring expensive implementation licenses to be dedicated to circuit debug and issue resolution. Predictive development aims to invert the design:debug ratio, connecting designer's RTL knowledge to highly-leveraged design decisions that smooth downstream implementation tasks.

This tutorial is an overview of how predictive development can improve the efficiency, cycle time, robustness, and predictability of IC design. By closing at the RT level, designers can be sure that their chosen micro-architecture is not only optimized to meet external system requirements, but can be smoothly and efficiently implemented through logic and physical design while meeting timing, power, test, area, and routing constraints.

The tutorial covers the basic synthesis-driven design methodology from planning to final place and route, describing data requirements at each handoff point. Predictive development is then discussed and described using relevant examples to illustrate how downstream issues in timing, power and test are identified and resolved in the source RTL. Using the practical techniques that we will show, designers will understand how they can achieve closure at the RT level. With these techniques augmenting today's industry-standard physical synthesis implementation flows, and with a deterministic path from RTL to final STA, the long-held goal of RTL handoff is within our reach.

Designing Extendable Cores with Low-Cost Metal Programmable Technology

(Magma Design Automation, Inc.; CoWare, Inc.; MIPS Technologies, Inc.; Virage Logic Corp.)

Tuesday, June 14 **2:00 pm - 5:00 pm** Rm: **211AB**

Attend this hands-on tutorial to experience a design flow that uses CoWare's System Level Design to explore and extend the functionality of a MIPS32® 24K™ Pro Microprocessor core using Virage Logic's ASAP Logic Metal Programmable library in Magma's unified implementation flow. In this tutorial, attendees will observe a complete system level design process, starting from exploring the system architecture, trading-off hardware and system software partitioning, and the creation of CorExtend User Defined Instructions using CoWare's CorXpert. The resultant Instructions can then be synthesized in the RTL implementation flow. The CorExtend block serves to extend the instruction set of the MIPS core so that the hardware can better perform application-specific tasks. CorExtend instructions also provide flexibility to extend the capability of the base design with faster design turn around time at much lower manufacturing cost.

The implementation flow will take advantage of MIPS inherent high-performance architecture and Magma's unified platform using Virage Logic's Metal Programmable Cell Library to achieve a near standard cell quality of results, including the enhanced CorExtend block to provide greater flexibility to optimize the design for a specific application.

Design of Multi-Core Systems with SystemC and Retargetable Processor Tools

(Target Compiler Technologies and Mentor Graphics Corp.)

Wednesday, June 15 **9:00 am - 12:00 pm** Rm: **211AB**

Next-generation communication, information and entertainment systems increasingly rely on efficient SoC designs to meet their low-cost, low-power, high-performance, and high-flexibility requirements. Such SoCs are essentially heterogeneous multi-core systems. They contain a multitude of application-specific instruction-set processor (ASIP) cores that serve as programmable accelerators, complementing the more conventional microprocessor and DSP cores, together with an optimized hierarchical memory and interconnect structure.

The design of such multi-core systems requires novel integrated EDA flows, addressing both the design of new ASIP cores, the delivery of software development tools for such cores, and a seamless integration of all cores in a system-level model based on SystemC. The purpose of this hands-on tutorial is to introduce such a design flow, based on offerings from Mentor and Target. The key tools that will be combined in this tutorial are:

- Mentor's ModelSim environment, one of the industry's most complete multi-level simulation tools, from SystemC up to RTL level.
- Target's Chess/Checkers environment, a state-of-the-art retargetable tool-suite for the design, programming, and verification of ASIPs.

The tutorial will demonstrate how new ASIP cores can be designed and programmed quickly, while at the same time ensuring the correctness of the design, not only at the level of individual cores but also at the overall system level. A demo application will be designed, including high-level SystemC simulation, design and programming of several ASIP cores, co-simulation, and verification of the resulting multi-core architecture.

A basic knowledge of SystemC, Verilog, and processor architecture would be recommended for participating in this tutorial.

Using Configurable Processors to Replace RTL Blocks

(Tensilica, Inc. and Virage Logic Corp.)

Wednesday, June 15 **2:00 pm - 5:00 pm** Rm: **211AB**

Because configurable processors employ firmware instead of state machines for control algorithms, it's easier and faster to develop and verify processor-based task engines than RTL-based hardware. Learn how fast you can design a configurable processor using Tensilica's XPRES Compiler and how to select the best corresponding embedded memory IP from Virage Logic.

Students will take a complex C-based algorithm and use the XPRES compiler to create several trial processor configurations that boost performance. Options for guiding the tool, selecting instructions, viewing area/performance trade-offs and, if necessary, tuning the original application to take better advantage of the added hardware instructions will be explored.

Students will choose from a variety of memory types for various foundries and process technologies. The web-based Virage memory generators allow designers to optimize the size, latency, and organization of the memory subsystem in conjunction with optimizing the processor configuration itself.

Once the processor is generated, students will compile the original C code and run it on that processor. No modifications are needed to the original C code or any other C code to take advantage of the new instructions added to the configurable processor. The compiler exploits new instructions automatically.

At completion of this 3-hour tutorial, students should have a good idea of the capabilities of configurable processors as well as the steps involved in the design process so they can decide if they want to use configurable processors in their design process.

Virtual System Prototypes for Core-Based SoC Design

(VaST Systems Technology and StarCore, LLC)

Thursday, June 16 **9:00 am - 12:00 pm** Rm: **211AB**

Virtual system prototypes are software simulation-based models of electronic systems and SoCs used for the development and evaluation of the system architecture, software development, and hardware verification. A virtual prototype can include one or more processors, buses, hardware peripheral components, and even models of mechanical subsystems that are part of the overall system. The virtual prototype runs the same compiled and linked target code as does the real or prototype hardware, accurately predicting the system's real-world behavior. In addition, the virtual system prototype is cycle-accurate so that the model accurately portrays real-time, critical control system behavior. In this session, participants will learn how a virtual system prototype is created and then used to enable architectural exploration and optimization plus concurrent development of hardware and software in which both are tightly linked back to architectural specification and system-level validation.

The heart of a Virtual System Prototype is the virtual processor model. StarCore and VaST have worked together to create a high-performance, cycle-accurate software model of the StarCore SC1200 processor core, which includes the cache subsystem.

Participants will be introduced to design methods and tools using the StarCore processor model with VaST's electronic system level (ESL) design tools. We will demonstrate how this enables designers to test and validate software such as RTOSs, drivers, and applications, long before actual silicon is available. Users of VaST Virtual System Prototypes have cut as much as nine months off their development time using these techniques.

Sponsors

The 42nd Design Automation Conference is sponsored by IEEE/CASS /CANDE (Institute of Electrical and Electronics Engineers/Circuits and Systems Society/Computer Aided Network Design), the ACM/SIGDA (Association for Computing Machinery/Special Interest Group on Design Automation), and the EDA Consortium (Electronic Design Automation Consortium). Membership information is available on the sponsor's web site or at the conference at the ACM and IEEE booths.

IEEE Circuits and Systems Society

The IEEE Circuits and Systems Society (CASS) is one of the largest societies within IEEE and in the world devoted to the analysis, design, and applications of circuits, networks, and systems. It offers its members an extensive program of publications, meetings, and technical and educational activities, encouraging an active exchange of information and ideas. The Society's peer reviewed publication activities include Trans. on CAD; Trans. on CAS-Part I (Regular Papers); Trans. on CAS-Part II (Express Briefs); Trans. on VLSI; Trans. on CAS for Video Technology; Trans. on Multimedia; and the new Transactions on Mobile Computing which is co-sponsored with IEEE sister societies. CASS also sponsors or co-sponsors a number of international conferences, which include the Design Automation Conference (DAC), the Int'l Conference on Computer-Aided Design (ICCAD) and the Int'l Symposium on Circuits & Systems (ISCAS). A worldwide comprehensive program of advanced workshops including a new series on "Emerging Technologies in Circuits and Systems," as well as our continuing education short courses, bring to our worldwide membership the latest developments in cutting-edge technologies of interest to industry and academia alike. The IEEE/CASS has been serving its membership for over 50 years with such member benefits as:

- Discounts on all Society publications, conferences and workshops (including co-sponsored and sister society publications and conferences)
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Computer Aided Network Design (CANDE)

is a technical committee of the IEEE Circuits and Systems Society. CANDE is dedicated to bringing design automation professionals together to further their education, to assist in building relationships, and to sponsor initiatives which grow the CAD/EDA industry. CANDE sponsors a workshop in the Fall to address emerging technologies and to provide an opportunity for the generation of new ideas. CANDE is the sponsoring technical committee from CASS for both DAC and ICCAD.

For more information, please contact the IEEE/CASS/CANDE.

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ACM/SIGDA, one of the three organizations that sponsor DAC, has a long history of supporting DAC and the EDA profession. In addition to sponsoring DAC, SIGDA sponsors ICCAD, DATE, and ASP-DAC, and many smaller EDA conferences, symposia, and workshops.

SIGDA has pioneered electronic publishing of EDA literature since 1989, and now produces CD-ROM proceedings for most major EDA conferences and symposia. For the past 10 years, SIGDA has also produced an annual CDROM Compendium of those proceedings, which has grown this year to a Super-Compendium DVD containing 10 years of EDA literature; this Compendium is sent to our members yearly as a member benefit. Further, SIGDA provides strong support for the ACM journal TODAES (Transactions on Design Automation of Electronic Systems).

SIGDA also publishes two electronic "newsletters." SIGDA's E-Newsletter is sent to all members twice each month, and contains information on upcoming conferences and funding opportunities. SIGDA's DA TechNews provides all SIGDA members with a summary of the latest EDA news twice each month.

In addition to electronic publishing, SIGDA provides a broad array of additional resources to its members and to the EDA profession in general. SIGDA organizes and provides partial funding for the University Booth and Ph.D. Forum at DAC and the CADathlon at ICCAD, and funds various scholarships and awards. SIGDA also publishes its Monthly Planner several times per year, helping EDA professionals plan their conference activities. For further information on SIGDA's programs and resources, see http://www.sigda.org.

In addition, SIGDA members may also want to consider joining our parent organization, ACM. ACM membership provides access to a variety of ACM products and resources, including discounts on conferences, subscriptions to ACM journals and magazines, and the ACM Digital Library, an invaluable IT resource. For further details, see ACM's home page at http://www.acm.org.

As an EDA professional, isn't it time YOU joined SIGDA?

SIGDA/DAC University Booth

Each year SIGDA organizes the University Booth. The booth is an opportunity for university researchers to display their results and to interact with visitors from industry. Priority is given to presentations that complement the conference technical program. Demos that highlight benchmark results are also encouraged. The Design Contest winners will give demonstrations presenting their designs at the University Booth, Tuesday, June 14, 12:00 pm - 2:00 pm. The schedule of presentations will be published at the conference and will also be available on the SIGDA web site. We thank the Design Automation Conference for its continued support of this project.

42nd DAC Proceedings

The 42nd DAC proceedings will contain 181 papers, panels, and special sessions. DAC is offering each conference and student registrant 42 years of DAC proceedings on DVD. One hardbound copy of this year's proceedings will be available to registrants for $35 at the time of registration. Should you wish to purchase additional copies, you may do so at the ACM kiosk or the IEEE booth located on the second level via self-help on-line computer orders. After the conference, mail orders should be sent to ACM or IEEE. The addresses for mail orders are:

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ACM is a major force in advancing the skills of information technology professionals and students. ACM serves its global membership of 75,000 by delivering cutting edge technical information and transferring ideas from theory to practice. ACM hosts the computing industry's leading Portal to Computing Literature. With its journals and magazines, special interest groups, conferences, workshops, electronic forums, Career Resource Centre and Professional Development Centre, ACM is a primary resource to the information technology field. For more information, see www.acm.org.

In 1997, ACM launched its Digital Library, which has now evolved into the ACM Portal. The Portal is an invaluable online resource of more than one million fully searchable pages of text (including a 40+ year archive) from ACM's high quality journals and proceedings dating back to the 1950s. The Portal also reaches the entire world of computing through the fully integrated Online Guide. Additionally, ACM has 33 Special Interest Groups that focus on different computing disciplines. More than half of all ACM members join one or more of these Special Interest Groups. The SIGs publish newsletters and sponsor important conferences such as SIGGRAPH, OOPSLA, DAC, ICCAD, and CHI, giving members opportunities to meet experts in their fields of interest and network with other knowledgeable members.

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EDA Consortium

The EDA Consortium is the international association of companies that provide tools and services that enable engineers to create the world's electronic products.

The EDA Consortium addresses issues that are common to its members and the community they serve. Recent accomplishments include simplification of international EDA export regulation and publication of an industry Operating Systems Roadmap.

Companies that become EDA Consortium members are eligible for a 10% discount on DAC Exhibit Space. Contact the EDA Consortium today about membership opportunities.

43rd DAC Call for Papers

43rd Design Automation Conference • July 24 - 28, 2006

Moscone Convention Center, San Francisco, CA

DAC is the premier conference devoted to Design Automation (DA) and the application of DA tools in designing electronic systems. Four types of submissions are invited: regular papers, special topic sessions, panels, and tutorials. Submissions must be made electronically at www.dac.com. **Panel and Tutorial suggestions, and Special Session submissions are due NO later than 5:00 pm MST, November 2, 2005; Regular Papers are due NO later than 5:00 pm MST, December 19, 2005; Student Design Contest submissions are due no later than 5:00 pm MST, December 6, 2005.**

DAC 2006 is seeking papers that deal with design tools, design methods and case studies, and embedded design in a number of categories described below.

Design Tools papers describe contributions to the research and development of design tools and their supporting algorithms.

Design Methods and case studies papers describe innovative methodologies for the design of electronic circuits and systems, as well as creative experiences with design automation in state-of-the-art design projects.

Embedded Systems are characterized by mixed hardware and software components with limited resources. Increases in software content introduce new system design issues. Embedded design papers describe tools, methods, and case studies for applications with specific embedded system content.

Requirements for Submission

Regular paper submissions must (1) be in PDF format only, (2) contain an abstract of approximately 60 words clearly stating the significant contribution, impact, and results of the submission, (3) be no more than 6 pages (including the abstract, figures, tables, and references), double columned, 9pt or 10pt font, and (4) MUST NOT include name(s) or affiliation(s) of the author(s) anywhere on the manuscript, abstract, or bibliographic citations. Format templates are available on the DAC web site for your convenience, but are not required. Submissions not adhering to these rules, or those previously published or simultaneously submitted to another conference, will be rejected. Additional submission guidelines are available on the DAC web site (after Sept. 1, 2005). All regular papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage. Authors of accepted papers must sign a copyright release form for their paper. Notice of acceptance will be sent via email by April 17, 2006.

Special session submissions must include descriptions of suggested papers and speakers, and the importance of the special session to the DAC audience. DAC reserves the right to restructure all special sessions.

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure all panels and tutorials.

Students are invited to submit descriptions of original electronic designs, either circuit level or system level. **Student Design Contest paper submissions** must (1) be in PDF format only, (2) contain the title of the project, (3) contain an abstract of approximately 60 words, (4) contain a complete description of the project, and (5) be no more than 6 pages (including the abstract, maximum of 10 figures/tables, and references), double-columned, 9pt or 10pt font. The submission should clarify the originality, distinguishing features, and measured performance of the design. Two categories of designs - operational and conceptual - are eligible for awards. For operational designs, proof-of-implementation is required, while for conceptual designs, complete simulation is necessary. Designs must have taken place as part of the students' work at the university and must have been completed after June 2004. Submitted designs should not have received awards in other contests. Selected designs will be presented at the conference (and at ISSCC in February 2006). Additional submission guidelines are available on the DAC web site.

ALL SUBMISSIONS MUST BE MADE ELECTRONICALLY AT THE DAC WEB SITE: WWW.DAC.COM

43rd DAC Call for Papers

Submitters no longer need to specify a tools, methods, or embedded systems track, but only specify a category from the 18 listed.

1. Circuit Simulation and Timing Analysis
- Electrical-level circuit and timing simulation
- Static timing analysis and timing verification
- Electrothermal simulation methods

2. Design-for-Manufacturability
- Design for yield, cost issues, and impacts of DFM
- Process technology development, extraction, measurement, and modeling
- Statistical performance analysis and optimization
- Reticle enhancement, lithography-related design optimizations

3. Power Analysis and Low-Power Design
- Analysis and estimation of power
- Embedded low-power approaches: partitioning, scheduling, and resource management
- Device, circuit, and system techniques for low-power design
- Impacts on thermal management of low-power design techniques

4. Testing
- Digital, system, memory, analog/mixed-signal, and RF test
- ATPG, fault modeling, DFT and BIST, test debugging
- Scan-based testing, delay testing, on-line testing
- Cost issues and impacts of testability

5. Verification
- Functional, transaction-level, RTL and gate-level modeling and verification of hardware design
- Dynamic simulation, equivalence checking, formal (and semi-formal) verification model and property checking
- Emulation and hardware simulators or accelerator engines
- Modeling languages and related formalisms, verification plan development and implementation
- Assertion-based verification, coverage-analysis, constrained-random testbench generation

6. IC Physical Design
- Physical floorplanning, partitioning, placement
- Buffer insertion, routing, interconnect planning
- Module generation, cell sizing, and library optimization
- Physical verification

7. Logic Synthesis
- Combinational, sequential, and asynchronous logic synthesis, both technology-independent and dependent
- Library mapping, cell-based design and optimization
- Transistor sizing
- Interactions between logic design and layout or physical synthesis

8. High-Level Synthesis
- High-level, behavioral, algorithmic, and architectural synthesis, "C" to gates tools and methods
- HW-SW interface synthesis, communication and network synthesis
- Synthesis of digital circuits above the RTL level
- Resource scheduling, allocation, and synthesis

9. Interconnect
- Interconnect modeling and extraction for current and advanced mainstream IC processes
- Model-order reduction methods for linear systems
- Substrate modeling with interconnect parasitic extraction
- High-frequency and electromagnetic simulation of circuits

10. Signal Integrity and Design Reliability
- Signal integrity, thermal analysis, and reliability modeling and analysis
- Timing, clocking, and power distribution, especially novel techniques
- Power grid robustness analysis and optimization
- Capacitive and inductive crosstalk noise
- Soft-errors and single-event upsets (SEUs)

11. Analog/Mixed-Signal and RF
- Analog, mixed-signal, and RF design
- Automated synthesis and macromodeling
- Simulation and optimization

12. FPGA Design Tools and Applications
- Rapid prototyping
- Logical synthesis and physical design techniques for FPGAs
- Configurable and reconfigurable computing

13. Embedded HW Design and Applications
- Case studies of embedded system design
- Flows and methods for specific applications and design domains

14. Embedded SW Tools and Design
- Retargetable compilation
- Memory/cache optimization
- Real-time single- and multi-processor scheduling, linking, loading
- Real-time operating systems

15. System-Level Design and Co-Design
- System specification, modeling, simulation, and performance analysis
- Scheduling, HW-SW partitioning
- IP and platform-based design, IP protection
- Communications-based design
- System-on-Chip (SoC), Network-on-Chip (NoC), Multi-processor SoC (MPSOC)
- Application-specific processor design tools

16. New, Emerging, or Specialized Design Technologies Including, but Not Restricted to
- MEMS, sensors, actuators, imaging devices
- Nano-technologies, nano-wires, nano-tubes
- Quantum computing
- Biologically based systems
- New transistor structures and devices, new or radical process technologies

17. Beyond Die-Integration and Packaging
- Chip-package-board codesign
- System-in-Package
- 3D design, stacked devices
- Analysis and optimization (signal integrity, physical layout, simulation) beyond the die

18. Special Theme Day—ENTERTAINMENT, GAMES, and MULTIMEDIA
- Design issues pertaining to mobile devices, music, video, broadcast, video on demand, and other multimedia/consumer entertainment devices
- Intensive multimedia processing as part of entertainment computing and specialized entertainment engine design
- Design and implementation of game playing, video, and audio engines
- Cross-platform entertainment and game software design and design implications
- System-level design approaches for games and multimedia entertainment devices

Awards

Marie R. Pistilli Women in EDA Achievement Award

- **Kathryn Kranen** - *President & CEO, Jasper Design Automation, Inc., Mountain View, CA*

For her significant contributions in helping women advance in the field of EDA technology.

The P.O. Pistilli Undergraduate Scholarships for Advancement in Computer Science and Electrical Engineering

The objective of the P.O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering and Computer Science from under-represented groups (women, African American, Hispanic, NativeAmerican, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship and SIGDA continues to administer the program for DAC. DAC normally funds two or more $4000 scholarships,renewable up to five years, to graduating high school seniors.

The 2005 winners are:

Elizabeth Hong-An Boi Ha - attending Georgia Institute of Tech., Atlanta, GA

Helen You - attending Massachusettes Institute of Tech., Cambridge, MA

For more information about the P.O. Pistilli scholarship, contact Dr. Cherrice Traver, ECE Dept., Union College, Schenectady, NY 12308. email: traverc@union.edu

Design Automation Conference Graduate Scholarships

Each year the Design Automation Conference sponsors several $24,000 scholarships to support graduate research and study in Design Automation (DA), with emphasis in "design and test automation of electronic and computer systems." Each scholarship is awarded directly to a university for the Faculty Investigator to expend in direct support of one or more DA graduate students.

The criteria for granting such a scholarship expanded in 1996 to include financial need. The criteria are: the academic credentials of the student(s); the quality and applicability of the proposed research; the impact of the award on the DA program at the institution; and financial need. Preference is given to institutions that are trying to establish new DA research programs.

The SPICE Modernization Project

Prof. Elias Kougianos - *Dept. of Engineering Technology, Univ. of North Texas, Denton, TX*

Student: Rahul Allawadhi

Spiral Inductor Synthesis for Mixed-Signal Systems

Prof. Yehia Massoud - *Dept. of Electrical and Computer Engineering, Rice Univ., Houston TX*

Student: Arthur Nieuwouldt

Information on next year's DAC scholarship award program will be available on the DAC web site: http://www.dac.com.

Awards

ACM Transaction on Design Automation of Electronic Systems (TODAES) 2005 Best Paper Award

Technology Mapping and Architecture Evaluation for k/m-macrocell-based FPGAs • **Volume 10, No. 1, January 2005, Pages: 3 - 23.**

Jason Cong - Univ. of California, Los Angeles, CA
Hui Huang - Sun Microsystems, Santa Clara, CA
Xin Yuan -IBM Corp., Essex Junction VT

The Association for Computing Machinery/Special Interest Group on Design Automation (ACM/SIGDA) presents its Distinguished Service Award

• **Mary Jane Irwin** - *Penn State Univ., University Park, PA*
For dedicated service as Editor in Chief of ACM Journal, TODAES (1998 - 2004), and many years of service to SIGDA, DAC, and the EDA profession.

2004 Phil Kaufman Award for Distinguished Contributions to EDA

• **Joe Costello** - Chairman and CEO of think3, Inc. and former Chairman and CEO of Cadence Design Systems, Inc.
For his business contributions that helped grow the EDA industry. Under his leadership (1987-1997), Cadence became the world's leading supplier of EDA software and services, and one of the top ten largest software suppliers in the world.

IEEE Circuits and Systems Society 2005 VLSI Transactions Best Paper Award

• **Radu Marculescu** - *Carnegie Mellon Univ., Pittsburgh, PA*
• **Girish Varatkar** - *Carnegie Mellon Univ., Pittsburgh, PA*
For the paper entitled, *On-Chip Traffic Modeling and Synthesis for MPEG-2 Video Applications*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 12, no. 1, pp. 108-119, January 2004

IEEE Circuits and Systems Society 2005 Darlington Award

• **Payam Heydari** - *Univ. of California, Irvine, CA*
For the paper entitled, *Analysis of the PLL Jitter Due to Power/Ground and Substrate Noise*, IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 51, no. 12, pp. 2404-2416, December 2004

IEEE Circuits and Systems Society 2005 Industrial Pioneer Award

• **Yervant Zorian** - *Virage Logic Corp., Freemont, CA*
For his contributions to design for test technology through Built-In Self-Test solutions and design tools that dramatically boosted the quality and reliability of digital systems and the efficiency of design and test engineers.

Awards

IEEE Circuits and Systems Society 2005 Outstanding Young Author Award

• **Chris Hyung-Il Kim** - *Purdue Univ., West Lafayette, IN*
For the paper entitled, *Ultra Low-Power DLMS Adaptive Filter for Hearing Aid Applications*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 11, no. 6, pp. 1058-1067, December 2003 (with H. Soeleman and K. Roy)

IEEE Circuits and Systems Society 2005 Donald O. Pederson Award

• **Subhasish Mitra** - *Intel Corp., Folsom, CA*
• **Kee Sup Kim** - *Intel Corp., Sacramento, CA*
For the paper entitled, *X-compact: An Efficient Response Compaction Technique*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 23, no. 3, pp. 421-432, March 2004

2005 IEEE Fellows

• **Fadi Joseph Kurdahi** - *Univ. of California, Irvine, CA*
For contributions to design automation of digital systems and to reconfigurable computing.

• **David J. Comer** - *Brigham Young Univ., Provo, UT*
For leadership in engineering education and publication of electronic circuit design textbooks.

• **Kartikeya Mayaram** - *Oregon State Univ., Corvallis, OR*
For contributions to coupled device and circuit simulation.

• **Chandu Visweswariah** - *IBM Corp., Yorktown Heights, NY*
For contributions to large scale integrated circuits.

• **Reinaldo Alvarenga Bergamaschi** - *IBM Corp., Yorktown Heights, NY*
For contributions to the development system design tools and methodologies.

• **Domine Leenaerts** - *Phillips Research, Eindhoven, Netherlands*
For contributions to nonlinear circuit theory and design.

DAC/ISSCC Student Design Contest

The purpose of the Student Design Contest is to promote excellence in the design of electronic systems by providing competition between graduate and undergraduate students at universities and colleges. This year we received over 50 submissions in two categories: "Conceptual" and "Operational." Operational designs are those which have been implemented and tested. Conceptual designs have not yet been fabricated and tested but must have been thoroughly simulated. Students compete for cash prizes donated by a number of industrial supporters, as well as the conference. Prize winners have been invited to show their work at the University Booth on the show floor. Awards will be given at the DAC Pavilion, on Wednesday, June 15, 2005 from 10:00 am - 10:45 am.

DAC/ISSCC 2005 Student Design Contest Winners

Operational Category:

1st Place **A 50MS/s (35mW) to 1kS/s (15µW) Power Scaleable 10b Pipelined ADC with Minimal Bias Current Variation**

Imran Ahmed, David Johns - *Univ. of Toronto, Toronto, ON. Canada*

2nd Place **A 1.3 TOPS H.264/AVC Single-Chip Encoder for HDTV Applications**

Tung-Chien Chen, Yu-Wen Huang, Chen-Han Tsai, To-Wei Chen, Ching-Yeh Chen, Liang-Gee Chen - *National Taiwan Univ., Taipei, Taiwan*

3rd Place **A Side-Channel Leakage Free Coprocessor IC in 0.18µm CMOS for Embedded AES-Based Cryptographic and Biometric Processing**

Kris Tiri, David Hwang, Alireza Hodjat, Bo-Cheng Lai, Shenglin Yang, Patrick Schaumont, Ingrid Verbauwhede - *Univ. of California, Los Angeles, CA*

Conceptual Category:

1st Place **Design and Implementation of a Fractional-N Frequency Synthesizer for Cellular Systems**

Petrus J. Venter, Saurabh Sinha - *Univ. of Pretoria, Pretoria, South Africa*

2nd Place **A 1-V IEEE 802.11a/b/g-Compliant Receiver IF-to-Baseband Chip in 0.35µm CMOS for Low-Cost Wireless SiP**

Pui-In Mak, Rui P. Martins - *Univ. of Macau, Macao SAR, China*
Seng-Pan U - *Chipidea Microelectronics (Macau) Ltd., Macao SAR, China*

3rd Place **Collision Detection System Using an FPGA Implemented on the FPX Platform**

Hasan N. Atay, Burchan Bayazit, John W. Lockwood - *Washington Univ., St. Louis, MO*

Award Contributors:

Additional Meetings

The 2005 EE Times EDA Users Survey

Monday, June 13 2:00 pm - 2:45 pm DAC Pavilion Booth 2269

Each year EE Times studies the likes and dislikes of design automation tool users and releases the data at DAC. This year's overview will be given Monday June 13 at the DAC pavilion by EE Times Editor in Chief Brian Fuller and EDA Editor Richard Goering.

The Annual X Initiative Anniversary Breakfast

Tuesday, June 14 7:30 am Ballroom D

The X Initiative, a consortium co-sponsored by Cadence, is focused on accelerating the adoption and fabrication of the X Architecture. The annual breakfast event at DAC serves as a platform to present the latest X Architecture silicon results and news and to celebrate the X Initiative's collaborative work. At the event, the consortium honors the year's recipient of the X Initiative Design-to-Manufacturing Catalyst Award, presented to the X Initiative member company that has made the greatest contribution towards making the X Architecture successful and bridging the gap between design and manufacturing. www.xinitiative.com

VSIA: Quality IP (QIP) Metric Updates and Training Session

Tuesday, June 14 12:00 pm - 1:30 pm Rm: **202B**

Join the VSIA and FSA to learn the latest developments with the VSIA Quality IP Metric including a new release, industry adoption and promotion. Following the QIP Metric update, VSIA and FSA will host an introductory QIP Metric training session. This event is open to all DAC attendees. Free lunch will be served.

Silicon Integration Initiative - Si2: Library Modeling Initiative – Open Industry Meeting

Wednesday, June 15 9:00 am - 12:00 pm Rm: **202A**

Silicon-accurate libraries are quickly becoming a huge bottleneck at finer process geometries. The complexity and quantity of sensitive parameters must be accounted for during characterization to support the design tools for the latest technology nodes. Design closure in the presence of an increasing set of intertwined constraints has become a growing challenge. Last year at DAC, the Design Technology Council, an organization of senior design technology leaders from leading semiconductor and systems companies, sponsored a summit meeting to discuss these problems with other IDMs, EDA vendors and IP providers. Over the last year the group has researched the problems and worked with leading EDA vendors to formulate a proposed plan of action.

The purpose of the Open Meeting is to present the findings and recommendations, and to obtain input from the industry on proposed solutions which would steer this new initiative forward to solve the problems mentioned above.

Silicon Design Chain Power Management Collaboration Results

Thursday, June 16 8:30 am Ballroom D

Industry leaders Applied Materials, ARM, Cadence, and Taiwan Semiconductor Manufacturing Corporation (TSMC), working together through the Silicon Design Chain Initiative, will discuss how their 90nm test chip project resulted in a new, silicon-validated power management approach that can reduce overall chip power consumption by 40%. This approach will enable a broad range of designers to apply sophisticated low-power design techniques to complex SoCs. It is expected that power will be a concern for nearly all designs at 90nm and below.

Additional Meetings

SIGDA Ph.D. Forum / Member Meeting

Tuesday, June 14 **6:30 pm - 8:00 pm** Rm: **204BC**

SIGDA invites you to attend our annual PhD Forum and Member Meeting. SIGDA members are invited, as we are all members of the EDA Community. We will begin with a brief presentation on SIGDA's programs, but the main focus of the meeting will be the Ph.D. Forum. Aimed at strengthening ties between academia and industry, students will present posters and discuss their Ph.D. dissertation research with interested attendees. The Ph.D. Forum gives the students feedback on their research, and gives the EDA community a preview of work in process. Also, light refreshments will be served at 7:00 pm. For more information, see http://www.sigda.org/programs.php.

Third Annual Hacks & Flacks: Emerging Companies — What Do You Communicate, to Whom, and When?

Wednesday, June 15 **3:00 pm - 4:30 pm** Rm: **204A**

Deciding when to communicate with various audiences, what to say, and who to say it to – every emerging company faces these issues when considering company and product launches. Please join us for a lively discussion among venture capitalists, EDA company board members, entrepreneurs, and PR and marketing professionals. Panelists will outline their best tips and pet peeves for communication programs."

Birds-of-a-Feather (BOF) Meetings

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather". All BOF meetings are held at the Anaheim Convention Center, Wednesday, June 15, 6:30 pm – 8:00 pm. DAC will facilitate common interest group meetings to discuss DA related topics. To arrange a BOF meeting sign up at the Information Desk located in Lobby B. A room will only be assigned if ten or more people sign up. An LCD projector and screen will be provided. Check DACnet and the Birds-of-a-Feather board at the Information Desk.

CANDE Meeting (BOF)

Wednesday, June 15 **6:30 pm - 8:00 pm** Rm: **303C**

CANDE is the Computer Aided Design Technical Committee of the IEEE Circuits and Systems Society. It is the sponsoring committee from CASS for both ICCAD and DAC. CANDE brings design automation professionals together to build relationships, and to sponsor a workshop and initiatives that improve the CAD/EDA industry. Please visit the CANDE website: (http://www.ics.uci.edu/~rgupta/cande/) for more information.

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Lee Wood
MP Associates, Inc.
Boulder, CO

Exhibitor Liaison Committee/Student Design Contest Judges

Exhibitor Liaison Committee

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Wilsonville, OR

Donna Castillo
Cadence Design Systems, Inc.
San Jose, CA

Ric Chope
Cadence Design Systems, Inc.
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Steve Pollock
Beach Solutions Inc.
San Jose, CA

Dave Reed
Blaze DFM, Inc.
Los Altos, CA

Lee Wood
MP Associates, Inc.
Boulder, CO

DAC/ISSCC Student Design Contest

DAC/ISSCC SDC Co-Chair
David Greenhill
Sun Microsystems, Inc.
Sunnyvale, CA

DAC/ISSCC SDC Co-Chair
Alan Mantooth
Univ. of Arkansas
Fayetteville, AK

DAC/ISSCC SDC Judges

Farrokh Ayazi
Georgia Tech
Atlanta, GA

Claude Gauthier
ATI Research
Cupertino, CA

James Goodman
ATI Technologies, Inc.
Markham, ON

Yatin Hoskote
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Hillsboro, OR

William B. Kuhn
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St. Louis, MO

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