44TH DESIGN AUTOMATION CONFERENCE

Only DAC offers:

- A robust technical program covering the latest research, developments and trends in electronic design, ranging from management practices to products, methodologies and technologies.
- Worldwide attendance from developers, designers, researchers, academics, managers and engineers from leading electronics companies and universities.
- A vibrant exhibition with 240 companies displaying products, technologies and services for the electronic design industry.

San Diego Convention Center • San Diego, California • June 4-8, 2007

ADVANCE PROGRAM

www.dac.com

Sponsored by:

In Technical Cooperation with:

41 DAC SAN DIEGO, CA JUNE 4-8, 2007

DAC: Where The Electronic Design Community Meets…

Dear Colleague:

Soon, thousands of us will converge in San Diego to attend the Design Automation Conference, the largest and most prestigious annual event focused on the design of electronic circuits and systems.

Who are we? We are the executives, managers, developers, designers, academics, journalists, venture capitalists, and others who make our industries and research groups the innovative, exciting, and productive drivers for the creation of electronic systems.

We will learn about the latest in design tools and methodologies for verification and test, design for manufacturing, IP, design libraries, RF/wireless, analog and mixed-signal designs, embedded software in SoCs, and other effects in today's designs. DAC is the place for the electronic design community to meet with:

- friends and renew acquaintances;
- colleagues and learn about the latest advances in tools, methodologies, fabrication, and test;
- vendors and learn about the latest product offerings;
- other designers and find out how they are using these tools to develop the next generation of …

This year, we have 240 exhibitors, 201 technical presentations (including 8 on "Wild And Crazy Ideas"), plus 8 technical program panels, 18 pavilion panels, 7 full day tutorials, 6 hands-on tutorials, 7 workshops, and various co-located events.

Of particular interest to many of us will be the Automotive Theme, which highlights design challenges that stem from embedding electronic systems in engine control, driver interfaces, communications, entertainment, navigation, and safety critical systems in our automobiles. DAC will also feature a special Executive Management Seminar with management guru and best-selling author Geoffrey Moore, on the topic of managing innovation in our industry.

We finish the week with a tribute to the legacy of A. Richard Newton, Professor and Dean of the College of Engineering at the University of California, Berkeley, with a Thursday keynote by Jan Rabaey, the Donald O. Pederson Distinguished Professor at the University of California at Berkeley.

For more detailed conference information, visit us online at www.dac.com.

Please join us for an informative and inspiring week.

Best regards,
Steve Levitan
General Chair, 44th DAC

Co-Located Conferences	The 44th Design Automation Conference Week in Review					
	Sunday, June 3	Monday, June 4	Tuesday, June 5	Wednesday, June 6	Thursday, June 7	Friday, June 8
• **IWLS** May 30 - June 1, *San Diego, CA* • **MSE 2007** June 2-4, *San Diego, CA*	• **Four Workshops**	• **FREE Monday Exhibits** • **Full-Day Tutorials** • **Hands-on Tutorials** • **Workshops** • **Keynote Address** • **Happy Hour on the Exhibit Floor**	• **General Session** • **Keynote Address** • **Technical Sessions** • **Management Seminar** • **Hands-on Tutorial** • **Exhibits**	• **Technical Sessions** • **Hands-on Tutorials** • **Automotive Theme Sessions** • **Exhibits** • **DAC Party**	• **Technical Sessions** • **Best Paper Awards** • **Keynote Address** • **Hands-on Tutorial** • **Exhibits**	• **Five Full-Day Tutorials**

Networking Opportunities and Social Activities

Be sure to attend these DAC functions!

- ✷ EDA Consortium Executive Reception, Sunday, 5:00pm - 7:00pm
- ✷ Exhibit Floor Happy Hour on Monday, 5:00pm - 6:00pm
- ✷ IEEE CEDA Distinguished Speaker Lecture, Monday, 6:00pm - 8:00pm
- ✷ SIGDA Ph.D Forum and Member Meeting, Tuesday, 6:30pm - 8:00pm
- ✷ Management Seminar on Tuesday, 10:30am - 6:45pm
- ✷ DAC Wednesday Night Party, 7:00pm - 10:00pm. Enjoy great food, drinks and entertainment.
- ✷ Mass Book Signing, Thursday, 11:00am - 12:30pm
- ✷ The DAC Pavilion in Booth 6360 on the exhibit floor – there's always something going on!
- ✷ Keynote Addresses on Monday, Tuesday and Thursday

DAC Technical Session Highlights...

This year's technical program consists of 161 selected papers out of 713 submissions, supplemented by 8 special sessions, 7 tutorials, 8 panels and 18 pavilion panels. The result is an exciting program, targeted to design engineers, management, developers and researchers, that showcases the latest advances in the field of electronic design automation.

The technical theme for this year's DAC is **automotive electronics**; an all-day track on Wednesday includes a special session, invited talks, a panel, and regular papers. Modern automobiles have an incredible array of electronic systems: engine management, satellite navigation, adaptive cruise control and many more. The increasing trend in automotive electronics shows few signs of abating. It has been estimated that electronics will account for as much as 40% of a car's bill-of-materials by the end of this decade. The modern car can now truly be described as a "networked computing platform," and the theme will highlight this issue in the context of electronic design automation.

The program this year includes a new **WACI** (Wild and Crazy Ideas) session, presenting early expositions of non-incremental ideas. The papers in this session encourage out-of-the-box thinking and are designed to promote discussions among attendees during and after the session.

The technical sessions are divided into eleven tracks: Analog/Mixed-Signal/RF and Simulation, Automotive Electronics, Business, DFM and the Manufacturing Interface, Interconnect and Reliability, Low Power Design, New and Emerging Technologies, Physical Design, Synthesis and FPGA, System Level and Embedded Design, and Verification and Test.

A major theme this year includes a strong focal point built around **system-level design**, including system-level communication issues aimed at designing the communication infrastructure of complex systems-on-chip, sessions that highlight industrial applications of ESL methods, MPSoC design, transaction level modeling, and 1000 core chips. Sessions in the area of **embedded systems** present the latest in embedded hardware and software design methods.

The **business track** is driven by an all-day track on Tuesday, beginning with a morning keynote, and continuing with an all-day **management seminar** presented by a group of luminaries: Geoffrey Moore, Raul Camposano and Jim Smith.

Design for manufacturability issues are prominent throughout the program, continuing a trend that has been active for several years now. In addition, there are sessions on process-aware physical design, statistical timing analysis, bridging the gap with silicon, and modeling the impact of technology on design. These are supplemented by special sessions on silicon measurement, and the design-manufacturing interface.

Low power is a prominent design consideration, and several sessions in the technical program focus on issues in this area. This year's selection of papers on power analysis and low power design covers a broad range of topics of wide interest for practical applications and workflows, with sessions dedicated to issues related to leakage power and implications of design variability on full-chip leakage power, on circuit-level approaches for low power design, and on tools and methodologies of interest to system-level design.

Another strong component of the program is in the area of **verification**. This year's program includes some outstanding papers on improving the verification process, ranging from theoretical results on the core computational engines of verification tools to practical, "best practice" case studies on the successful use of cutting-edge verification methodologies.

The technical paper presentations on Tuesday through Thursday are complemented by 7 **tutorial** presentations on Monday and Friday. These are presented by experts in the field, and cover themes such as DFM and variability, system level design, formal verification, reliability under soft errors, low power design, and power delivery concerns for die and package design. The 6 **hands-on tutorials** are in the area of DFM.

An array of **panels** spread throughout the program allow for free-form discussions headed by luminaries in the field, addressing emerging and important areas in the field of EDA. The panels cover topics such as EDA megatrends under shortening consumer cycles, handoffs between design and manufacturing, early power-aware design, transaction-level modeling, IP issues, multicore design, and challenges in functional verification. **Pavilion panels** on the exhibit floor lay the basis for more free-flowing and informal discussions. Topics of this year's panels include trends in EDA, managing mixed-signal designs, DFM, system-level wireless design, anticipating the next killer app, and many more.

44th Design Automation Conference®

Sunday, June 3

Workshops

- **4th UML for SoC Design Workshop** - 9:00am - 5:30pm
- **Low Power Coalition Workshop - Standards for Low Power Design Intent** - 12:30pm - 3:30pm
- **Design and Verification of Low Power ICs** - 4:00pm - 7:00pm
- **Hardware Dependent Software (HdS)** - 1:00pm - 7:30pm

EDA Consortium Executive Reception at the San Diego Marriott Hotel and Marina 5:00pm - 7:00pm

Monday, June 4

Free Monday Exhibit Hours 9:00am - 6:00pm

	Rm: 6C	Rm: 6D	Rm: 11A	Rm: 6A		
9:00	**Tutorial 1** Anatomy of Variability and Making of "Variation Tolerance" Vaccine in Nanometer Technologies	**Tutorial 2** System Design for Multimedia Applications - Challenges, Design Methods and Recent Developments	**Hands-on Tutorial** Standard Cell Library and Hard IP Design *Blaze DFM, Inc. Ponte Solutions*		Workshop for Women in Design Automation 9:00am – 1:45pm • Room 8	Introduction to Chips and EDA for a Non-Technical Audience 10:00am - 12:00pm • Room 9
10:00						
12:00	**Lunch** (Rm: 1AB)	**Lunch** (Rm: 1AB)				
1:00	**Tutorial 1 (cont.)** Anatomy of Variability and Making of "Variation Tolerance" Vaccine in Nanometer Technologies	**Tutorial 2 (cont.)** System Design for Multimedia Applications - Challenges, Design Methods and Recent Developments	**Hands-on Tutorial** Design for Manufacturing Variability with Confidence *ClearShape Technologies Cadence Design Systems, Inc. Texas Instruments Inc., UMC*	3rd Integrated Design Systems Workshop: Models for Design and Manufacturing - How Modeling Challenges are Touching Every Aspect of IC Design 12:00pm - 5:00pm	**Monday Keynote** ***Designing a New Automotive DNA*** **Lawrence D. Burns** - *Vice President of Research & Development and Strategic Planning, General Motors Corp.* 2:00pm - 3:00pm • Ballroom 20ABC	
2:00						
5:00						

DAC Pavilion

Booth #6360

- Gary Smith on EDA: Trends & What's Hot at DAC? **9:30am - 10:30am**
- EDA Exit Strategies: What's Next **10:45am - 11:45pm**
- Student Design Contest Award Presentations **12:00pm - 1:00pm**
- Hogan's Heroes: What We Hear and See in Optimized Timing and Power in 2007 **2:00pm - 3:00pm**
- Just Who is Providing the IP? **3:15pm - 4:00pm**
- Anticipating the Next Killer App: Is There an iPhone in Your Future? **4:15pm - 5:00pm**

IEEE Council on EDA's Distinguished Speaker Lecture and Reception in the Sails Pavilion from 6:00pm - 8:00pm

Tuesday, June 5

Exhibit Hours 9:00am - 6:00pm

General Session and Keynote Speaker — **Ballroom 20ABC**

8:30 to 10:15 — **Perspective of the Future Semiconductor Industry: Challenges and Solutions**
Oh-Hyun Kwon - President, System LSI Division Samsung Semiconductor Business

BREAK 10:15am - 10:30am

	Rm: 6B	Rm: 6C	Rm: 6D	Rm: 6E	Rm: 6F
	Session 1	Session 2	Session 3	Session 4	Session 5
10:30 to 12:00	**SPECIAL SESSION:** Trusted Hardware	**PANEL SESSION:** Mega Trends and EDA 2017	Industrial Application of System Level Methods	Novel Techniques for Interconnect	Formal & Semi-Formal Verification Techniques
	LUNCH 12:00pm - 2:00pm				
	Session 6	Session 7	Session 8	Session 9	Session 10
2:00 to 4:00	Leakage Power Analysis & Optimization	**PANEL SESSION:** Making Manufacturing Work for You	Energy & Performance Issues in On-Chip Communication Networks	Circuit Simulation	Signal & Power Delivery Integrity
	BREAK 4:00pm - 4:30pm				
	Session 11	Session 12	Session 13	Session 14	Session 15
4:30 to 6:30	**SPECIAL SESSION:** Functional Verification of ESL Models	**PANEL SESSION:** Early Power-Aware Design and Validation	Memories in Embedded Systems	Statistical Techniques for Timing Analysis and Design	**SPECIAL SESSION:** Wild And Crazy Ideas

HOTs

Deploying Statistical Timing – from Characterization to Analysis and Optimization *Atoss Design Automation/Cadence Design Systems, Inc.*

DAC Pavilion

Booth #6360

- Career Advancement for Technologists: An Interview with the Marie R. Pistilli Woman in EDA Award Winner **10:15am - 11:00am**
- Managing Mixed-Signal Designs: What's Working? What's Missing? **11:15am - 12:00pm**
- Deploying Formal: When and Where? **2:00pm - 3:00pm**
- ESL for Wireless **3:15pm - 4:15pm**
- To Be or Not To Be Compliant: That is the Question **4:30pm - 5:30pm**

SIGDA Ph.D. Forum and Member Meeting in the Sails Pavilion from 6:30pm - 8:00pm

Wednesday, June 6

Exhibit Hours 9:00am - 6:00pm

	Rm: 6B	Rm: 6C	Rm: 6E	Rm: 6F	Rm: 6A
	Session 16	Session 17	Session 18	Session 19	Session 20
8:30 to 10:00	Distributed Computing: Automotive Network Design & Analysis	Emerging Nanoscale Hybrid Circuits & Architectures	Physical Implementation of FPGAs	Process Aware Physical Design	Reliable Design & CAD Solutions for Circuit Aging
	BREAK 10:00am - 10:30am				
	Session 21	Session 22	Session 23	Session 24	Session 25
10:30 to 12:00	**INVITED SESSION:** Silicon, Safety and Self-Driving Cars	**SPECIAL SESSION:** Silicon Measurement Correlation to Reliability	Optimizing Arithmetic & Communication	Analog & RF Simulation	**PANEL SESSION:** TLM: Crossing Over from Buzz to Adoption
	LUNCH 12:00pm - 2:00pm				
	Session 26	Session 27	Session 28	Session 29	Session 30
2:00 to 4:00	**PANEL SESSION:** Electronics: The New Differential in the Automotive Industry	Modern Placement Techniques	Advances in Embedded Hardware Design	Bridging the Gap with Silicon	Practical Solutions for Power-Aware Testing
	BREAK 4:00pm - 4:30pm				
	Session 31	Session 32	Session 33	Session 34	Session 35
4:30 to 6:30	**SPECIAL SESSION:** Virtual Automotive Platforms	**SPECIAL SESSION:** The Future of Interconnects	Advances in Decision Procedures	3D IC & Package Design Issues	**PANEL SESSION:** Corezilla: Build and Tame the Multicore Beast

HOTs

Approaching Yield in the Nanometer Age: *Mentor Graphics Corp./ Chartered Semiconductor Manufacturing/ Sierra Design Automation, Inc./AMI Ltd.*

Manufacturing Aware Optimization *Blaze DFM, Inc./Taiwan Semiconductor Manufacturing Company, Ltd.*

DAC Pavilion

Booth #6360

- The Urban Challenge: Paving the Way for Driverless Automobiles **9:30am - 10:15am**
- Improving Automotive Competitiveness: New Methods and Tools For Embedded Design **11:00am - 12:00pm**
- Electronics: The Key to Disruption of Automobile Powertrain Technology **1:00pm - 1:45pm**
- DFM: Prevention or Cure **2:00pm - 3:00pm**
- On a Crash Course: Validation and Testing of Automotive Software **3:15pm - 4:15pm**
- The One Ton Mobile Platform: Where is it Taking Us? **4:30pm - 5:30pm**

Wednesday Night Party • 7:00pm - 10:00pm • Sails Terrace, San Diego Convention Center

Presenters will be available in Room 1AB for additional 20-minute question-and-answer periods after each session. ☐ **Of special interest to designers**

Session Tracks: **Analog/Mixed-Signal/RF and Simulation** **Business** **DFM and the Manufacturing Interface** **Interconnect and Reliability** **Low Power Design** **Automotive Theme** **New and Emerging Technologies** **Physical Design** **Synthesis and FPGA** **System Level and Embedded** **Verification and Test**

San Diego, CA, June 4 - 8, 2007

Thursday, June 7

Exhibit Hours 9:00am - 1:00pm

	Rm: 6B	Rm: 6C	Rm: 6D	Rm: 6E	Rm: 6F	Rm: 6A
	Session 36	Session 37	Session 38	Session 39	Session 40	Session 41
9:00 to 11:00	**SPECIAL SESSION:** Synthetic Biology	Programming & Scheduling Embedded Systems	Emerging Test Solutions	Circuit Level Power Analysis & Low Power Design	Parameter Tuning in System Architecture Exploration	**PANEL SESSION:** Verification Coverage: When is Enough Enough?
	LUNCH 11:00am - 12:30pm					
12:30 to 1:45	**Best Paper Award Presentations and Keynote Speaker** — Ballroom 20ABC **Design without Borders – A Tribute to the Legacy of A. Richard Newton** *Jan M. Rabaey* - Donald O. Pederson Distinguished Professor, University of California, Berkeley					
	Session 42	Session 43	Session 44	Session 45	Session 46	Session 47
2:00 to 4:00	**SPECIAL SESSION:** Thousand-Core Chips	Communication-Based Resource Allocation	Embedded Processor & MPSoC Design	Modeling Technology Impact	Technology Mapping & Physical Synthesis	System-Level Power Management & Analysis
	BREAK 4:00pm - 4:30pm					
	Session 48	Session 49	Session 50	Session 51	Session 52	Session 53
4:30 to 6:00	Dynamic Verification of Processors & Processor-Based Designs	FPGA Tools & Methodologies	Mixed-Signal Modeling, Methodology & Synthesis	Design Methods & Manufacturability Solutions for Emerging Technologies	High-Performance Synchronization Techniques	**PANEL SESSION:** IP Exchange

Hands On Tutorial

Timing Closure: Requirements for Variation Aware Design
Extreme DA Corp./ Texas Instruments Inc./ PDF Solutions/UMC
9:00am - 12:00pm

DAC Pavilion

Booth #6360

P-cells or Free Cells
10:15am - 11:15am

Friday, June 8

Full-Day Tutorials

	Rm: 6F	Rm: 6A	Rm: 6C	Rm: 6D	Rm: 6E
9:00 to 5:00	**TUTORIAL 3** Formal Assertion Based Verification in an Industrial Setting	**TUTORIAL 4** Design and Analysis of High-Performance Package and Die Power Delivery Networks	**TUTORIAL 5** Soft Errors: Technology Trends, System Effects and Design Techniques	**TUTORIAL 6** How Design Meets Yield in the Fab	**TUTORIAL 7** Circuit and CAD Techniques for Low Power Design

Keynote, Monday, June 4 • 2:00pm - 3:00pm • Ballroom 20ABC

Designing a New Automotive DNA

Lawrence D. Burns

Vice President of Research & Development and Strategic Planning, General Motors Corp.

The automotive industry stands on the threshold of a new opportunity – an opportunity that stems from the reinvention of the automobile using a new DNA that exchanges the internal combustion engine, petroleum, and mechanical linkages for fuel cells and batteries, hydrogen and electricity, and electronic systems and controls.

Electrically driven vehicles and the introduction of advanced electronics and connected vehicle technologies will revolutionize how our vehicles operate, how we interact with them, and how they communicate with each other and the outside world. These new technologies will also, importantly, dramatically change how automobiles are designed and built.

In this talk, Dr. Burns will highlight why the new automotive DNA will be paradigm shifting for the industry and address the design challenges and opportunities presented by the requirement for new electrical and electronics-based architectures, systems, and software for our vehicles.

Keynote, Tuesday, June 5 • 8:30am - 10:15am • Ballroom 20ABC

Perspective of the Future Semiconductor Industry: Challenges and Solutions

Oh-Hyun Kwon

President, System LSI Division, Samsung Semiconductor Business

The semiconductor industry currently faces serious challenges and changes on both the business and technology fronts. The business environment is becoming more difficult. The huge investment required for new fabrication facilities is forcing many IDMs (Integrated Device Manufacturer) to change their business model to either fablite or fabless. The significant costs to develop the next generation process technologies are necessitating joint development between various companies. Furthermore, due to severe competition in the mobile and digital consumer markets, low chip prices and short time-to-market are both essential for survival. To satisfy these market requirements, heavy R&D expenses and resources are needed. However, its return on investment is becoming marginal and even uncertain. To overcome this difficult situation, the industry is experiencing consolidation of once proudly independent companies. On the technical side, controlling chip yield, power consumption and design complexity have become extremely difficult in the nano-technology era.

This talk will present a perspective on how the semiconductor industry must respond to these challenges by developing new markets, new products, and new technologies. The solutions will come from (i) collaborations with key customers for new markets and products, as well as, with key partners for new technologies, and (ii) technology breakthroughs with innovative ideas, such as 3-D package, fusion technologies (OneDRAM™, OneNAND™), variation-tolerant designs, and low leakage devices. These approaches can lead to lower chip costs and relieve physical uncertainty problems.

Keynote, Thursday, June 7 • 12:30pm - 1:45pm • Ballroom 20ABC

Design without Borders – A Tribute to the Legacy of A. Richard Newton

Jan M. Rabaey

Donald O. Pederson Distinguished Professor, Director Gigascale Systems Research Center (GSRC), Scientific Co-director BWRC, University of California, Berkeley

Electrical engineers have learned how to build amazingly complex systems by assembling transistors, wires, and passive components into intricate networks. While solidly founded in semiconductor physics, pure engineering has made possible the design of multi-billion transistor chips in a repetitive, reliable and cost-effective way. A comprehensive "design methodology" was developed based on modularization, hierarchy and abstraction.

Today this story is repeating itself. Physicists, chemists and biologists are exploring entirely different components such as molecules, atoms, and enzymes. Systems built from those will most probably impact our lives and society in a profound way. Outcomes will influence the ways we build mechanical structures, do computing, make drugs, generate energy and take care of our environment.

Yet, while the basic components are dramatically different from our silicon devices, the basic strategy for building very complex systems from them remains unchanged. The art of design, as was developed in the silicon era, is just as applicable to these nano- or bio-constructions. Design methodology is a legacy that will live long after Moore's Law has come to a halt. To quote Richard, "The Future is BDA (Bio Design Automation)".

Management Seminar – Tuesday, June 5 • 10:30am - 6:45pm • Rm: 6A

Innovation or Extinction - The Choice Is Yours!

Innovation is critical for the long term success of any industry. The electronics, semiconductor and the electronic design automation industry have pursued such a strategy successfully for several decades. This was made possible by technological advances in processing, innovative design flows and methodologies, and continued improvement in design tools. However limitations in manufacturing, increasing design complexity and design costs have started to decelerate the possible gains obtained along these directions. In the recent past, growth in these industries has slowed and it is perceived by many that these industries need to do more to capture growth. In addition, the twin forces of globalization and technology have led to changes that impact business dramatically. Globalization has enabled vast and eager talent pools to participate in business at low cost. Technology has lowered the barriers to market entry and leveled the playing field in many situations. In the current scenario, innovation is not only key but perhaps the only method to differentiate your business from that of your competitors. Registration for this event includes: entrance to the Keynotes, entrance to the Exhibition, a copy of the book "Dealing with Darwin", coffee breaks, and the Productivity Impact Luncheon (produced by EDA Consortium and FSA).

This seminar is designed for middle and senior management who wish to consider innovation as a part of strategic planning. The seminar is structured in three parts:

1. **Innovative Fundamentals**, Speaker: Geoffrey Moore - TCG Advisors, San Mateo, CA
2. **Innovation in the Semiconductor and Electronic Design Automation Markets**, Speaker: Raul Camposano - Xoomsys, Inc., Cupertino, CA
3. **Investing for Innovation**, Speaker: Jim Smith - Mohr Davidow Ventures, Menlo Park, CA

Productivity Impact Luncheon - Changing the Dialogue Between Engineers & Management

Produced by the EDA Consortium and FSA
Date: Tuesday, June 5, Noon to 1:30 pm
Admission: $50 early registration, $60 after May 7

Speakers: Kathryn Kranen, Brian Fuller, Lisa Tafoya

Automotive Electronics at DAC

There has been an explosion of electronic content in automobiles recently. For 2007, the automotive semiconductor market is expected to be $19 billion (Gartner/Dataquest) and by 2010 it is expected that 40% of the bill of materials in cars will be for electronics. The Automotive theme addresses how design tools and methodologies will be used to support the tremendous design requirements for automotive electronics and what role EDA will play.

Attendees will have a chance to "look under the hood" of two cars that represent the future of automotive electronics: the GM Sequel Hydrogen car and the Wrightspeed X1 prototype electric car with a few lucky attendees getting a chance to test drive the Sequel Hydrogen car.

Technical presentations from experts representing leading electronics and automotive suppliers include a Keynote address by Larry Burns, Vice President Research & Development and Strategic Planning for General Motors. Other technical presentations include sessions on Automotive Electronics as a major product differentiator, the network protocols for distributed architectures, safety issues including robust design, and the validating and testing of automotive software. Additional sessions address the use of virtual platforms to reduce MCU count, embedded systems design as a competitive advantage, and how the changing requirements of the automotive market will affect the R&D agendas of semiconductor and EDA companies.

DAC Pavilion on the Exhibit Floor Booth #6360

DAC has an exciting line-up of panels and presentations in the DAC Pavilion on the exhibit floor. The DAC Pavilion sessions are open to all attendees and feature provocative technical, business, and strategy discussions.

DAC PAVILION	DAY	TIME
Gary Smith on EDA: Trends & What's Hot at DAC?	Mon., June 4	9:30am - 10:30am
EDA Exit Strategies: What's Next?	Mon., June 4	10:45am - 11:45am
Student Design Contest Award Presentations	Mon., June 4	12:00pm - 1:00pm
Hogan's Heroes: What We Hear and See in Optimized Timing and Power in 2007	Mon., June 4	2:00pm - 3:00pm
Just Who is Providing the IP?	Mon., June 4	3:15pm - 4:00pm
Anticipating the Next Killer App: Is There an iPhone in Your Future?	Mon., June 4	4:15pm - 5:00pm
Career Advancement for Technologists: An Interview with the Marie R. Pistilli Woman in EDA Award Winner	Tues., June 5	10:15am - 11:00am
Managing Mixed-Signal Designs: What's Working? What's Missing?	Tues., June 5	11:15am - 12:00pm
Deploying Formal: When and Where?	Tues., June 5	2:00pm - 3:00pm
ESL for Wireless	Tues., June 5	3:15pm - 4:15pm
To Be or Not To Be Compliant: That is the Question	Tues., June 5	4:30pm - 5:30pm
The Urban Challenge: Paving the Way for Driverless Automobiles	Wed., June 6	9:30am - 10:15am
Improving Automotive Competitiveness: New Methods and Tools for Embedded Design	Wed., June 6	11:00am - 12:00pm
Electronics: The Key to Disruption of Automobile Powertrain Technology	Wed., June 6	1:00pm - 1:45pm
DFM: Prevention or Cure	Wed., June 6	2:00pm - 3:00pm
On a Crash Course: Validation and Testing of Automotive Software	Wed., June 6	3:15pm - 4:15pm
The One Ton Mobile Platform: Where is it Taking Us?	Wed., June 6	4:30pm - 5:30pm
P-cells or Free Cells	Thur., June 7	10:15am - 11:15am

44th DAC Workshops

4th UML for SoC Design Workshop
Sunday, June 3, 9:00am - 5:30pm

Low Power Coalition Workshop - Standards for Low Power Design Intent
Sunday, June 3, 12:30pm - 3:30pm

Design and Verification of Low Power ICs
Sunday, June 3, 4:00pm - 7:00pm

Hardware Dependent Software (HdS)
Sunday, June 3, 1:00pm - 7:30pm

Introduction to Chips and EDA for a Non-Technical Audience
Monday, June 4, 10:00am - 12:00pm

Workshop for Women in Design Automation - *Managing Your Career*
Monday, June 4, 9:00am - 1:45pm

3rd Integrated Design Systems Workshop
Monday, June 4, 12:00pm - 5:00pm

Exhibition

The 44th DAC Exhibition is located on the main floor of the San Diego Convention Center

The 44th exhibit floor is bursting with 240 vendors offering products for all phases of the electronic design process including EDA tools, IP cores, embedded system and system-level tools, as well as silicon vendors and design-for-manufacturing companies. The DAC show floor features its unique exhibit booth and private suite combination, which gives you the freedom to deeply explore the products on the show floor and find a solution that is right for your design flow. Visit the DAC exhibition and find out how you can improve performance and shorten the time-to-market on your next design.

Attend Free Monday, June 4 , 2007

Exhibit Hours

Monday-Wednesday, June 4-6	**9:00am - 6:00pm**
Thursday, June 7	**9:00am - 1:00pm**

Exhibiting Companies (as of April 27, 2007)

Accelicon Technologies, Inc.
ACE Associated Compiler Experts bv
Advantest Technology Solutions
Agilent Technologies
Aldec, Inc.
Algotronix Ltd.
Altos Design Automation
Analog Bits Inc.
Analog Rails
Anasift Technology, Inc.
Anchor Semiconductor, Inc.
Ansoft Corp.
Apache Design Solutions, Inc.
Applied Simulation Technology
Applied Wave Research, Inc.
Appro International
Arasan Chip Systems
ArchPro Design Automation, Inc.
ARM
Artwork Conversion Software, Inc.
Athena Design Systems
Atoptech
Atrenta Inc.
Attachmate
austriamicrosystems
AutoESL Design Technologies Inc.
Averant, Inc.
Avery Design Systems, Inc.
Axiom Design Automation
Azuro, Inc.
Beach Solutions Ltd.
Berkeley Design Automation, Inc.
Blaze DFM, Inc.
Blue Pearl Software
Bluespec, Inc.
Breker Verification Systems
Brion Technologies
BullDAST s.r.l.
CAD Science, Inc.
Cadence Design Systems, Inc.
Calypto Design Systems
Carbon Design Systems, Inc.
CAST, Inc.
Center for Embedded Computer Systems
Certess Inc.
Chip Estimate Corp.
ChipVision Design Systems
Ciranova, Inc.
Clear Shape Technologies, Inc.
ClioSoft, Inc.
CLK Design Automation, Inc.
CMP
CoFluent Design
CommandCAD, Inc.
Concept Engineering GmbH
Coupling Wave Solutions
CoWare, Inc.
CRC Press - Taylor & Francis
CriticalBlue
DAC Pavilion
Dataram
DATE '08
DeFacTo Technologies
Denali Software, Inc.
Design and Reuse
Dini Group (The)
Dolphin Integration
Doulos
Dynalith Systems Co., Ltd.
EDXACT
Elsevier
EMA Design Automation, Inc.
eMemory Technology Inc.
ENOVIA MatrixOne
Entasys Design, Inc.
Envision Technology
EVE
Evolvable Systems Research Institute, Inc
Extension Media
Extreme DA
Fenix Design Automation
FishTail Design Automation
Flomerics, Inc.
Forte Design Systems
Fortelink Inc.
FSA
FTL Systems, Inc.
Gaisler Research AB
GateRocket, Inc.
Genesys Testware, Inc.
Gidel Inc.
Golden Gate Technology, Inc.
Gradient Design Automation
Handshake Solutions
HARDI Electronics AB
Helic S.A.
Heller Ehrman
Hewlett-Packard Co.
Hummingbird Connectivity - Open Text
IBM Corp.
IC Manage
IEEE Spectrum
IMEC
Imperas, Inc.
Incentia Design Systems, Inc.
Innovative Silicon Inc.
InsideChips.com
Intel Corp.
Intellitech Corp.
InternetCAD.com, Inc.
Interra Systems, Inc.
Jasper Design Automation, Inc.
Javelin Design Automation, Inc.
JEDA Technologies
KETI / IP SoC Support Center
Kilopass Technology, Inc.
Kimotion Technologies Inc.
Knowlent Corp.
Laflin Instigate
Legend Design Technology, Inc.
Library Technologies, Inc.
Liga Systems, Inc.
Lightspeed Logic
LogicVision, Inc.
Lorentz Solution
Lynguent, Inc.
Magillem Design Services
Magma Design Automation, Inc.
Manhattan Routing Inc.
MataiTech LLC
MathWorks, Inc. (The)
McGraw-Hill Professional
Mentor Graphics Corp.
Micro Magic, Inc.
Micrologic Design Automation
Mirabilis Design Inc.
Mixel, Inc.
MOSAID
MOSIS
MunEDA GmbH
MyCAD, Inc.
Nangate
Nannor Technologies, Inc.
Nanovata Design Automation
Nascentric, Inc.
National Instruments Corp.
NEC Informatec Systems, Ltd.
NEC System Technologies, Ltd.
Novas Software, Inc.
Novelics
Nusym Technology, Inc.
Obsidian Software, Inc.
OCP International Partnership
OEA International, Inc.
OneSpin Solutions GmbH
Open iT, Inc.
Optimal Corp.
Orora Design Technologies, Inc.
Pextra
Platform Computing
PLD Applications (PLDA)
Plurality Ltd.
Ponte Solutions, Inc.
Prentice Hall Prof. / Pearson Education
ProDesign Electronic Corp.
Proficient Design, LLC
Prolific, Inc.
Pulsic Ltd.
Pyxis Technology, Inc.
QThink
Quik-Pak
Real Intent, Inc.
Reed Business Information
Rio Design Automation
Runtime Design Automation
Sagantec
Samtec, Inc.
Sandwork Design Inc.
Saratoga Data Systems, Inc.
Sarnoff Europe
Semifore, Inc.
Sequence Design, Inc.
Shearwater Group, Inc. (The)
Si2
Sierra Design Automation, Inc.
SIGDA/DAC University Booth
Sigrity, Inc.
Silicon Canvas Inc.
Silicon Design Solutions
Silicon Frontline Technology
Silicon Hive
Silicon Image
Silicon Navigator
Silistix, Inc.
Simucad Design Automation Inc.
SoftJin Technologies Pvt. Ltd.
Solido Design Automation Inc.
Space Codesign
Springer
StarNet Communications
Swati Design Automation, Inc.
Synchronicit
SynCira
Synfora, Inc.
Synopsys, Inc.
Synopsys, Inc. - Partner Booth
Synplicity, Inc.
SynTest Technologies, Inc.
Takumi Technology Corp.
Tanner EDA
Target Compiler Technologies
Tata Elxsi
TeamEDA, Inc.
TechForce, Inc.
Teklatech
Time To Market Inc.
TOOL Corp.
Triad Semiconductor, Inc.
True Circuits, Inc.
TSMC
TSSI - Test Systems Strategies, Inc.
Tuscany Design Automation, Inc.
UMC
UniqueICs, LLC
Uniquify, Inc.
VaST Systems Technology
VeriEZ Solutions, Inc.
Verific Design Automation
Veritools, Inc.
ViASIC Inc.
Virage Logic Corp.
Xoomsys
XYALIS
Z Circuit Automation, Inc.
Zeland Software, Inc.

Detailed conference and exhibition information is now available on-line: www.dac.com. *Register today!*

QUESTIONS? call 800-321-4573

REGISTER TODAY! Register on-line through June 8, 2007

Registration Options:

- **Register on-line** Internet registration open through June 8. Mail/Fax registrations not accepted after May 25.
- **Free Monday Exhibit-Only** to visit the Exhibition, on *Monday only*, June 4.
- **Keynote Addresses** on Monday, Tuesday, and Thursday are open to all.
- **Exhibit-Only** allows admittance to the Exhibition, Monday through Thursday.
- **Full Conference** includes all three days of the Technical Conference, access to the Exhibition Monday through Thursday, and the 44 Years of DAC DVD Proceedings, plus a ticket to the Wednesday Night Party.
- **Student** includes all three days of the Technical Conference, access to the Exhibition Monday through Thursday, and the 44 Years of DAC DVD Proceedings, plus a ticket to the Wednesday Night Party.
- **One-/Two-Day Registration** includes the day(s) you select for the Technical Conference, Monday through Thursday of the Exhibition, and the 44 Years of DAC DVD Proceedings.
- **Full-Day Tutorials** are offered on Monday, June 4, and Friday, June 8. You must register for at least one day of the Technical Conference to attend tutorials. Tutorial registration fee includes continental breakfast, lunch, coffee breaks, and tutorial notes.
- **Hands-on Tutorials** are three-hour tutorials utilizing hands-on software tools from DAC exhibitors. Attendees must register for a minimum of an Exhibit-Only registration to be eligible to attend Hands-on Tutorials. Due to the proprietary nature of the discussions, presenting companies reserve the right to refuse access to employees or contractors of competitors. Space is limited.
- **Management Seminar:** Cost: $350, No Conference Registration required. Registration for this event includes: entrance to the Keynotes, entrance to the Exhibition, a copy of the book "*Dealing with Darwin*", coffee breaks, and the Productivity Impact Luncheon.

CONFERENCE	**Received by May 7, 2007**	**After May 7, 2007, or at the conference**
Member ACM or IEEE	$380	$475
Non-Member	$495	$620
Students with ACM or IEEE membership	$165	$165
One-Day Only *(Tues., Wed., Thur.)*	$255	$255
Two-Day Only *(Tues., Wed., Thur.)*	$455	$455
EXHIBIT-ONLY		
Free Monday	Free	Free
Exhibit-Only (access all days)	$65	$65

TUTORIALS	**member ACM or IEEE**	**non-member**	**student**
Full-Day Tutorials	$300 (per tutorial)	$375 (per tutorial)	$125 (per tutorial)
Hands-on Tutorials	$75 (per tutorial)	$75 (per tutorial)	$75 (per tutorial)
MANAGEMENT SEMINAR:	**$350**	**$350**	

Two ways to save $! Register before May 7, 2007 and save 20% on your registration.

IEEE and ACM members save an additional 25%. Not yet a member? Find out how to join on the DAC web site.

WORKSHOPS

4th UML for SoC Design - $100 (member) - $150 (non-member)
Low Power Coalition Workshop - Standards for Low Power Design Intent - $75 (member), $100 (non-member)
Design and Verification of Low Power ICs - $75 (member), $100 (non-member)
Hardware Dependent Software (HdS) - $100 (member), $150 (non-member)
Introduction to Chips and EDA for a Non-Technical Audience - $10
Workshop for Women in Design Automation – ***Managing Your Career*** $50 (member) - $75 (non-member)
3rd Integrated Design Systems Workshop - $50 (member) - $75 (non-member)

Visit the DAC web site for on-line registration, complete conference and exhibit details, travel and hotel reservations, and San Diego information at www.dac.com.

Refund Policy: Written requests for cancellations must be received on or before **May 7, 2007**, and are subject to a $25 processing fee. Cancellations after May 7, 2007, will NOT be honored and all registration fees will be forfeited. **No faxed or mailed registration will be accepted after May 25, 2007, in the DAC office.**

TELEPHONE REGISTRATIONS ARE NOT ACCEPTED! Faxed or mailed registrations without payment will be discarded

44th Design Automation Conference®
5405 Spine Rd., Ste. 102
Boulder, CO 80301 USA
800-321-4573
Intl: +1-303-530-4333
Fax: +1-303-530-4334
www.dac.com

FIRST CLASS
U.S. POSTAGE
PAID
BOULDER, CO
PERMIT NO. 537