DESIGN**AUTOMATION**CONFERENCE

Call For Papers

DAC 2008 is seeking papers that deal with design tools, design methods, design techniques, and embedded design in a number of categories described below.

Design Tools papers describe contributions to the research and development of design tools and their supporting algorithms.

Design Methods and Case Studies papers describe innovative methodologies for the design of electronic circuits and systems, as well as creative experiences with design automation in state-of-the-art design projects.

Design Techniques papers describe the use of design tools and methods from the perspective of a specific design project. They include a brief description of the design and discussion of: methodology, flow, innovative use of tools, the limits of current tools, and what new tool capabilities are required for future designs.

Embedded Systems papers are characterized by mixed hardware and software components with limited resources. Increases in software content introduce new system design issues. Embedded Design papers describe tools, methods, and case studies for applications with specific embedded system content.

Wireless is the theme topic for DAC 2008. Papers that specifically target wireless related design, verification, test and implementation issues will be highlighted at the conference.

1. System-Level Design and Co-Design
- 1.1 System specification, modeling, simulation, and performance analysis
- 1.2 Scheduling, HW-SW partitioning
- 1.3 IP and platform-based design, IP protection
- 1.4 System-on-Chip (SoC) and Multiprocessor SoC (MPSoC)
- 1.5 Application-specific processor design tools

2. System-Level Communication and Networks on Chip
- 2.1 Modeling and performance analysis
- 2.2 Communications-based design
- 2.3 Architectural synthesis, mapping, routing, scheduling
- 2.4 Optimization for energy, fault-tolerance, reliability
- 2.5 Interfacing and software issues
- 2.6 NoC Design methodologies and CAD flows, case studies and prototyping

3. Embedded HW Design and Applications
- 3.1 Case studies of embedded system design
- 3.2 Flows and methods for specific applications and design domains

4. Embedded SW Tools and Design
- 4.1 Retargetable compilation
- 4.2 Memory/cache optimization
- 4.3 Real-time single- and multi-processor scheduling, linking, loading
- 4.4 Real-time operating system

5. Power Analysis and Low-Power Design
- 5.1 System level power design and thermal management
- 5.2 Embedded low-power approaches: partitioning, scheduling, and resource management
- 5.3 High-level power estimation and optimization
- 5.4 Gate-level power analysis and optimization
- 5.5 Device, circuit techniques for low-power design

6. Verification
- 6.1 Functional, transaction-level, RTL, and gate-level modeling and verification of hardware design
- 6.2 Dynamic simulation, equivalence checking, formal (and semi-formal) verification model and property checking
- 6.3 Emulation and hardware simulators or accelerator engines
- 6.4 Modeling languages and related formalisms, verification plan development and implementation
- 6.5 Assertion-based verification, coverage analysis, constrained-random test bench generation

7. High-Level Synthesis
- 7.1 High-level, behavioral, algorithmic, and architectural synthesis, "C" to gates tools and methods
- 7.2 HW-SW interface synthesis, communication and network synthesis
- 7.3 Synthesis of digital circuits above the RTL level
- 7.4 Resource scheduling, allocation, and synthesis

8. Beyond Die-Integration and Package/Hybrid/Board Design
- 8.1 Chip-package-board co-design
- 8.2 System-in-Package, 3D design, stacked devices
- 8.3 Beyond-the-die communication, highspeed I/O, optical communication
- 8.4 Analysis and optimization (signal integrity, physical layout, simulation) beyond the die

9. Logic Synthesis and Circuit Optimization
- 9.1 Combinational, sequential, and asynchronous logic synthesis
- 9.2 Library mapping, cell-based design and optimization
- 9.3 Transistor and gate sizing and resynthesis
- 9.4 Interactions between logic design and layout or physical synthesis

10. Circuit Simulation and Interconnect Analysis
- 10.1 Electrical-level circuit simulation
- 10.2 Model-order reduction methods for linear systems
- 10.3 Interconnect and substrate modeling and extraction
- 10.4 High-frequency and electromagnetic simulation of circuits
- 10.5 Thermal and electrothermal simulation

11. Timing Analysis and Design for Manufacturability
- 11.1 Design for yield, defect tolerance, cost issues, and impacts of DFM
- 11.2 Process technology development, characterization, and modeling
- 11.3 Deterministic static timing analysis and verification
- 11.4 Statistical performance analysis and optimization
- 11.5 Design for resilience under manufacturing variations

12. Physical Design and Manufacturability
- 12.1 Physical floorplanning, partitioning, placement
- 12.2 Buffer insertion, routing, interconnect planning
- 12.3 Physical verification and design rule checking
- 12.4 Automated synthesis of clock networks
- 12.5 Reticle enhancement, lithography related design optimizations

13. Signal Integrity and Design Reliability
- 13.1 Signal integrity, capacitive and inductive crosstalk
- 13.2 Reliability modeling and analysis
- 13.3 Novel clocking and power delivery schemes
- 13.4 Power grid robustness analysis and optimization
- 13.5 Soft-errors and single-event upsets (SEUs)
- 13.6 Thermal Reliability

14. Analog/Mixed-Signal and RF
- 14.1 Analog, mixed-signal, and RF design methodologies
- 14.2 Automated synthesis and macromodeling
- 14.3 Analog, mixed-signal and RF simulation and optimization

15. FPGA Design Tools and Applications
- 15.1 Rapid prototyping
- 15.2 Logical synthesis and physical design techniques for FPGAs
- 15.3 Configurable and reconfigurable computing

16. Testing
- 16.1 Test quality/reliability, current-based test, delay test, low power test
- 16.2 Digital fault modeling, automatic test generation, fault simulation
- 16.3 Digital design-for-test, test data compression, built-in self test
- 16.4 Memory test and repair, FPGA testing
- 16.5 Fault tolerance and on-line testing
- 16.6 Analog/mixed-signal/RF testing, System-in-Package (SiP) testing
- 16.7 Board- and system-level test, System-on-Chip (SoC) testing
- 16.8 Silicon debug, diagnosis, post-silicon design validation

17. New and Emerging Design Technologies, (including but not restricted to)
- 17.1 MEMS, sensors, actuators, imaging devices
- 17.2 Nano-technologies, nano-wires, nano tubes
- 17.3 Quantum computing
- 17.4 Biologically based or biologically inspired systems
- 17.5 New transistor structures and devices, new or radical process technologies

18. Special Theme Topic: Wireless
- 18.1 Emerging technologies for the design, verification, test and implementation of wireless systems
- 18.2 Power-aware and energy-efficient wireless protocols, algorithms and associated design techniques and methodologies
- 18.3 Embedded software design challenges for wireless applications and its impact on ESL design solutions
- 18.4 Promising analog and mixed signal design techniques for wireless systems including but not limited to advanced antenna and RF design solutions

ALL SUBMISSIONS MUST BE MADE ELECTRONICALLY AT THE DAC WEBSITE: WWW.DAC.COM - SUBMISSION SITE OPENS SEPTEMBER 17, 2007

REGULAR PAPERS DUE BEFORE 5pm Mountain Time, Nov. 19, 2007

Regular paper submissions MUST (1) be in PDF format only, (2) contain an abstract of approximately 60 words clearly stating the significant contribution, impact, and results of the submission, (3) be no more than 6 pages (including the abstract, figures, tables, and references), double column, 9pt or 10pt font, and (4) MUST NOT include name(s) or affiliation(s) of the author(s) anywhere on the manuscript or abstract; and any references to the author(s)'s own previous work or affiliations in the bibliographic citations must be in the third person. Format templates are available on the DAC website for your convenience, but are not required. Submissions not adhering to these rules, or those previously published or simultaneously under review by another conference, will be rejected. DAC will work cooperatively with other conferences, symposia and journals in the field to check for double submissions. Additional submission guidelines are available on the DAC website (after September 3, 2007). All regular papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage. Authors of accepted papers must sign a copyright release form for their paper. Accepted papers will be posted on the DAC website after February 25, 2008. Complete author kits will be sent via email by March 7, 2008.

WILD AND CRAZY IDEAS (WACI) SESSION PAPERS DUE BEFORE 5pm Mountain Time, Nov. 19, 2007

WACI submissions should propose, in two pages or less, forward-looking and innovative ideas that are typically less developed than regular papers. **Please see the website for further details.**

SPECIAL SESSION SUBMISSIONS DUE BEFORE 5pm Mountain Time, Nov. 1, 2007

Special session submissions must include descriptions of suggested papers and speakers, and the importance of the special session to the DAC audience. DAC reserves the right to restructure all special sessions. Please see the website for further details.

PANEL and TUTORIAL SUBMISSIONS DUE BEFORE 5pm Mountain Time, Nov. 1, 2007

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure all panel and tutorial proposals. Please see the website for further details.

STUDENT DESIGN CONTEST SUBMISSIONS DUE BEFORE 5pm Mountain Time, Dec. 5, 2007

Students are invited to submit descriptions of original electronic designs, either circuit level or system level. Student Design Contest paper submissions MUST (1) be in PDF format only, (2) contain the title of the project, (3) contain an abstract of approximately 60 words, (4) a complete description of the project, and (5) be no more than 6 pages (including the abstract, maximum of 10 figures/tables and references), double column, 9pt or 10pt font. The submission should clarify the originality, distinguishing features, and measured performance of the design. Three categories of designs - operational, system and conceptual - are eligible for awards. For operational designs, proof-of-implementation is required, while for conceptual designs, complete simulation and test plan is necessary. Designs must have taken place as part of the students' work at the university and must have been completed after June 2006. Submitted designs should not have received awards in other contests. Selected designs will be presented at the conference (and at ISSCC in February 2008). Additional contest rules are available on the DAC website.

WORKSHOPS SUBMISSION SITE OPENS Monday, Sept. 17, 2007, until Friday, Feb. 15, 2008.

DAC invites you to organize a workshop on topics related to design, design methodologies, and design automation. DAC provides the financial and organizational support, including attendee registration, rooms at the conference center and audio visual equipment. Please see the website for further details, or call Kevin Lepine, Conference Manager at +1 303-530-4333.

CO-LOCATED EVENTS SUBMISSION SITE OPENS Monday, Sept. 17, 2007, until Friday, Feb. 15, 2008.

DAC invites you to co-locate your event – conference, meeting or some other special event – at DAC. We will provide you with rooms at the Anaheim convention center at no cost, free admission for your attendees to the DAC exhibition floor on Monday and free access to DAC's keynotes. Your event will be financed and otherwise organized by you. Please see the website for further details, or call Kevin Lepine, Conference Manager at +1 303-530-4333.

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In Technical Cooperation with:

DESIGN AUTOMATION CONFERENCE

Call For Papers

Dear Colleague,

I'd like to invite you to submit your work to next year's Design Automation Conference (DAC) and get international recognition and prestige for work well done. The conference enables dialogue among peers and experts in our field. It is an opportunity for you to share your ideas and have a chance to win a Best Paper Award. Some new initiatives to encourage a broader audience include wireless and embedded design, Wild and Crazy Ideas – or WACI – Design Case Studies and a Design Contest. DAC is Where Electronic Design Meets! The Design Automation Conference is the world's premier conference for the design of electronic circuits and systems. We look forward to hearing from you.

Limor Fix
General Chair, 45th DAC

Eight types of submissions are invited:

Regular Papers • Special Sessions • Panels • Tutorials • Student Design Contest • Workshops • WACI • Co-Located Events

Submissions must be made electronically at www.dac.com. Panel and tutorial suggestions, and special session submissions, are due no later than 5:00pm Mountain Time, November 1, 2007. Visit our website for complete information on the electronic submission process:

www.dac.com

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Panel & Tutorial – Nov. 1, 2007
Regular Papers –Nov. 19, 2007
WACI – Nov. 19, 2007
Student Design Contest – Dec. 5, 2007
Workshops – Feb. 15, 2008
Co-Located Events – Feb. 15, 2008

All submissions are due by 5pm Mountain Time