ACM/EDAC/IEEE 45th DESIGN AUTOMATION CONFERENCE
JUNE 8-13, 2008 • ANAHEIM, CA • WWW.DAC.COM

45

State-of-the-art Research

Exhibits

Breakthrough Technology

Final Program

45 YEARS

DESIGN AUTOMATION CONFERENCE

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DAC: WHERE ELECTRONIC DESIGN MEETS . . .

WELCOME TO THE 45TH DESIGN AUTOMATION CONFERENCE AND THE CITY OF ANAHEIM!

DAC is the premier event for the electronic design community. It offers the industry's most prestigious technical conference in combination with the biggest exhibition. DAC is also increasingly the meeting place for many related organizations – the conference this year has attracted a record number of additional events. In particular, 14 workshops and seven collocated events are taking place during DAC.

We are privileged to have as guest speakers, the ACM Turing Award winners, who have been recognized with the highest honor in the area of computing for their role in developing Model-checking into a highly effective verification technology, widely adopted in the hardware and software industries: Edmund M. Clarke, FORE Systems Professor, Carnegie Mellon University, E. Allen Emerson, Endowed Professor, University of Texas at Austin and Joseph Sifakis, CNRS Research Director, Verimag.

DAC is proud to present outstanding industry leaders in three keynote presentations. On Tuesday, Justin R. Rattner, Intel Senior Fellow, Vice President, Director, Corporate Technology Group and Chief Technology Officer, Intel Corp., will re-examine radio architecture and describe the expected shift from largely analog to nearly pure digital and programmable multi-radios design. On Wednesday, Sanjay K. Jha, Chief Operating Officer, Qualcomm and President, Qualcomm CDMA Technologies, will present the design challenges of advanced wireless silicon systems. His talk will focus on how partnering companies need to collaborate to tackle complex design issues through synergistic groups. On Thursday, Jack Little, President, and Co-founder of The MathWorks, Inc., will discuss the emerging workflow from idea to system implementation. Such a design flow will provide great value to companies that develop embedded systems and electronics.

DAC's 82 member Technical Program Committee selected 147 papers for this year's technical program from a pool of 639 submissions. Highlighted topics this year are Business, Design Methodologies, System Level and Embedded Design, Interconnect and Reliability, Synthesis and FPGA, Low Power, Multi-core, Wireless, Physical Design, DFM and the Manufacturing Interface, Analog/Mixed Signal/RF and Simulation, Verification and Test, Strictly Design and New and Emerging Technologies. The program also includes eight Panels, eight Special Sessions, six Tutorials and six Hands-on Tutorials, Management Day and WACI ("Wild and Crazy Ideas"). DAC's exhibition features over 225 companies and includes 20 exciting Pavilion Panels.

New this year are DAC's iDesign sessions, the DACeZine newsletter, the YouTube preview of the technical program, the Exhibitor Forum that offers a series of technical presentations from exhibitors, and the Best of DAC Contest, which invites you to vote for your favorite products and vendors.

Continuing DAC's 45-year tradition, the efforts of hundreds of volunteers – authors, speakers, session chairs, reviewers, session organizers, moderators, panelists, and members of the DAC Executive Committee, Technical Program Committee, Panel Committee, Exhibitor Liaison Committee, SDC Judges, Tutorial Committee, and Strategy Committee – have gone into making DAC the premier event for the electronic design community. Fantastic contributions are also made by all of the companies participating in DAC's exhibition and by DAC's management company, MP Associates, Inc. We are grateful for all of this support and in particular, we extend special thanks to our sponsors, ACM/SIGDA, IEEE/CASS/CANDE/CEDA, and the EDA Consortium.

We wish you a productive and exciting week at DAC!

Best regards,

Limor Fix

Limor Fix
General Chair, 45th
Design Automation Conference

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Weather

Anaheim is one of the few places in the world with a Mediterranean climate. With 355 days of sunshine every year, it is nearly guaranteed that you will experience a beautiful tropical day. Anaheim offers delightful ocean breezes, low humidity, and very little rain. The average high temperature in June is 77 degrees, cooling off at night to 59 degrees. Summer clothing is appropriate and a light jacket may be needed for the evenings.

First Aid Room

The First Aid Room is located in Lobby B of the Anaheim Convention Center. For assistance, please call ext. 8101; for an emergency call ext. 8080. A nurse will be on duty at all times while meetings and exhibits are open. From a mobile phone, dial (714) 765-8950.

Guest/Family Program

An $80 registration fee will admit each guest or family member to the following:

1. Wednesday Night Party at the Anaheim Marriott in the Platinum Ballroom.

2. Admission to the exhibit hall (when accompanied by an attendee). Registration for the Guest/Family Program will be at the Conference Registration desk on Sunday, June 8 through Wednesday, June 11, 2008. A badge will be provided for each registered guest or family member. This badge must be worn to participate in the above activities.

3. Children under the age of 14 are not allowed in the exhibit hall area. A $30 registration fee will allow access to the Wednesday Night Party only.

On-site Information Desk

The Information Desk will be located in the Main Lobby of the Anaheim Convention Center, Phone: (714) 765-2014.

Anaheim Attractions

The Anaheim Resort is an 1100-acre garden district that encompasses the redesigned and expanded Anaheim Convention Center and the Disneyland Resort, which features the original Disneyland (this year is their 53rd anniversary), the thrilling new theme park – Disney's California Adventure, and the lively Downtown Disney, a new shopping, dining, and entertainment district. For more information on the Anaheim Resort and Orange County, visit www.anaheimoc.org or call the Anaheim/Orange County Visitor and Convention Bureau at (714)765-8888.

Hotel Locations

1 - Anaheim Marriott Hotel

2 - Hilton Anaheim Hotel

Important Information At-a-Glance

EXHIBIT HOURS

Monday, June 9 ..... 9:00am - 6:00pm
Tuesday, June 10 ..... 9:00am - 6:00pm
Wednesday, June 11 ..... 9:00am - 6:00pm
Thursday, June 12 ..... 9:00am - 1:00pm

REGISTRATION HOURS

Sunday, June 8 ..... 8:00am - 6:00pm
Monday, June 9 ..... 7:00am - 6:00pm
Tuesday, June 10 ..... 7:00am - 6:00pm
Wednesday, June 11 ..... 7:00am - 6:00pm
Thursday, June 12 ..... 7:00am - 6:00pm
Friday, June 13 ..... 8:00am - 6:00pm

TUTORIAL REGISTRATION

Monday Tutorial Registration

Register for Tutorials on Sunday and Monday at times above in Lobby B Conference Registration.

Friday Tutorial Registration

Friday, June 13 / 8:00am - 6:00pm

Tutorial Registration is located on the 2nd floor outside of Room 205AB.

STAY CONNECTED AT DAC

Wireless Internet

DAC is offering complimentary wireless internet throughout the Anaheim Convention Center. Look for SSID: **DAC2008**.

Mobile Devices

DAC has a special website built for viewing from handheld mobile devices. From your Windows Mobile or Blackberry device, log in to www.dac.com and you will be automatically redirected to the mobile site. Presentation schedules, the exhibitor listing and other useful information are available and optimized for viewing on small screens.

Daily Updates on DAC.com

Check the DAC website daily for a complete listing of each day's schedule, latest exhibitor announcements, and press coverage.

Food Courts

Two food courts and an espresso café are available on the exhibit floor. Each food court includes tables with power connections for laptop plug-in.

DACnet - 2008

DACnet internet stations are available in Lobby D and on the 2nd floor next to room 213A. Power for laptop plug-in is also available at both locations.

WEDNESDAY NIGHT PARTY

Wednesday, June 11 / 7:30 - 10:00pm

Please join us at the Anaheim Marriott Hotel in the Platinum Ballroom for the 45th DAC Wednesday Night Party! There will be a wide array of delectable foods along with plentiful amounts of wine, beer, and assorted beverages. This year DAC is proud to present The Zippers. Since their beginning as champions on Ed McMahon's StarSearch, the Zippers have performed to rave audiences the world over. Now featuring the addition of two incredibly talented female vocalists, the Zippers have achieved a new level that can only be described as spectacular. They are flashy, energetic, funny, and guaranteed to make you want to dance all night long. Entertainment begins at 8:00pm as The Zippers take you on a musical journey. Don't miss the fun! This is sure to be a memorable experience!

To join these festivities, you must register as a student or full conference attendee. You may also register for the Guest/Family Program.

Technical Program Highlights

This year's technical program is especially strong, consisting of 147 papers selected from 639 submissions, with Wild and Crazy Ideas (WACIs) and the popular panels and special sessions to round it out. The program, intended for design engineers, management, researchers and developers, showcases the latest results and emerging trends in the design of electronic circuits and systems, and Electronic Design Automation (EDA).

On Tuesday, the "iDesign" Track has been added. The first session will address how to build a practical physical implementation flow, while the second session offers hands-on aspects of SystemVerilog, the Verification Methodology Manual for SystemVerilog (VMM) and Open Verification Methodology (OVM). This year's conference theme is "Wireless", highlighted by an all-day track of sessions on Wednesday, including a panel that will identify who's ready for next-generation wireless multimedia devices, and a special session titled "Business Meets Technology."

In the 36 technical paper sessions, topics range from system-level design and design for manufacturing (DFM) to verification and emerging technologies. At DAC 2008 there is ample opportunity to discuss the emergence of multi-core systems. Speakers will discuss the latest in acceleration of circuit simulation on multi-threaded processors, and how to improve fault simulation on graphics processing units (GPUs).

A special session highlights issues related to the use of multi-cores for general-purpose as well as EDA applications. This is followed by a two-part panel; the first paper examines the outlook for EDA on multi-cores, providing the perspective of the major EDA vendors, while the second addresses the design of multi-core systems. Other sections of the technical program will illustrate how embedded systems are going multi-core as well, and present design tools to optimize embedded applications. A practical session for the verification engineer details how to achieve coverage convergence and verify multi-threaded processors.

DAC's embedded systems area continues to grow. A panel will determine whether Electronic System-level (ESL) signoff is imminent or impossible. Expect a debate about on-chip communication and it's role in upcoming generations of on-chip systems. Paper presentations will analyze the importance of security, design validation and cache optimization in modern embedded system design.

Emerging technologies that are enabling to the Moore's Law tracjectories of integration and cost - notably die stacking, system in package (SiP) and magnetic RAM - find their place in the "Beyond-the-Die" Track.

On-chip variability remains an important topic, with paper topics spanning improvements in statistical timing analysis, statistical transistor modeling, and methods to calculate on-chip capacitance sensitivity. Methods to avoid crosstalk and power delivery noise and to mitigate the effects of dynamic power gating will also be discussed. A DFM session will address what effects need to be considered during the design phase to minimize post-tapeout issues, and what circuit parameters need to be considered for more effective mask data preparation.

The technical program contains eight topical panels, including one that details how to verify extremely large systems and another that assesses the current state of DFM from the vantage point of practitioners working with cutting-edge technologies. A business-focused panel, (Session 6) goes beyond EDA and electronics design, and addresses how changes in the political and regulatory context can benefit our industry. Yet another panel will review whether custom design offers a worthwhile benefit over synthesized logic, while another panel will look at on-chip thermal problems. A slate of Pavilion panels, held on the exhibit floor, complements the technical program lineup by addressing design methodology, advanced technologies and business, as well as wireless theme-related other new topics.

Finally this year's technical program features six tutorials on subjects that span modern software programming, DFM, system-level synthesis and verification, system-level design for embedded systems, low-power design, and practical mixed-signal design principles. All tutorials have an emphasis on technology fundamentals that can be used productively - and immediately - in the design process. In addition, each tutorial has one or more speakers who are practitioners and use the technology on production designs.

The theme for this year's Hands-on Tutorials (HoTs) is "Embedding Intellectual Property (IP) in your Design: Challenges and Solutions."

Wireless Theme

Wireless applications can be found in every aspect of our lives. The wireless communications industry is diverse, with its products ranging from systems such as cellular phones, to personal wireless internet such as WiFi, to shorter-range devices such as low-power Bluetooth devices.

DAC explores wireless design and its impact on design automation from both a business and a technical perspective. While wireless communications systems represented more than 67% of the total communications systems market in 2007, cellular technology was more than 40% of that wireless market and remains the dominant driver of design automation technology.

Wireless semiconductor systems design requires design success on numerous fronts. This makes DAC the ideal place for the industry to explore design automation advances to solve wireless design challenges. Across a broad selection of technical paper sessions, special sessions, iDesign track, panels, and Pavilion panels, the DAC program covers the pressing deep-submicron, complex SoC design, verification, low-power and hardware/software design challenges that must be resolved to enable continued productivity of wireless design teams.

- **Monday, June 9 / 10:45 - 11:45am** **Booth #364**
  PAVILION PANEL: EDA Heritage Series: Maxwell's Legacy
- **Monday, June 9 / 3:00 - 3:45pm** **Booth #364**
  PAVILION PANEL: Today's Consumers: High Schoolers Spec Your Next Product
- **Tuesday, June 10 / 8:30 - 10:15am** **Ballroom ABC**
  KEYNOTE: EDA for Digital, Programmable, Multi-radios
- **Tuesday, June 10 / 4:00 - 4:45pm** **Booth #364**
  PAVILION PANEL: Quality Versus Time to Market: The Unmentionable Tradeoff
- **Wednesday, June 11 / 9:00 - 11:00am** **Room: 208AB**
  PANEL: Next Generation Wireless-multimedia Devices - Who is up for the Challenge?
- **Wednesday, June 11 / 11:15am - 12:15pm** **Ballroom ABC**
  KEYNOTE: Challenges on Design Complexities for Advanced Wireless Silicon Systems
- **Wednesday, June 11 / 2:00 - 4:00pm** **Room: 208AB**
  SESSION: Advanced Wireless Design
- **Wednesday, June 11 / 3:30 - 4:30pm** **Booth #364**
  PAVILION PANEL: Designing the New-generation Wireless Platform: Lessons from iPhone and Android
- **Wednesday, June 11 / 4:30 - 6:00pm** **Room: 208AB**
  SPECIAL SESSION: Wireless: Business Meets Technology

Exhibition Hours:
Monday - Wednesday, June 9 - 11 / 9:00am - 6:00pm
Thursday, June 12 / 9:00am - 1:00pm

Visit the DAC exhibition to learn in-depth information on new products and services from 225 vendors offering products and services for all phases of the electronic design process including EDA tools, IP cores, embedded system and system-level tools, as well as design-for-manufacturing, silicon vendors and design services companies. The DAC show floor features its unique exhibit booth and private suite combination, which gives you the freedom to deeply explore the products on the show floor and find the right solution for your design flow. Visit the DAC exhibition and find out how you can improve performance and shorten the time-to-market on your next design.

Check out these exciting features of the DAC exhibition:

NEW Best of DAC contest! Look for kiosks on the show floor and vote for your favorite vendors! When you cast your ballot you will be entered to win one of three Nintendo Wiis!

NEW Exhibitor Forum - DAC's newest feature for exhibit floor education. Attendees are invited to the Exhibitor Forum in Booth 2849 to hear a series of technical presentations from exhibitors on focused topics. Compare how exhibitors are solving your tough design issues with their latest tools and methodologies.

DAC Pavilion - The popular DAC Pavilion is back in Booth 364 with 20 presentations this year on business and technical issues.

Visit these First-time Participating Companies at DAC:

ACCIT - New Systems Research
Booth 1375

Acresso Software Inc.
Booth 1376

Amiq Consulting S.R.L.
Booth 682

Axilica Ltd.
Booth 1373

Common Platform
Booth 628

Cyclos Semiconductor, Inc.
Booth 1378

Dorado Design Automation, Inc.
Booth 2660

DTC, National Tsing Hua University
Booth 2867

Duolog Technologies Ltd.
Booth 241

Electronic Design and Solution Fair 2009
Booth 780

eXludus Tech., Inc.
Booth 1675

GATeIC
Booth 1371

Gauda
Booth 323

Imera Systems, Inc.
Booth 2861

iNoCs
Booth 1478

Jspeed Design Automation, Inc.
Booth 2866

Laflin HOTSCOPE
Booth 679

Paradigm Works, inc.
Booth 2318

Polar Instruments Inc.
Booth 1379

POLYTEDA Software Corp.
Booth 1365

Satin IP Tech.
Booth 1474

SeaSolve Software Inc.
Booth 1673

Snowbush Microelectronics
Booth 1435

SOI Consortium
Booth 678

Sonnet Software, Inc.
Booth 2119

Spatial
Booth 421

Synapse Design Automation
Booth 671

Tech Source Media, Inc./ SCDSource
Booth 606

Tela Innovations
Booth 473

The RTC Group
Booth 2765

WinterLogic Inc.
Booth 2767

IP, Design Services and Test Companies

Cyclos Semiconductor, Inc.
Booth 1378

PLD Applications (PLDA)
Booth 1479

Polar Instruments, Inc.
Booth 1379

SeaSolve Software, Inc.
Booth 1673

EDA for Digital, Programmable Multi-radios

Justin R. Rattner, *Intel Senior Fellow*
Vice President, Director, Corporate Technology Group
and Chief Technology Officer, Intel Corp., Hillsboro, OR

New technology and innovative usage models are driving the industry towards the ubiquitous use of wireless communications. The result is an end-to-end re-examination of radio architecture from the front end module to the MAC and the expected shift from largely analog to nearly pure digital radio design. Even RF power amplifiers will be digital, rather than analog in nature. Most importantly, radios will enter an age where one physical radio acts as many logical radios all at the same time. Much in the way computers evolved decades ago, radios will become multi-programmable. The combination of new radio architectures and mostly digital implementations will drive a new generation of design tools and techniques and, by necessity, will evolve to satisfy the demands of reconfigurable hardware and software programmability. Digital multi-radios will also accelerate the move from System-on-Chip to Platform-on-Chip design as all the elements of the platform, including the radios, are built on one chip using a single semiconductor process.

In his keynote, Intel's Chief Technology Officer, Justin Rattner, will talk about the challenges that this very high level of integration will have on design automation from architecture to manufacturing.

Justin Rattner, 59, is vice president and chief technology officer (CTO). He is also an Intel Senior Fellow and head of the Corporate Technology Group. In the latter role, he directs Intel's global research efforts in microprocessors, systems, and communications including the company's disruptive research activity.

In 1989, Rattner was named Scientist of the Year by R&D Magazine for his leadership in parallel and distributed computer architecture. In December 1996, Rattner was featured as Person of the Week by ABC World News for his visionary work on the Department of Energy ASCI Red System, the first computer to sustain one trillion operations per second (one teraFLOPS) and the fastest computer in the world between 1996 and 2000. In 1997, Rattner was honored as one of the Computing 200, the 200 individuals having the greatest impact on the U.S. computer industry today, and subsequently profiled in the book Wizards and Their Wonders from ACM Press.

Rattner has received two Intel Achievement Awards for his work in high-performance computing and advanced cluster communication architecture. He is a member of the executive committee of Intel's Research Council and serves as the Intel executive sponsor for Cornell University where he is a member of the External Advisory Board for the School of Engineering. Rattner is also a trustee of the Anita Borg Institute for Women and Technology.

Rattner joined Intel in 1973. He was named its first Principal Engineer in 1979 and its fourth Intel Fellow in 1988. Prior to joining Intel, Rattner held positions with Hewlett-Packard Company and Xerox Corporation. He holds B.S. and M.S. degrees from Cornell University in electrical engineering and computer science.

JUNE 11 / 11:15AM - 12:15 PM

RM: BALLROOM ABC

Challenges on Design Complexities for Advanced Wireless Silicon Systems

Sanjay K. Jha
Chief Operating Officer of Qualcomm, Inc.
President of Qualcomm CDMA Tech., San Diego, CA

The global wireless landscape continues to change as demand for 3G technology accelerates. Qualcomm is meeting the challenge with its highly integrated SoC solutions that enable customers worldwide to bring more advanced consumer devices to market faster. Relationships and tight collaboration continue to play an integral role in product development, as it becomes more crucial than ever for partnering companies to tackle complex design issues through synergistic groups such as EDA partners, foundry partners and customers. Technology migration with the right approach is also key as chipset design continues to evolve rapidly, bringing a whole new set of design challenges to semiconductor companies. Jha will elaborate on these present and future trends and reveal how collaborative business models are changing the game in chipset design.

Sanjay K. Jha is chief operating officer of Qualcomm, Inc. and president of Qualcomm CDMA Technologies (QCT). QCT is the world's top wireless chipset provider and largest fabless semiconductor producer.

Jha began his career at Qualcomm in 1994. In 2002, he led the formation of Qualcomm Technologies and Ventures, where he managed both the technology investment portfolio and the new technology group as senior vice president and general manager. He became executive vice president of Qualcomm and president of QCT in 2003, and was promoted to chief operating officer of Qualcomm in 2006. He is also a member of the Qualcomm Ventures advisory committee.

Jha has also served as chairman of the Fabless Semiconductor Association, the voice of the fabless business model and a group with more than 450 corporate members, now known as the Global Semiconductor Alliance (GSA).

Prior to joining Qualcomm, Jha held lead design engineering roles with Brooktree Corporation in San Diego, and GEC Hirst Research Labs in London. He holds a Ph.D. in electronic and electrical engineering from the Univ. of Strathclyde, Scotland and received his Bachelor of Science degree in engineering from the Univ. of Liverpool, England.

JUNE 12 / 12:45 - 1:45PM

RM: BALLROOM ABC

Idea to implementation: A Different Perspective on System Design

Jack Little
President and Co-founder, The MathWorks, Inc., Natick, MA

Today's electronic devices are multi-faceted, software-intensive systems that interact with the real world. These interactions create a new kind of complexity that increases pressure on engineering teams to deliver the right product under shrinking schedules. These multi-disciplinary teams are inhibited by gaps between the different tools and workflows they must use for system concept development, hardware design, and software development. Unless we connect these tools, we'll continue to see missed deadlines and spiraling verification costs.

Emerging EDA and software techniques promise to address some complexity issues such as system-on-chip verification and distributed processing. These important advances are necessary but not sufficient, because system design has become more than silicon and software.

To develop any electronic system, engineers must now characterize the impact of the "next-level system" - the system and environment in which their product must operate. For example, the design of the electronics and software in a hybrid electric vehicle depends on requirements imposed by vehicle dynamics, while a multimedia mobile phone's design is impacted by network traffic.

In response to this challenge, we have seen a significant movement to bridge math-based system modeling with established hardware and software implementation and verification flows using Model-based Design. Central to this approach are multi-domain models that engineers use to specify and validate system behavior. The models provide the basis for design elaboration, automatic code generation, and earlier detection and correction of design flaws.

Leading automotive and aerospace companies have applied model-based design to accelerate embedded system development while improving software reliability, supported by a broad collection of vendors providing simulation, prototyping, implementation, and testing capabilities. Now this approach is rapidly extending into communications, electronics, industrial automation, and other industries as new tools, workflows, and partnerships are established to address design and verification problems that span systems, hardware, and software.

The solution to tomorrow's design challenges won't come solely from any one of the traditional tool categories, but from an interdisciplinary collaboration to deliver a complete tool chain that provides a flow from idea to system implementation. This will provide great value to companies that develop embedded systems and electronics, while creating growth opportunities for all tools that participate in the new workflow.

Jack Little is president and a co-founder of The MathWorks, Inc. He was a co-author and principal architect of early versions of the company's flagship MATLAB product as well as, the Signal Processing Toolbox and the Control System Toolbox.

Little holds a B.S. degree in electrical engineering and computer science from MIT and an M.S.E.E. degree from Stanford University.

A Fellow of the IEEE and Trustee of the Massachusetts Technology Leadership Council, he writes and speaks about technical computing, model-based design, entrepreneurship, and software industry issues.

Management Day is designed to provide managers with timely information to help them make decisions where business and technology intersect. The day is comprised of three sessions featuring presentations by managers representing key integrated device manufacturers (IDMs) and major fabless companies. Consumer application chips are the technology drivers today. They require different types of optimizations and thus the adoption of emerging solutions to meet such requirements. Optimizing for low power, high volume production, and shrinking sizes necessitates adequate trade-off analysis and technical/business decision making by management. Also, moving to new semiconductor technology nodes, such as 45nm and 65nm, can significantly affect the choices of suppliers. Management Day sessions will discuss these changing needs and demonstrate corresponding management decision criteria to make the right choices from a pool of alternate options for flows, methodologies and suppliers. The leading managers of today's most complex nanometer chips will present these emerging solutions and their economic impact. This year's Management Day will provide a unique opportunity for managers to gain insights from their peers in the industry.

Registration Required
$95

8:30 - 10:15am **Keynote: Justin R. Rattner - EDA for Digital Programmable Multi-radios** - **Ballroom ABC**

10:30am -12:00pm **Session 1: Managing Low Power SoC Development on Emerging Technology Nodes**

Session Chair:
Ron Wilson - *EDN Worldwide, San Jose, CA*

Session Organizer:
Yervant Zorian - *Virage Logic Corp., Fremont, CA*

Low power chips are the technology drivers today. They require multi-dimensional optimization and thus the need to adopt emerging technology nodes to meet such requirements. Optimizing for low power production, and shrinking sizes necessitate adequate trade-off analysis and technical/business decision making by management. The leading managers in this session will discuss today's emerging solutions and their economic impact.

Key Design Challenges of 45nm Intel Atom Low Power Processor
Elinora Yoeli - *Vice President, Mobility Group, Intel Corp., Santa Clara, CA*

45/40nm Low Power Design Solutions for Wireless Multi-media SoCs
Philippe Magarshack - *Vice President, Central R&D, STMicroelectronics, Crolles, France*

A Case Study of 65nm 5-million Instances Chip Development
Andrew C. Chang - *Vice President, Design Tech., MediaTek, Inc., Hsinchu, Taiwan*

2:00 - 4:00pm **Session 2: Trade-offs and Choices for Advanced SoCs in High-volume Application**

Session Chair:
Nic Mokhoff - *EE Times, Manhasset, NY*

Session Organizer:
Yervant Zorian - *Virage Logic Corp., Fremont, CA*

Design and manufacturing flows and methodologies are directly impacted by the demand for high volume SoCs with increasing performance and parallelism. Moving to new semiconductor technology nodes while producing in high volumes can significantly affect the choices of suppliers. This session will provide an overview of changing needs and corresponding management decision criteria to make the right choices from a pool of alternate options for flows, methodologies and internal/external suppliers.

Challenges That New Wireless SoC Designs Are Facing from New Process Technology Nodes
Charles Matar - *Vice President of Engineering, Qualcomm, Inc., San Diego, CA*

A 45nm Power Optimized Digital Baseband SoC - An Introspective Review
Bob Pitts - *45nm Platform Manager, Texas Instruments, Inc., Dallas, TX*

Graphics Processor for XBOX-360 - Cost Reduction - Design Challenges and Decision Criteria
Srinivas Nori - *ASIC Design Manager, XBOX Silicon Development, Microsoft Corp., Mountain View, CA*

From Specifications to High Volume Production
Manuel D'Abreu - *Director, SanDisk Corp., Milpitas, CA*

4:30 - 5:30pm **Session 3: Panel Discussion - Making Critical Decisions for Emerging SoC Development**

Session Chair:
Peggy Aycinena - *EDA Confidential, San Mateo, CA*

Session Organizer:
Yervant Zorian - *Virage Logic Corp., Fremont, CA*

This panel is designed to provide the attendees with timely information to help them make decisions where business and technology intersect. The panel complements the two management presentation sessions where the key managers of today's most complex nanometer chips will discuss the emerging solutions and discuss their economic impact. This Management Day panel will provide a unique opportunity for all attending managers to interact directly with the panelists and gain insights from their peers in the industry.

Panelists:
Elinora Yoeli, *Vice President, Mobility Group, Intel Corp., Santa Clara, CA*
Philippe Magarshack, *Vice President, Central R&D, STMicroelectronics, Crolles, France*
Andrew C. Chang, *Vice President, Design Tech., MediaTek, Inc., Hsinchu, Taiwan*
Charles Matar, *Vice President of Engineering, Qualcomm, Inc., San Diego, CA*
Bob Pitts, *45nm Platform Manager, Texas Instruments, Inc., Dallas, TX*
Srinivas Nori, *ASIC Design Manager, XBOX Silicon Development, Microsoft Corp., Mountain View, CA*
Manuel D'Abreu, *Director, SanDisk Corp., Milpitas, CA*

5:30 - 6:00pm **Reception**

NEW! Exhibitor Forum - Exhibit Hall D, Booth #2849

COFLUENT DESIGN - EARLY DECISION TRADE-OFF, ADDRESSING PERFORMANCE CONCERNS IN FUTURE NETWORK INFRASTRUCTURE

Monday, June 9 / 9:30 - 10:10am

As demand on network resources grows, and multi-core processing capabilities increase, software elements are soon to dominate the networking infrastructure application domain. System architects have to make correct cost-impacting decisions and performance tradeoffs, prior to any implementation commitment or development investment. Following a "Y" design flow, CoFluent Studio allows users to elaborate the most adequate partitioning strategy across multiple cores, distributing I/O connectivity, managing shared resources, optimizing communications on the fabric interconnect and profiling power consumption.

Presenters: Hagay Zamir, Laurent Isenegger - *CoFluent Design, San Jose, CA*

MENTOR GRAPHICS CORP. - OBJECT ORIENTED HARDWARE REUSE WITH ANSI C+++ AND ALGORITHMIC SYNTHESIS

Monday, June 9 / 10:10 - 10:50am

Both algorithm researchers and hardware designers can learn how to use ANSI C+++ to implement and verify algorithmic designs in ASIC or FPGA hardware, balancing design requirements for performance, area and power with Algorithmic C Synthesis. This exhibit will cover a coding style based on C+++ object oriented templates for a highly flexible reuse methodology. The end result is high performance hardware typical in wireless, video and imaging products.

Presenter: Andres Takach - *Mentor Graphics Corp., Wilsonville, OR*

MENTOR GRAPHICS CORP. - WHAT YOU SHOULD KNOW ABOUT THE OPEN VERIFICATION METHODOLOGY (OVM)

Monday, June 9 / 10:50 - 11:30am

This presentation covers the use and benefits of the Open Verification Methodology (OVM). The OVM brings together verification knowledge, experience and expertise to provide a modular approach to building reusable verification IP and testbenches powerful enough to meet the most demanding requirements, yet easy to adopt. We will touch on all aspects of the OVM, including the following: testbench architecture, transaction-level modeling in verification, sequential stimulus and block-to-system-level reuse.

This session followed by 15 min. of Q & A

Presenter: Tom Fitzpatrick - *Mentor Graphics Corp., Wilsonville, OR*

MAGMA DESIGN AUTOMATION - TITAN™ CHIP FINISHING AND FASTER ANALOG DESIGN IMPLEMENTATION/MIGRATION

Monday, June 9 / 2:00 - 2:40pm

Efficiency improvements in analog design implementation/migration have not kept pace with the digital standard cell world. In addition, finishing complex mixed-signal chips has become increasingly unwieldy due to the database and tool disconnect between the analog and digital domains. Titan, the comprehensive mixed-signal platform from Magma, addresses both these areas by bringing unprecedented automation to analog circuit design, optimization, floorplanning, placement and routing. Titan eliminates the disconnect between the analog and digital domains in handling late ECOs, verification and custom layout for chip finishing.

Presenter: Khalid Islam - *Magma Design Automation, Inc., Austin, TX*

MENTOR GRAPHICS CORP. - MENTOR GRAPHICS CORP. AND AGILENT TECHNOLOGIES INTEGRATED RF DESIGN SOLUTION FOR PCBs

Monday, June 9 / 2:40 - 3:20pm

The proliferation of wireless consumer devices has pushed the PCB design envelope, due to increasingly short time-to-market windows for innovative products that require greater functionality. Mentor's new RF Design Solution allows simultaneous and seamless RF, analog, and digital design in Expedition Enterprise and Agilent ADS through Mentor's two-way Dynamic Link interface. This integration of technologies allows full parameter-driven schematic and layout design with an easily-synchronized RF library, providing the most automated mixed-signal design, simulation, and implementation solution on the market.

Presenters: John Isaac, Per Viklund - *Mentor Graphics Corp., Longmont, CO*

Free and open to ALL attendees!

NEW! Exhibitor Forum - Exhibit Hall D, Booth #2849

DENALI SOFTWARE, INC. - KEY INGREDIENTS OF A NEXT-GENERATION NAND FLASH PLATFORM

Monday, June 9 / 3:20 - 4:00pm

This presentation will discuss the challenges of developing and verifying a multichannel NAND Flash SoC platform Flashpoint™; which was designed to maximize the random read/write operations of the controller and maximize the bandwidth of a system using NVMHCI, PCIe 2.0, and ONFi 2.0. We will explore several key developments and tools that allow Flashpoint to achieve the desired performance parameters, including HW-SW partitioning and extensive use of DMA and hardware accelerated approaches.

Presenter: **Robert Pierce** - *Denali Software, Inc., Sunnyvale, CA*

This session followed by 15 min. of Q & A

MENTOR GRAPHICS CORP. - 2-D AND 3-D VARIABILITY OPTIMIZATION

Tuesday, June 10 / 2:00 - 2:40pm

Variability is a reality creating hurdles in physical design and verification. To ease designers' jobs, DFM must be integrated into design flows to automate improvements, manage complex design rules, and ensure timing closure based on "as built" device and interconnect models. This session shows designers how to deal with variability and reduce time to tapeout; how DFM tools are expanding from 2-D to 3-D analysis and from functional to electrical DFM; how DFM can be integrated into the design process.

Presenter: **David Abercrombie** - *Mentor Graphics Corp., Wilsonville, OR*

MENTOR GRAPHICS CORP. - MULTI-CORNER-MULTI-MODE P&R FOR TIMING, POWER, AND SI CLOSURE

Tuesday, June 10 / 2:40 - 3:20pm

Achieving closure for ICs with many operating modes and complex low power techniques is a critical design challenge in advanced ICs. Smaller geometries present more difficult signal integrity problems; higher interconnect resistance impacts circuit performance and reliability of clock trees. Designs are taking longer and designers are forced to increase design margins, leaving performance on the table. This session shows how multi-corner-multi-mode timing and SI analysis and DFM-aware routing can improve the speed and quality of advanced 45nm designs.

Presenter: **Sudhakar Jilla** - *Mentor Graphics Corp., San Jose, CA*

BLAZE DFM, INC. - LEAKAGE POWER REDUCTION USING ELECTRICAL DFM TECHNIQUES (CUSTOMER CASE STUDY)

Tuesday, June 10 / 3:20 - 4:00pm

Blaze MO reduces leakage power by 20% and cuts leakage variability in half on 90nm, 65nm, and 45nm digital chips. It has been proven in silicon on numerous customer designs. It works on both new and existing designs. It does not require changes to the chip architecture, IP blocks, libraries, logic design, or layout. A customer case study will be presented on how the design team was able to significantly lower leakage power on a multi-million gate system-on-chip (SoC).

Presenter: **Dave Reed** - *Blaze DFM, Inc., Sunnyvale, CA*

PYXIS TECHNOLOGY, INC. - PYXIS HIGH PERFORMANCE YIELD-AWARE IC ROUTER

Wednesday, June 11 / 9:15 - 9:55am

Pyxis Technology will give a presentation on its NexusRoute IC router, highlighting key architectural features required for 45nm design closure and contrasting these features against existing router architectures. The presentation will also discuss how the router has been successfully integrated into existing EDA design flows and used with customers such as Microsoft Corporation to provide as much as a 4X improvement in design closure cycle time with faster circuit performance, lower power and higher predicted yield.

Presenter: **Phil Bishop** - *Pyxis Tech., Inc., Austin, TX*

This session followed by 15 min. of Q & A

Free and open to ALL attendees!

NEW! Exhibitor Forum - Exhibit Hall D, Booth #2849

TEKLATECH - IR DROP AND NOISE AWARE SoC FLOORPLANNING

Wednesday, June 11 / 9:55 - 10:35am

As IC fabrication technologies scale into nanometer geometries, physical-level issues present an increasing challenge to semiconductor companies. Addressing power and timing integrity in early design phases is critical to maintaining proper sign-off without compromising leakage power, area and design time. Increasing parasitics and fast on-chip switching times make it vital to control the dynamic power usage in order to reduce noise and IR drop peaks. Teklatech's FloorDirector™ provides IR drop and noise aware floorplanning, enabling designs which are robust to sign-off challenges.

Presenter: Tobias Bjerregaard - *Teklatech, Copenhagen, Denmark*

TELA INNOVATIONS, INC.- 45nm LEAKAGE REDUCTION USING GRIDDED, ONE DIMENSIONAL LAYOUT

Wednesday, June 11 / 10:35 - 11:15am

45nm test chip results will be presented based on Tela Innovations proprietary, unidirectional, on-grid layout techniques demonstrating substantial reduction in leakage, variability and area. Tela's topology based layout methodology will be reviewed in the context of existing SoC design flows. The applicability of these layout structures to enable double patterning techniques for 32nm and 22nm nodes will be covered.

Presenter: Neal Carney - *Tela Innovations, Inc., Campbell, CA*

This session followed by 15 min. of Q & A

AZURO, INC. - CLOCK IMPLEMENTATION FOR NANOMETER CHIP DESIGN

Wednesday, June 11 / 2:00 - 2:40pm

Effective clock design at nanometer geometries requires some new thinking to keep CTS from becoming a major bottleneck in the flow. A CTS tool must be directly driven by the designer's underlying objectives, such as timing, power, and area. Customers are using Azuro's PowerCentric in all major design flows as a complete CTS solution, addressing dynamic power, skew, insertion delay, OCV, variability and routability. PowerCentric also provides unique visualizations that permit designers to manage even the most complex clock structures.

Presenter: Marc Swinnen - *Azuro, Inc., Santa Clara, CA*

SYNFORA, INC. - ARCHITECTURAL EXPLORATION FOR LOW POWER DESIGN USING PICO EXTREME

Wednesday, June 11 / 2:40 - 3:20pm

Power consumption, rather than area, is an increasingly key design parameter for SoCs for integrated mobile devices. Currently, designers have no practical method to perform architectural and micro-architectural exploration for low power design. Algorithmic synthesis using PICO Extreme enables the implementation of complex hardware sub-systems from untimed, sequential C algorithms. Integration of PICO Extreme with an RTL power estimation tool enables exploration of multiple algorithms and architectures with different power profiles to determine the optimal algorithm-architecture combination in a very short period of time. This presentation will describe this new methodology for low power design and illustrate it using real-life examples.

Presenter: Vinod Kathail -*Synfora, Inc., Mountain View, CA*

SEQUENCE DESIGN, INC. - DESIGN FOR POWER

Wednesday, June 11 / 3:20 - 4:00pm

Design for Power (DFP) has become essential for product success, especially in today's consumer driven battery powered market. This presentation will focus upon particular DFP methods and techniques, focusing on those deployed early in the design process when DFP can be most effective. In addition, the concept of power regression testing will be introduced as a means of tracking and controlling power consumption beginning at the earliest design phases and continuing through tapeout.

Presenter: Jerry Frenkil - *Sequence Design, Inc., Santa Clara, CA*

This session followed by 15 min. of Q & A

Free and open to ALL attendees!

DAC Pavilion Panels - Exhibit Hall B, Booth #364

MONDAY, JUNE 9 / 9:30 - 10:30AM

PAVILION PANEL: GARY SMITH ON EDA: TRENDS AND WHAT'S HOT AT DAC

Chair: **Robert Gardner** - *EDA Consortium, San Jose, CA*
Organizer: **Gary Smith** - *Gary Smith EDA, Santa Clara, CA*

EDAC brings you DAC's traditional kick off: Gary Smith reviews EDA's hottest technology trends. What's shaping design over the next 5 years? How is DFM changing EDA? How is parallel computing affecting EDA tool development? Which acquisitions were critical in 2007 and which ones should you watch for in 2008? What are the "must see" products? Find out here!

Speaker:
Gary Smith - *Gary Smith EDA, Santa Clara, CA*

MONDAY, JUNE 9 / 10:45 - 11:45AM

PAVILION PANEL: EDA HERITAGE SERIES: MAXWELL'S LEGACY

Chair: **Rich Goldman** - *Synopsys, Inc., Mountain View, CA*
Organizer: **Rich Goldman** - *Synopsys, Inc., Mountain View, CA*

James Clerk Maxwell stands shoulder to shoulder with Newton and Einstein, yet even those of us who have spent decades working with Maxwell's equations are almost totally unfamiliar with his life and times. What is Maxwell's legacy to us? This presentation provides insight into Maxwell's life and adds depth to those four simple equations we have studied ever since.

Speaker:
James C. Rautio - *Sonnet Software, Inc., Syracuse , NY*

MONDAY, JUNE 9 / 12:00 - 1:00PM

PAVILION PANEL: STUDENT DESIGN CONTEST AWARD PRESENTATION

Chair: **Byunghoo Jung** - *Purdue Univ., West Lafayette, IN*
Organizer: **William Bowhill** - *Intel Corp., Hudson, MA*

Presentation of the nine student design award winners, across operational, system-level and conceptual award categories of the Student Design Contest, organized by the Design Automation Conference and the International Solid-state Circuits Conference (ISSCC).

MONDAY, JUNE 9 / 2:00 - 2:45PM

PAVILION PANEL: NEXT GENERATION DATA CENTERS: ENVIRONMENTALLY GREEN, FINANCIALLY GREEN

Chair: **Joel Swisher** - *Rocky Mountain Institute, Boulder, CO*
Organizer: **Kevin Silver** - *Denali Software, Inc., Palo Alto, CA*

Data center energy costs can be 100 times higher than those for typical buildings according to Lawrence Berkeley National Laboratory. Even a small improvement in energy efficiency can significantly reduce environmental impact and operating costs. Following an overview of data centers and the challenges associated with energy efficiency, the panelists take a fresh look at leading-edge technology and environmental legislation that enable green data centers.

Speakers:
Dileep Bhandarkar - *Microsoft Corp., Redmond, WA*
Mark Bramfitt - *PG&E Corp., San Francisco, CA*
Bill Weihl - *Google, Washington, DC*

MONDAY, JUNE 9 / 3:00 - 3:45PM

PAVILION PANEL: TODAY'S CONSUMERS: HIGH SCHOOLERS SPEC YOUR NEXT PRODUCT

Chair: **Kathryn Kranen** - *Jasper Design Automation, Inc., Mountain View, CA*
Organizer: **Rich Goldman** - *Synopsys, Inc., Mountain View, CA*

We all want to design the new hot consumer device like the iPod or the Wii. Today's consumers are college students and high schoolers, and they think very differently from you. This panel features tech savvy Java programming students. Hear what these high schoolers find cool in current devices and what they want in the future.

Speakers:
JonMichael Guay, Brett Davis, Justin Towers - *Servite High School, Anaheim, CA*

MONDAY, JUNE 9 / 4:00 - 5:00PM

PAVILION PANEL: WILL 22NM BE OUR CATCH-22?

Chair: **Joe Sawicki** - *Mentor Graphics Corp., Wilsonville, OR*
Organizer: **Gene Forte** - *Mentor Graphics Corp., Wilsonville, OR*

Does the world end at 22nm? Will optical lithography fail, forcing us to use nanoimprinting, direct-write e-beam or some other exotic imaging technology? Will silicon fail us completely? This panel of experts drawn from the tools, design services, process technology, and semiconductor foundry communities looks into their collective crystal ball for answers.

Speakers:
S. T. Juang - *Taiwan Semiconductor Manufacturing Company, Ltd., Hsin-Chu, Taiwan*
John Kibarian - *PDF Solutions, Inc., San Jose, CA*
Lars Liebmann - *IBM Corp., East Fishkill, NY*

Free and open to ALL attendees!

DAC Pavilion Panels - Exhibit Hall B, Booth #364

TUESDAY, JUNE 10 / 10:30 - 11:15AM

PAVILION PANEL: 45NM: COLLABORATE, AGGREGATE, DIFFERENTIATE

Chair: **Mike Santarini** - *Xilinx, Inc., San Jose, CA*
Organizer: **Phil Dworsky** - *Synopsys, Inc., Mountain View, CA*

At 45nm, process is being defined by a limited few, everyone has access to the same IP and tools, and fabs may no longer be differentiators even for IDMs. Where will differentiation come from? Some companies are turning to collaboration; others are moving toward a re-aggregated model. These experts will explore how companies can succeed at 45nm and beyond.

Speakers:
Naveed Sherwani - *Open-Silicon, Inc., Milpitas, CA*
Ana Hunter - *Samsung, San Jose, CA*
Alex Shubat - *Virage Logic Corp., Fremont, CA*

TUESDAY, JUNE 10 / 11:30AM - 12:15PM

PAVILION PANEL: EDA: A VIEW FROM SAND HILL ROAD

Chair: **Lucio Lanza** - *Lanza Tech. Ventures, Palo Alto, CA*
Organizer: **Dave Kelf** - *Sigmatix, Inc., Boston, MA*

Today, locating investment for even the most exciting of EDA startups is challenging. What are investors looking for in EDA companies, what are the interesting trends and opportunities and what investments are being made? Why is investment in EDA critical to the entire electronics industry?

Speakers:
Juan-Antonio Carballo - *Argon Venture Partners, Redwood City, CA*
Kent Shimasaki - *Nollenburger Partners, San Francisco, CA*
Erach Desai - *Integrated Corporate Relations, Inc, Boston, MA*

TUESDAY, JUNE 10 / 1:00 - 1:45PM

PAVILION PANEL: MULTI-PROCESSOR SOCS: THE NEXT GENERATION

Chair: **Markus Levy** - *Multicore Assoc., El Dorado Hills, CA*
Organizer: **Dave Kelf** - *Sigmatix, Inc., Boston, MA*

A 1990s IC designer awakening from a coma in 2008 would observe little change in the SoC design/verification flows, despite order of magnitude leaps in multiprocessor SoC complexity. Recent ESL advances, such as transaction-based acceleration/emulation, system-level modeling, virtual prototyping, platform-based design, and high level synthesis have not yet gone mainstream. Why not?

Speakers:
Sreenivasa Rao - *Analog Devices, Inc., Wilmington, MA*
Laurent Ducousso - *STMicroelectronics, Grenoble, France*
Grant Martin - *Tensilica, Inc., Santa Clara, CA*

TUESDAY, JUNE 10 / 2:00 - 2:45PM

PAVILION PANEL: IP SELECTION: THE GOOD, THE BAD, AND THE UGLY

Chair: **Jordan Selburn** - *iSuppli Corp., El Segundo, CA*
Organizer: **Meghan Le** - *Synopsys, Inc., Mountain View, CA*

As the number of third-party IP vendors increases, the quality of available IP varies dramatically. Although purchased IP can reduce project cycle time and improve time to market, integrating a bad (or worse, ugly) piece of IP can mean costly re-spins and missed market windows. How do you find the gold among the dross?

Speakers:
Satya Gupta - *Open-Silicon, Inc., Milpitas, CA*
Joachim Kunkel - *Synopsys, Inc., Mountain View, CA*
Kathy Werner - *Freescale Semiconductor, Inc., Austin, TX*

TUESDAY, JUNE 10 / 3:00 - 3:45PM

PAVILION PANEL: EDA GLOBALIZATION: THIRD WORLD OR NEW WORLD?

Chair: **Jodi Shelton** - *Global Semiconductor Alliance, Dallas, TX*
Organizer: **Yatin Trivedi** - *Magma Design Automation, Inc., San Jose, CA*

Leading edge SoC projects are now starting in far away places. EDA suppliers must support them as if in their own backyards. What are the challenges? Has outsourcing encircled the EDA industry or does EDA have it covered? Semiconductor industry leaders from India and China present the everyday challenges and unique solutions offered by the local industry ecosystems.

Speakers:
S. Janakiraman - *Mindtree Services, Bangalore, India*
Shaojun Wei - *Tsinghua Univ., Beijing, China*

TUESDAY, JUNE 10 / 4:00 - 4:45PM

PAVILION PANEL: QUALITY VERSUS TIME TO MARKET: THE UNMENTIONABLE TRADEOFF

Chair: **Will Strauss** - *Forward Concepts Co., Tempe, AZ*
Organizer: **Rajiv Maheshwary** - *Synopsys, Inc., Mountain View, CA*

The enormous wireless market has completely altered the rules of product development. Timeliness is everything. But does timeliness come at the expense of quality and performance? This panel will explore how to improve turn around time (TAT), time to results (TTR), and time to market (TTM), but would you trade off quality for a 50% increase in these areas?

Speakers:
Andrew C. Chang - *MediaTek, Inc., Hsinchu, Taiwan*
Atul Jain - *Texas Instruments, Inc., Bangalore, India*
T. W. Williams - *Synopsys, Inc., Mountain View, CA*

Free and open to ALL attendees!

DAC Pavilion Panels - Exhibit Hall B, Booth #364

TUESDAY, JUNE 10 / 5:00 - 5:45PM

PAVILION PANEL: SOI: FACT, FUTURE AND FICTION

Chair: **Richard Goering** - *SCDsource, Felton, CA*
Organizer: **Horacio Mendez** - *SOI Industry Consortium, Austin, TX*

Silicon on Insulator (SOI) technology has promised a next-generation alternative to traditional bulk CMOS, enabling high performance without the heat and power issues associated with other substrates. Although SOI has been perceived as cost-prohibitive for all but limited applications, recent developments demonstrate otherwise. This panel of SOI experts will discuss the benefits and challenges associated with SOI.

Speakers:
Percy Gilbert - *IBM Corp., East Fishkill, NY*
Nick Kepler - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Jean-Luc Pelloie - *ARM, Grenoble, France*

WEDNESDAY, JUNE 11 / 9:30 - 10:30AM

PAVILION PANEL: HOGAN'S HEROES - BEHAVIORAL SYNTHESIS: IS THAT LIGHT AT THE END OF THE TUNNEL AN ONCOMING TRAIN?

Chair: **Jim Hogan** - *Vista Ventures Partners, Campbell, CA*
Organizer: **Jim Hogan** - *Vista Ventures Partners, Campbell, CA*

Jim Hogan grills industry experts about critical system design challenges. What really can be expected of high-level synthesis? Where does h synthesis work? Has a usable methodology and flow developed? What level of abstraction is practical? What types of efficiencies can you expect on first pass and re-spins?

Speakers:
Jason Cong - *Univ. of California, Los Angeles, CA*
Loic Le Toumelin - *Texas Instruments, Inc., Nice, France*
Jan Willis - *Calibra, Bracknell, United Kingdom*

WEDNESDAY, JUNE 11 / 1:00 - 2:00PM

PAVILION PANEL: ADVANCED LOW POWER TECHNIQUES: IS YOUR DESIGN METHOD TOO POWERFUL?

Chair: **Gary Delp** - *LSI Logic Corp., Rochester, MN*
Organizers: **Sabina Burns** - *Virage Logic Corp., Fremont, CA*

Because of the increasing adoption of mobile device technologies and the shift toward sub-90nm geometries, advanced techniques for low power are rapidly moving from early-adopter to mainstream. Panelists will discuss actual experiences "the good and the bad" in applying advanced 65nm and 45nm low power technologies and methodologies in real projects.

Speakers:
Yoshio Inoue - *Renesas Tech. Corp., Itami-shi, Hyogo, Japan*
Juergen Karmann - *Infineon Tech. AG, Munich, Germany*
David Hathaway - *IBM Corp., Essex Junction, VT*

WEDNESDAY, JUNE 11 / 2:30 - 3:15PM

PAVILION PANEL: DFM DESIGN RULES: WORTH THE EFFORT?

Chair: **Dave Maliniak** - *Electronic Design, Penton Media, New York, NY*
Organizer: **Cedric Iwashina** - *Blaze DFM, Inc., Sunnyvale, CA*

At 65nm, foundries have added many new design rules intended to improve manufacturability and boost yield. But are these rules working for you? If so, do the benefits justify the increased cost and complexity of design? How many more rules will you have to endure in the future and how many will remain optional?

Speakers:
Michael Buehler-Garcia - *Ponte Solutions, Inc., Mountain View, CA*
Ed Chen - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Walter Ng - *Chartered Semiconductor Manufacturing, Milpitas, CA*

WEDNESDAY, JUNE 11 / 3:30 - 4:30PM

PAVILION PANEL: DESIGNING THE NEW-GENERATION WIRELESS PLATFORM: LESSONS FROM iPHONE AND ANDROID

Chair: **Ron Wilson** - *EDN Worldwide, San Jose, CA*
Organizer: **Dave Kelf** - *Sigmatix, Inc., Boston, MA*

Apple's iPhone has been hailed as a shining example of next-generation user interface design coupled with state-of-the-art wireless technology. Google's proposed Android open software platform is meant to unify applications across different hardware platforms. Portelligent and ARM take you under the covers of these remarkable devices, providing insight on their design advances and innovations.

Speakers:
James Bruce - *ARM, Sunnyvale, CA*
Dave Carey - *Portelligent, Inc., Austin, TX*

WEDNESDAY, JUNE 11 / 5:00 - 5:45PM

PAVILION PANEL: WHAT'S HOLDING BACK ANALOG DESIGN AUTOMATION?

Chair: **Gabe Moretti** - *Gabe on EDA, Venice, FL*
Organizer: **Dave Millman** - *Ciranova, Inc., Santa Clara, CA*

While digital design automation has moved forward with amazing speed over the past 20 years, analog design automation has lagged far behind, particularly analog physical design automation. Are analog designers ready for automation? Are adequate analog tools and methodologies available? Will they take us to true SoC designs for consumer and RF devices? Is there any hope for innovation?

Speakers:
Anirudh Devgan - *Magma Design Automation, Inc., Austin, TX*
Jim Solomon - *Ciranova, Inc., Santa Clara, CA*
Rudy C. Hernandez - *Texas Instruments, Inc., Dallas, TX*

DAC Pavilion Panels - Exhibit Hall B, Booth #364

THURSDAY, JUNE 12 / 10:00 - 10:45AM

PAVILION PANEL: NEGOTIATING A SUCCESSFUL CAREER

Chair: **Peggy Aycinena** - *EDA Confidential, San Mateo, CA*
Organizer: **Sabina Burns** - *Virage Logic Corp., Fremont, CA*

Join Intel's Limor Fix, 2008 DAC General Chair, in a one-on-one conversation with EDA Confidential's Peggy Aycinena as they discuss the other side of your career equation – those negotiation and networking skills that can prove as important to your future success as the technical skillset you bring to the workplace. Fix and Aycinena will discuss the challenges of setting short-term and long-term goals, having the wisdom to see your own strengths and weaknesses and how to leverage that wisdom in crafting your career, and the importance of building trusted relationships with your co-workers – particularly in large, distributed, multi-national organizations. Finally, who better than the DAC General Chair to examine the many benefits of attending conferences, the ultimate networking venue. The conversation promises to be lively and wide-ranging, with ample opportunity for audience participation in a discussion that spans both gender and generational issues.

Moderator:
Peggy Aycinena - *EDA Confidential, San Mateo, CA*
2008 Chair, Workshop for Women in Design Automation

Speaker:
Limor Fix - *Intel Research Pittsburgh, Pittsburgh, PA*

This year's winner of the Marie R. Pistilli Women in EDA Achievement Award:

Louise Trevillyan - *Research Staff Member, Design Automation Department, IBM T.J. Watson Research Center*

THURSDAY, JUNE 12 / 11:00 - 11:45AM

PAVILION PANEL: YOUR FUNCTIONAL VERIFICATION ROADMAP: OVM, VMM, OR ROLL YOUR OWN?

Chair: **Brian Bailey** - *Brian Bailey Consulting, Beaverton, OR*
Organizer: **Francine Bacchini** - *Francine Bacchini, Inc., San Jose, CA*

What is the future for verification? This panel of verification experts will discuss two key verification methodologies, OVM and VMM, and the roadmap for these flows. Learn how and why industry-leading companies have either customized these flows or developed their own methodologies.

Speakers:
Janick Bergeron - *Synopsys, Inc., Mountain View, CA*
Faisal Haque - *Qualcomm, Inc., San Jose, CA*
Tom Fitzpatrick - *Mentor Graphics Corp., Groton, MA*

Free and open to ALL attendees!

45th Design Automation Conference / Anaheim, CA, June 8-13, 2008

Time ➡ 8:00 :15 :30 :45 9:00 10:00 11:00 12:00 1:00 2:00 3:00 4:00 5:00 6:00 7:00

Date ⬅ / Room(s) ➡

Sunday, June 8

- Collocated — MEMOCODE 2008 - Thursday, June 5 - Saturday, June 7 - Room 304B Meeting and 304C Lunch
- 209A — Workshop — 5th International UML for SoC Design Workshop: UML in Application - Rooms: 209A Meeting, 209B Lunch
- 208A — Workshop — High-level Synthesis: Back to the Future - Rooms: 208A Meeting, 208B Lunch
- 206B — Workshop — Low Power Coalition Workshop - Advances in Low Power Design for Circuits and Systems
- 204C — Collocated — 6th IEEE Symposium on Application Specific Processors - Rooms: 204C Meeting, 204B Lunch
- Anaheim Hilton — Collocated — GSRC
- 303B — Workshop — System and SoC Debug - Rooms: 303B Meeting, 303A Lunch
- 210AB — Workshop — Biochips to Interface and Monitor Human Biological Functions - Rooms: 210AB Meeting, 210C Lunch
- 303C — Workshop — Design and Verification of Low Power SoCs: An Application Oriented Approach
- Anaheim Hilton — Collocated — 7th Symposium on Electronic System-level Design with SystemC
- EDA Consortium Executive Reception, Anaheim Hilton Hotel Pacific Ballroom, 4:30-7:30pm

Monday, June 9

- 204C — Collocated — 6th IEEE Symposium on Application Specific Processors - Rooms: 204C Meeting, 204B Lunch
- 206B — Workshop — Introduction to Chips and EDA for a Non-Technical Audience
- 212A — Workshop — Cross-layer Power and Thermal Management - Rooms: 212A Meeting, 212B Lunch
- 205A — Workshop — Women in Design Automation: Networking, Negotiation, and Nonsense: Achieving Career Balance in an Unbalanced World - Rooms: 205A Meeting, 205B Lunch
- 208A — Workshop — 4th Integrated Design Systems Workshop - OpenAccess: A Platform for Continuous Evolution and Innovation - Rooms: 208A Meeting, 208B Lunch
- 303AB — Workshop — Diagnostic Services in Network-on-Chips (DSNOC) - Rooms: 303AB Meeting, 303C Lunch
- 207D — Workshop — Beyond Syntax and Semantics: Industry Experiences with OVL/SVA/PSL
- 204A — Collocated — IEEE International Workshop on Hardware-oriented Security and Trust (HOST-2008) - Rooms: 204A Meeting, 206A Lunch
- DAC Pavilion Booth #364 — Gary Smith on EDA: Trends and What's Hot at DAC
- DAC Pavilion Booth #364 — EDA Heritage Series: Maxwell's Legacy
- DAC Pavilion Booth #364 — Student Design Contest Award Presentation
- DAC Pavilion Booth #364 — Next Generation Data Centers: Environmentally Green, Financially Green
- DAC Pavilion Booth #364 — Today's Consumers: High Schoolers Spec Your Next Product
- DAC Pavilion Booth #364 — Will 22nm Be Our Catch-22?
- 210AB — Tutorial 1 — Bridging a Verification Gap: C++ to RTL for Practical Design
- 209AB — Tutorial 2 — Programming Massively Parallel Processors: The NVIDIA Experience
- 213D — HOTs — Elevating Confidence in Design IP Through Mutation-based Analysis Technology
- Ballroom ABC — HOTs — IP Validation for Macro and Embedded SoC
- Ballroom ABC — ACM Turing Award Winners
- Ballroom E — Collocated — 7th Symposium on Electronic System-level Design with SystemC
- Booth #2849 — Exhibitor Forum — Morning Sessions followed by 15min. Q&A period
- Booth #2849 — Exhibitor Forum — Afternoon Sessions followed by 15min. Q&A period

Tuesday, June 10

- 206AB — Session 1 — iDesign I: Flow Engineering for Physical Implementation: Theory and Practice — For Designers
- 207ABC — Session 2 — **SPECIAL SESSION:** Enabling Concurrency in EDA
- 208AB — Session 3 — CAD for FPGA
- 209AB — Session 4 — Analog Performance Modeling and Synthesis
- 210AB — Session 5 — Novel Techniques in Embedded Processor Design
- 210CD — Session 6 — **PANEL:** Electronics and Politics: What the Industry Needs from the Incoming US Administration
- Ballroom ABC — General Session and Keynote Address 8:30-10:15am
  EDA for Digital, Programmable, Multi-Radios
  Justin R. Rattner, Intel Senior Fellow, Vice President, Director, Corporate Technology Group and Chief Technology Officer, Intel Corp.
  
- LUNCH
- IEEE Council on EDA's Distinguished Speaker Lecture and Lunch 12:00 - 2:00pm Rm: 303AB
- DAC Pavilion Booth #364 — 45nm: Collaborate, Aggregate, Differentiate
- DAC Pavilion Booth #364 — EDA: A View From Sand Hill Road
- DAC Pavilion Booth #364 — Multi-processor SoCs: The Next Generation
- DAC Pavilion Booth #364 — IP Selection: The Good, The Bad, and The Ugly
- DAC Pavilion Booth #364 — EDA Globalization: Third World or New World?
- DAC Pavilion Booth #364 — Quality Versus Time to Market: The Unmentionable Tradeoff
- DAC Pavilion Booth #364 — SOI: Fact, Future and Fiction
- 212A — Workshop — Effective Technical Writing
- 213D — HOTs — Advanced Methodologies in Validating and Integrating High-speed Serial Interconnects in the Ultra Deep Sub-micron CMOS Era
- 204BC — Management Day — For Designers
- Booth #2849 — Exhibitor Forum — Morning Sessions followed by 15min. Q&A period
- Booth #2849 — Exhibitor Forum — Afternoon Sessions followed by 15min, Q&A period
- BREAK
- Session 7 — **SPECIAL SESSION:** Student Design Contest — For Designers
- Session 8A — **PANEL:** Reinventing EDA with Manycore Processors
- Session 8B — **PANEL:** Multi-core SoC Design is the Challenge! What is the Solution?
- Session 9 — Formal Verification Technology
- Session 10 — Layout Techniques for Modern Chip Designs
- Session 11 — Application Mapping and Power Efficiency
- Session 12 — Variation-aware Design
- Session 13 — iDesign II: SystemVerilog Implicit Port Enhancements... and Translation of an Existing VMM-based — For Designers
- Session 14 — Multi-core Simulation, Mixed-signal Power Optimization and Nanodevices
- Session 15 — Experiences and Advances in Formal and Dynamic Verification
- Session 16 — Emerging Nano/Biotechnologies
- Session 17 — Cache Optimization and Embedded Systems Modeling
- Session 18 — **PANEL:** ESL Hand-off: Fact or EDA Fiction? — For Designers
- SIGDA Ph.D. Forum and Member Meeting 6:00 - 7:30pm Room: 204 Foyer

Topic Area Legend:

- Synthesis and FPGA
- Business
- Interconnect and Reliability
- Analog/Mixed-signal/RF and Simulation
- Verification and Test
- Physical Design
- New and Emerging Technologies
- DFM and the Manufacturing Interface
- Wireless
- Strictly Design
- System-level and Embedded
- Low Power Design

45th Design Automation Conference / Anaheim, CA, June 8-13, 2008

Time ➡ 8:00 :15 :30 :45 9:00 10:00 11:00 12:00 1:00 2:00 3:00 4:00 5:00 6:00 7:00

⬅Date / Room(s)

Wednesday, June 11

206AB
Session 19 Analytical Modeling and Simulation of Complex Processing Systems

207ABC
Session 20 **SPECIAL SESSION:** Wild and Crazy Ideas

208AB
Session 21 **PANEL:** Next Generation Wireless - Multimedia Devices - Who is Up for the Challenge? For Designers

209AB
Session 22 Diagnosis and Debug

210AB
Session 23 Architectural and Precision Optimization in High-level Synthesis

210CD
Session 24 Extraction, Interconnect and Timing

DAC Pavilion Booth #364
Hogan's Heroes - Behavioral Synthesis: Is That Light at the End of the Tunnel an Oncoming Train?

213D Booth #2849
HOTs Integration, Test, Repair and Debug of Embedded Memory IP in an SoC
Exhibitor Forum Morning Sessions followed by 15min. Q&A period

LUNCH

Ballroom ABC
Keynote Address 11:15am - 12:15pm
Challenges on Design Complexities for Advanced Wireless Silicon Systems
Sanjay K. Jha, Chief Operating Officer, Qualcomm, Inc. and President, Qualcomm CDMA Technologies

Advanced Low Power Techniques: Is Your Design Method Too Powerful?

Session 25 Architectures for On-chip Communication
Session 26 **SPECIAL SESSION:** CMOS Gate Modeling for Timing, Noise, and Power: Rapidly Changing Paradigm
Session 27 Advanced Wireless Design For Designers
Session 28 Manufacturing Aware Design and Design Aware Manufacturing
Session 29 Advances in Sequential Optimization
Session 30 **PANEL:** Verifying Really Complex Systems: On Earth and Beyond

DFM Design Rules: Worth The Effort?

Designing the New-generation Wireless Platform: Lessons from iPhone and Android

HOTs What, Why and How: Using a Chip Prediction System to Find the Best IP Solution for Your Next Chip
Exhibitor Forum Afternoon Sessions followed by 15min. Q&A period

BREAK

Session 31 Beyond the Die - Packaging and Die Stacking
Session 32 **SPECIAL SESSION:** ESL Methodologies for Platform-based Synthesis For Designers
Session 33 **SPECIAL SESSION:** Wireless: Business Meets Technology For Designers
Session 34 Leakage Analysis and Optimization
Session 35 Design Methods for On-chip Communication
Session 36 **PANEL:** Keeping Hot Chips Cool: Are IC Thermal Problems Hot Air? For Designers

What's Holding Back Analog Design Automation?

45th DAC Party
7:30 - 10:00pm
Anaheim Marriott

Thursday, June 12

206AB
Session 37 New Advances in Logic Synthesis

207ABC
Session 38 **SPECIAL SESSION:** 3-D Semiconductor Integration and Packaging

208AB
Session 39 Statistical Timing Analysis

209AB
Session 40 Performance Driven Layout Optimization

210AB
Session 41 Power and Thermal Considerations in Single- and Multi-core Systems

210CD
Session 42 Multi-core Design Tools and Architectures

212A
Collocated NANOARCH'08: IEEE/ACM Symposium on Nanoscale Architectures - Rooms: 212A Meeting, 212B Lunch

DAC Pavilion Booth #364
Negotiating a Successful Career

Your Functional Verification Roadmap: OVM, VMM or Roll Your Own?

213D
HOTs Hardened DDR PHY Integration

303A

LUNCH

Ballroom ABC
DAC Best Paper Presentation and Keynote Address 12:45 - 1:45pm
Idea to Implementation: A Different Perspective on System Design
Jack Little, President and Co-Founder, The MathWorks, Inc.

Session 43 Reconfigurable Architecture Optimizations
Session 44 **SPECIAL SESSION:** Formal Verification: Dude or Dud? Experiences from the Trenches For Designers
Session 45 Random Topics in Testing
Session 46 Securing and Debugging Embedded Systems
Session 47 Topics in Power and Thermal Management
Session 48 **PANEL:** DFM in Practice: Hit or Hype For Designers

Workshop Maximizing Efficiency in the Development Cycle

BREAK

Session 49 Physical Effects of Variability
Session 50 Soft Error in Scaled CMOS Design
Session 51 Advances in Verification of Abstract (pre RTL) Models
Session 52 Design Space Exploration
Session 53 Noise Reliability Enhancement
Session 54 **PANEL:** Custom is from Mars and Synthesis from Venus For Designers

Friday, June 13

208AB
Tutorial 3 Robust Analog Mixed-signal Design

210AB
Tutorial 4 DFM Revisited: A Comprehensive Analysis of Variability at All Levels of Abstraction

209AB
Tutorial 5 Low Power Techniques for SoC Design

210CD
Tutorial 6 System-level Design for Embedded Systems

212A
Collocated NANOARCH'08: IEEE/ACM Symposium on Nanoscale Architectures - Rooms: 212A Meeting, 212B Lunch

Topic Area Legend:

- Synthesis and FPGA
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- DFM and the Manufacturing Interface
- Wireless
- Strictly Design
- System-level and Embedded
- Low Power Design

General Session/Keynote Address

TUESDAY, JUNE 10 / 8:30 - 10:15AM

RM: BALLROOM ABC

Opening Remarks - Limor Fix - 45th DAC General Chair

Awards/Scholarships

- A. Richard Newton Graduate Scholarships
- Marie R. Pistilli Women in EDA Achievement Award
- P.O. Pistilli Undergraduate Scholarships for Advancement in Computer Science and Electrical Engineering
- 2007 Phil Kaufman Award for Distinguished Contributions to EDA
- 2008 IEEE Emanuel R. Piore Award
- 2008 IEEE Fellow
- ACM Turing Award
- ACM Fellow
- Outstanding Contribution to ACM Award
- SIGDA Distinguished Service Award
- SIGDA Outstanding New Faculty Award
- ACM Transactions on Design Automation of Electronic Systems (TODAES) 2008 Best Paper Award

Keynote Address

EDA for Digital, Programmable, Multi-radios

Justin R. Rattner - *Intel Senior Fellow, Vice President, Director, Corporate Technology Group and Chief Technology Officer, Intel Corp., Hillsboro, OR*

iDESIGN I

Chair:
David Reda - *Synopsys, Inc., Irvine, CA*
Organizer:
Leon Stok - *IBM Corp., Hopewell Junction, NY*

EDA tools are never used in isolation. Rather, multiple tools are combined into a sequence called a "flow". Furthermore an elaborate infrastructure is required to support and enable flow execution. This "flow infrastructure" includes directory organization, configuration management, compute servers, desktop machines, job control, license administration, dependency management, operating systems, team communication, error reporting, and libraries of all sorts. Oh, and of course the EDA tools themselves. While EDA tools come with documentation and user guides, and many of the components of the flow infrastructure have standalone documentation, there is virtually no manual or reference guide or checklist available to aid in the creation and improvement of a flow. Join two veteran consultants, each with over 20 years experience in IC design, as we discuss the theory and practice of "flow engineering", the design of "flow infrastructure and the flows themselves.

1.1 Flow Engineering for Physical Implementation: Theory and Practice

Steve Golson - *Trilobyte Systems, Carlisle, MA*
Pete Churchill - *EdgeRate Consulting, Hillsborough, NC*

SPECIAL SESSION: ENABLING CONCURRENCY IN EDA

Chair:
Patrick Madden - *Binghamton Univ., NY*
Organizer:
Eli Chiprout - *Intel Corp., Hillsboro, OR*

The effort to parallelize applications has been a difficult problem for many years. However, new directions in hardware, compiler technology, and software methods have forced us to take a new look at the problem. With increasing size of our designs and with higher demand for faster turnaround time there is also a demand-side motivation for enabling EDA to take advantage of multi-core and parallel processing. This session will give some fresh perspective on how EDA should be thinking about the problem. The first talk will address new parallel mechanism that are enabled for GPUs and an example application on sparse matrices. The second talk will discuss what has been learned in parallel computing and what is being enabled in multi-core systems to address past mistakes. The third talk will prepare us for the radical changes that are coming to CAD due to the availability of multi-core systems.

2.1 Sparse Matrix Computation on Manycore GPUs

Michael Garland - *NVIDIA Corp., Urbana-Champaign, Urbana, IL*

2.2 Parallel Computing Technology: Can We PLEASE Do It Right This Time?

Michael Wrinn - *Intel Corp., Hillsboro, OR*
Timothy Mattson - *Intel Corp., Dupont, WA*

2.3 Parallelizing CAD: A Timely Research Agenda for EDA

Kurt Keutzer, Bryan Catanzaro, Bor-Yiing Su - *Univ. of California, Berkeley, CA*

CAD FOR FPGA

Chair:
Yegna Parasuram - *Mentor Graphics Corp., San Jose, CA*

This session presents advances in CAD for FPGAs. The first paper presents a novel approach to synthesis of XOR-based logic. The second paper reduces netlist area by using multi-output function based sequential resynthesis. The third paper uses a network flow model to minimize power in embedded memory mapping. The final paper improves VPR's timing results by incrementally updating slack and criticality.

3.1 Functionally Linear Decomposition and Synthesis of Logic Circuits for FPGAs

Tomasz S. Czajkowski, Stephen D. Brown - *Univ. of Toronto, Toronto, ON, Canada*

3.2 FPGA Area Reduction by Multi-output Function Based Sequential Resynthesis

Yu Hu, Victor Shih, Rupak Majumdar, Lei He - *Univ. of California, Los Angeles, CA*

3.3s A Generalized Network Flow Based Algorithm for Power-aware FPGA Memory Mapping

Tien-Yuan Hsu, Ting-Chi Wang - *National Tsing Hua Univ., Hsinchu, Taiwan*

3.4s Enhancing Timing-driven FPGA Placement for Pipelined Netlists

Ken Eguro, Scott Hauck - *Univ. of Washington, Seattle, WA*

TOPIC AREA: STRICTLY DESIGN

TOPIC AREA: SYSTEM-LEVEL AND EMBEDDED

TOPIC AREA: SYNTHESIS AND FPGA

s - indicates short paper

SESSION 4 RM: 209AB

ANALOG PERFORMANCE MODELING AND SYNTHESIS

Chair:
Peng Li - *Texas A&M Univ., College Station, TX*

The first paper in the session presents an innovative response surface modeling technique that is very efficient when the dimension of the parameter space is very large. The second paper presents an analog topology synthesis methodology based on a genetic programming formulation that does not require an initial building block library and produces designer-recognizable circuit topologies. The third paper is on a placement methodology for analog circuits that takes into account hierarchical matching, symmetry and proximity constraints simultaneously.

4.1 Statistical Regression for Efficient High-dimensional Modeling of Analog and Mixed-signal Performance Variations
Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*
Hongzhou Liu - *Cadence Design Systems, Inc., Pittsburgh, PA*

4.2 Topology Synthesis of Analog Circuits Based on Adaptively Generated Building Blocks
Angan Das, Ranga Vemuri - *Univ. of Cincinnati, Cincinnati, OH*

4.3 Analog Placement Based on Hierarchical Module Clustering
Po-Hung Lin - *National Taiwan Univ., Taipei, Taiwan*
Shyh-Chang Lin - *SpringSoft, Inc., Hsinchu, Taiwan*

TOPIC AREA: ANALOG/MIXED-SIGNAL/RF AND SIMULATION

SESSION 5 RM: 210AB

NOVEL TECHNIQUES IN EMBEDDED PROCESSOR DESIGN

Chair:
Pai Chou - *Univ. of California, Irvine, CA*

This session presents advanced topics for the design of highly-optimized embedded processors. The first paper presents a new concept that is capable of dynamically transmuting its instruction set for an application specific reconfigurable processor. The second paper presents a novel algorithm to optimize an application specific floating-point unit by sharing floating point datapaths with variable bit-widths. The third paper presents an adaptive resource resizing scheme that can improve processing performance and energy efficiency simultaneously. The last paper presents an architecture design example of a VoIP codec using a C-based design flow.

5.1 Run-time Instruction Set Selection in a Transmutable Embedded Processor
Lars Bauer, Muhammad Shafique, Jörg Henkel - *Univ. of Karlsruhe, Karlsruhe, Germany*

5.2 Rapid Application Specific Floating-point Unit Generation with Bit-alignment
Yee Jern Chong, Sridevan Parameswaran - *Univ. of New South Wales, Sydney, Australia*

5.3s Dynamic Register File Resizing to Improve Embedded Processor Performance and Energy-delay Efficiency
Houman Homayoun, Sudeep Pasricha, Mohammad Makhzan, Alexander V. Veidenbaum - *Univ. of California, Irvine, CA*

5.4s C-based Design Flow: A Case Study on G.729A for Voice over Internet Protocol (VoIP)
Mehrdad Reshadi, Bita Gorjiara, Daniel D. Gajski - *Univ. of California, Irvine, CA*

TOPIC AREA: SYSTEM-LEVEL AND EMBEDDED

SESSION 6 RM: 210CD

PANEL: ELECTRONICS AND POLITICS: WHAT THE INDUSTRY NEEDS FROM THE INCOMING US ADMINISTRATION

Chair:
Pete Weitzner - *Chapman Univ., Orange, CA*
Organizer:
Tiffany Sparks - *Chartered Semiconductor Manufacturing, Milpitas, CA*

It's election time again and the US is about to see a new administration come into power. This could include a new party, and the US could elect the first woman or first African-American president. Closer to the DAC population, this election could be crucial for the Electronics Industry for any number of business or technology reasons. What, then, is going to be the most important platform to help boost the flagging technology sector? Where does the tech sector want the new administration to focus?

- Revising outsourcing policies
- Reducing visa restrictions
- Eliminating Sarbanes-Oxley and offering more tax incentives for startups
- Nationalized Health Care
- A reinvigorated technical program to recapture interest in science, similar to the space race in the 1960s
- Focus on math and science programs for middle and high schools
- Investing in more DARPA-like programs to promote research, innovation and new ideas to stimulate the economic growth engine

Panelists will debate which initiatives are most important for the DAC community and what changes candidates are talking about.

Panelists:
Luc Burgun - *EVE, Palaiseau, France*
Todd Cutler - *Agilent Tech., Inc., Santa Clara, CA*
Vicki Hadfield - *SEMI North America, Washington, DC*
Russell Lefevre - *IEEE, Washington, DC*
Clayton Parker - *Magma Design Automation, Inc., San Jose, CA*
Chris Rowen - *Tensilica, Inc., Santa Clara, CA*

TOPIC AREA: BUSINESS

s - indicates short paper

SESSION 7 FOR DESIGNERS RM: 206AB

SPECIAL SESSION: STUDENT DESIGN CONTEST

Chair:
Byunghoo Jung - *Purdue Univ., West Lafayette, IN*

Out of 47 papers submitted to the Student Design Contest, 8 papers demonstrating excellence in their design solutions and methodology have been invited to the Student Design Contest special session. The papers address important issues in a wide range of technologies: media processing, sensors, vision processing, microprocessor, FPGA, memory, and wireless.

7.1 A 242mW, 10mm² 1080p H.264/AVC High Profile Encoder Chip
Yu-Kun Lin, **De-Wei Li, Chia-Chun Lin, Tzu-Yun Kuo, Sian-Jin Wu, Wei-Cheng Tai, Wei-Cheng Chang, Tian-Sheuan Chang** - *National Chaio Tung Univ., Hsinchu, Taiwan*

7.2 The Design of a Low Power Carbon Nanotube Chemical Sensor System
Taeg Sang Cho, **Kyeong-Jae Lee, Jing Kong, Anantha P. Chandrakasan** - *Massachusetts Institute of Tech., Cambridge, MA*

7.3 iVisual: An Intelligent Visual Sensor SoC with 2790fps CMOS Image Sensor and 205GOPS/W Vision Processor
Chih-Chi Cheng, **Chia-Hua Lin, Chung-Te Li, Liang-Gee Chen** - *National Taiwan Univ., Taipei, Taiwan*
Samuel C. Chang - *Massachusetts Institute of Tech., Cambridge, MA*

7.4 Vision Platform for Mobile Intelligent Robots Based on 81.6 GOPS Object Recognition Processor
Donghyun Kim, **Kwanho Kim, Joo-Young Kim, Seungjin Lee, Hoi-Jun Yoo** - *KAIST, Daejeon, Republic of Korea*

7.5 A MIPS R2000 Implementation
Nathaniel Pinckney, **Thomas Barr, Michael Dayringer, Matthew McKnett, Nan Jiang, Carl Nygaard, David M. Harris** - *Harvey Mudd College, Claremont, CA*
Joel Stanley, Braden Phillips - *Univ. of Adelaide, Australia*

7.6 Process Variation Tolerant SRAM Design for Ultra Low Voltage Applications
Jaydeep P. Kulkarni, **Sang Phill Park, Kaushik Roy** - *Purdue Univ., West Lafayette, IN*
Keejong Kim - *Broadcom, Inc., Tempe, AZ*

7.7 PicoCube: A 1cm3 Sensor Node Powered by Harvested Energy
Yuen-Hui Chee, **Mike Seeman**, **Mike Koplow, Michael Mark, Nathan Pletcher, Dan Steingart, Fred Burghardt, Jan Rabaey, Paul Wright, Seth Sanders** - *Univ. of California, Berkeley, CA*

7.8 An 8x8 Run-time Reconfigurable FPGA Embedded in a SoC
Sumanta Chaudhuri, **Sylvain Guilley, Florent Flament, Philippe Hoogvorst, Jean-Luc Danger** - *Ecole Nationale Supérieure des Télécommunications, Paris, France*

SESSION 8A RM: 207ABC

PANEL: REINVENTING EDA WITH MANYCORE PROCESSORS

Chair: Kurt Keutzer - *Univ. of California, Berkeley, CA*
Organizers: Eshel Haritan - *CoWare, Inc., San Jose, CA*
Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

Multi-core processors are becoming increasingly widespread, providing the potential for parallelizing applications for improved computational efficiency. In the EDA domain, this raises a number of intriguing possibilities, as new approaches and algorithms can be used to exploit these platforms. Does programming on multi-core processors require a fundamental rethink and a new programming mindset? How can EDA applications most effectively exploit multi-core processors? Where does the low-hanging fruit lie? What tasks are the most amenable to parallelization? Can anything be parallelized? Where does Amdahl's law begin to play a role in limiting the gains of multi-core systems? The assembled panel will provide insights into questions such as this.

Panelists:
Anirudh Devgan - *Magma Design Automation, Inc., Austin, TX*
Desmond Kirkpatrick - *Intel Corp., Hillsboro, OR*
Steve Meier - *Synopsys, Inc., Mountain View, CA*
Duaine Pryor - *Mentor Graphics Corp., San Jose, CA*
Tom Spyrou - *Cadence Design Systems, Inc., San Jose, CA*

SESSION 8B RM: 207ABC

PANEL: MULTI-CORE SoC DESIGN IS THE CHALLENGE! WHAT IS THE SOLUTION?

Chair:
Wayne Wolf - *Georgia Institute of Tech., Atlanta , GA*
Organizers:
Hiroyuki Yagi - *STARC, Shin-Yokohama, Japan*
Eshel Haritan - *CoWare, Inc., San Jose, CA*

Multi-core SoC are being designed today. Multi-core SoC design can help achieve many aggressive performance and low power targets but it creates new design challenges which will be discussed in this panel.

Panelists:
Toshihiro Hattori - *Renesas Tech. Corp., Tokyo, Japan*
Pierre Paulin - *STMicroelectronics, Ottawa, ON, Canada*
Mike Muller - *ARM, Cambridge, United Kingdom*
Achim Nohl - *CoWare, Inc., Aachen, Germany*
Drew Wingard - *Sonics, Inc., Milpitas, CA*

SESSION 9 RM: 208AB

FORMAL VERIFICATION TECHNOLOGY

Chair:
Ziyad Hanna - *Jasper Design Automation, Inc., Mountain View, CA*

A core challenge with formal verification is always scalability to large designs. This session presents four papers that advance the state-of-the-art in formal verification technology, making formal verification tools more efficient and usable.

9.1 Compositional Verification of Retiming and Sequential Optimizations
In-Ho Moon - *Synopsys, Inc., Hillsboro, OR*

9.2 Tunneling and Slicing: Towards Scalable BMC
Malay Ganai, **Aarti Gupta** - *NEC Labs America, Princeton, NJ*

9.3 Optimizing Automatic Abstraction Refinement for Generalized Symbolic Trajectory Evaluation
Yan Chen, **Fei Xie** - *Portland State Univ., OR*
Jin Yang - *Intel Corp., Hillsboro, OR*

9.4 Faster Symmetry Discovery using Sparsity of Symmetries
Paul T. Darga, **Karem A. Sakallah, Igor L. Markov** - *Univ. of Michigan, Ann Arbor, MI*

TOPIC AREA: STRICTLY DESIGN | TOPIC AREA: SYSTEM-LEVEL AND EMBEDDED | TOPIC AREA: VERIFICATION AND TEST

s - indicates short paper

SESSION 10 RM: 209AB

LAYOUT TECHNIQUES FOR MODERN CHIP DESIGNS

Chair:
Ting-Chi Wang - *National Tsing Hua Univ., Hsinchu, Taiwan*

This session addresses novel partitioning, floorplanning, and placement techniques for modern chip designs. The first paper presents an application-driven, floorplan-aware algorithm for voltage partitioning and island creation. The second paper presents a high-quality fixed-outline floorplanner based on a deferred decision making principle. The third paper proposes a routability-driven analytical placer for mixed-size designs based on a new net overlapping removal formulation. The last paper presents a clique-partitioning technique for broadcast addressing of pin-constrained digital microfluidic biochips.

10.1 Application-driven Floorplan-aware Voltage Island Design
Dipanjan Sengupta, Resve Saleh - *Univ. of British Columbia, Vancouver, British Columbia, Canada*

10.2 * DeFer: Deferred Decision Making Enabled Fixed-outline Floorplanner
Jackey Z. Yan, Chris Chu - *Iowa State Univ., Ames, IA*

10.3 Routability-driven Analytical Placement by Net Overlapping Removal for Large-scale Mixed-size Designs
Zhe-Wei Jiang, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*
Bor-Yiing Su - *Univ. of California, Berkeley, CA*

10.4 Broadcast Electrode-addressing for Pin-constrained Multi-functional Digital Microfluidic Biochips
Tao Xu, Krishnendu Chakrabarty - *Duke Univ., Durham, NC*

TOPIC AREA: PHYSICAL DESIGN

SESSION 11 RM: 210AB

APPLICATION MAPPING AND POWER EFFICIENCY

Chair:
Luca Carloni - *Columbia Univ., New York, NY*

This session advances state-of-the-art in tools for embedded designs. In the area of power optimization, new approaches to off-line scheduling of dynamic voltage scaling and software partitioning enable significant power savings. For real-time power aware design, a feedback control mechanism shows a new way to dynamically adjust power for even more savings. Finally, in the area of application mapping for generation of processor accelerators, a new automation technique delivers impressive results. In short, the three long and two short papers in this session present significant new advances in mapping and power efficiency for applications running in embedded hardware and software.

11.1* Optimality and Improvement of Dynamic Voltage Scaling Algorithms for Multimedia Applications
Zhen Cao, Brian Foo, Lei He, Mihaela van der Schaar - *Univ. of California, Los Angeles, CA*

11.2 Feedback Controlled Reliability-aware Power Management for Real-time Embedded Systems
Ranjani Sridharan, Nikhil Gupta, Rabi N. Mahapatra - *Texas A&M Univ., College Station, TX*

11.3 Energy Optimal Software Partitioning in Heterogeneous Multiprocessor Embedded Systems
Michel Goraczko, Jie Liu, Bodhi Priyantha, Feng Zhao - *Microsoft Corp., Redmond, WA*
Dimitrios Lymberopoulos - *Yale Univ., New Haven, CT*
Slobodan Matic - *Univ. of California, Berkeley, CA*

11.4s Customizing Computation Accelerators for Extensible Multi-issue Processors with Effective Optimization Techniques
Ya-Shuai Lü, Li Shen, Li-Bo Huang, Zhi-Ying Wang, Nong Xiao - *National Univ. of Defense Tech., Changsha, Hunan, China*

11.5s An Automatic Scratch Pad Memory Management Tool and MPEG-4 Encoder Case Study
Rogier Baert, Eddy De Greef, Erik Brockmeyer, Geert Vanmeerbeeck, Prabhat Avasare, Jean-Yves Mignolet, Miroslav Cupak - *IMEC, Leuven, Belgium*

TOPIC AREA: SYSTEM-LEVEL AND EMBEDDED

SESSION 12 RM: 210CD

VARIATION-AWARE DESIGN

Chair:
Masanori Hashimoto - *Osaka Univ., Osaka, Japan*

Coping with variation is a critical concern in recent designs, and this session discusses how to take variation into consideration. The first paper predicts speedpaths based on machine-learning. The second paper improves performance of pipelined circuits by inserting delay sensors and programmable delay elements. The third paper presents a methodology for statistical simulation of SRAM read access yield. The fourth paper proposes a clock skew scheduling methodology for timing yield considering non-Gaussian distribution. The last paper gives a statistical current source based cell model.

12.1 A Methodology for Statistical Estimation of Read Access Yield in SRAMs
Mohamed H. Abu-Rahma, Kinshuk Chowdhury, Joseph Wang, Zhiqin Chen, Sei Seung Yoon - *Qualcomm, Inc., San Diego, CA*
Mohab Anis - *Univ. of Waterloo, Waterloo, ON, Canada*

12.2 Automated Design of Self-adjusting Pipelines
Jieyi Long, Seda Ogrenci Memik - *Northwestern Univ., Evanston, IL*

12.3* Speedpath Prediction Based on Learning From a Small Set of Examples
Pouria Bastani, Li-C. Wang - *Univ. of California, Santa Barbara, CA*
Kip Killpack, Eli Chiprout - *Intel Corp., Hillsboro, OR*

12.4s Timing Yield Driven Clock Skew Scheduling Considering Non-Gaussian Distributions of Critical Path Delays
Yi Wang, Wai-Shing Luk, Xuan Zeng, Jun Tao, Changhao Yan, Jiarong Tong - *Fudan Univ., Shanghai, China*
Wei Cai - *Univ. of North Carolina, Charlotte, NC*
Jia Ni - *Fudan Univ., Shanghai, China*

12.5s Statistical Waveform and Current Source Based Standard Cell Models for Accurate Timing Analysis
Amit Goel, Sarma Vrudhula - *Arizona State Univ., Tempe, AZ*

TOPIC AREA: DFM AND THE MANUFACTURING INTERFACE

* indicates Best Paper Candidate

s - indicates short paper

SESSION 13 — FOR DESIGNERS — RM: 206AB

iDESIGN II

Chair:
Ali El-Zein - *IBM Corp., Austin, TX*
Organizer:
Leon Stok - *IBM Corp., Hopewell Junction, NY*

This iDesign session addresses practical aspects of designing using SystemVerilog. Experienced design consultants and users will give extensive examples on how to capitalize on several of the language features and unlayer the intimacies of the class libraries built on top of SystemVerilog. The first presentation addresses the new implicit port instantiation enhancements that help accelerate top-level composition of large ASIC and FPGA Designs. The second presentation focuses on the class libraries in SystemVerilog that enhance productivity. Both the VMM on OVM methodologies will be discussed and important differences pointed out. It will be described how to convert between the two, where this is straight forward and which aspects require more attention.

13.1 SystemVerilog Implicit Port Enhancements Accelerate System Design and Verification
Cliff Cummings - *Sunburst Designs, Inc., Beaverton, OR*

13.2 Translation of an Existing VMM-based SystemVerilog Testbench to OVM
Kelly Larson - *MediaTek, Inc., Austin, TX*

SESSION 14 — RM: 207ABC

MULTI-CORE SIMULATION, MIXED-SIGNAL POWER OPTIMIZATION AND NANODEVICES

Chair:
Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*

The first paper in the session is an excellent and timely contribution in the important area of fast, high-accuracy transient simulation of large mixed-signal circuits. The authors present extensions of classical time-integration methods that take fundamental advantage of multi-threading at the numerical discretization level, achieving more than 2x speedups on a 4-core machine. The second paper describes a discrete optimization technique for power tradeoffs between digital and analog sections of ADCS. The third paper presents a compact model with capacitances for CNFETS.

14.1* WavePipe: Parallel Transient Simulation of Analog and Digital Circuits on Multi-core Shared-memory Machines
Wei Dong, Peng Li, Xiaoji Ye - *Texas A&M Univ., College Station, TX*

14.2 The Mixed Signal Optimum Energy Point: Voltage and Parallelism
Brian P. Ginsburg - *Texas Instruments, Inc., Dallas, TX*
Anantha P. Chandrakasan - *Massachusetts Institute of Tech., Cambridge, MA*

14.3 Analysis and Implications of Parasitic and Screening Effects on the High-frequency/RF Performance of Tunneling-carbon Nanotube FETs
Chaitanya U. Kshirsagar, Mohamed N. ElZeftawi, Kaustav Banerjee - *Univ. of California, Santa Barbara, CA*

SESSION 15 — RM: 208AB

EXPERIENCES AND ADVANCES IN FORMAL AND DYNAMIC VERIFICATION

Chair:
Maruthy Vedam - *Qualcomm, Inc., San Diego, CA*

In the first paper in this session, a methodology is presented for identifying challenging parts of a design and improving their verifiability. The second paper introduces a method for compressing test cases based on machine learning with the hope of improving the speed of coverage convergence. In the third paper, the authors present their experience of applying assertion-based verification to a microprocessor. The fourth and final paper suggests to pipeline emulation to speed up dynamic verification.

15.1 Assertion Based Verification of a 32 Thread SPARC CMT Microprocessor
Babu Turumella, Mukesh Sharma - *Sun Microsystems, Inc., Santa Clara, CA*

15.2 Functional Test Selection Based on Unsupervised Support Vector Analysis
Onur Guzey, Li-C. Wang - *Univ. of California, Santa Barbara, CA*
Jeremy Levitt - *Mentor Graphics Corp., San Jose, CA*
Harry Foster - *Mentor Graphics Corp., Addison, TX*

15.3s Early Formal Verification of Conditional Coverage Points to Identify Intrinsically Hard-to-verify Logic
C. Richard Ho - *D. E. Shaw Research, Cupertino, CA*
Michael Theobald, Martin M. Deneroff, Ron O. Dror, Joseph Gagliardo, David E. Shaw - *D. E. Shaw Research, New York, NY*

TOPIC AREA: STRICTLY DESIGN

TOPIC AREA: ANALOG/MIXED-SIGNAL/RF AND SIMULATION

TOPIC AREA: VERIFICATION AND TEST

s - indicates short paper

* indicates Best Paper Candidate

SESSION 16 — RM: 209AB

EMERGING NANO/BIOTECHNOLOGIES

Chair:
Subhasish Mitra - *Stanford Univ., Palo Alto, CA*

This session features three exciting papers on emerging nano/biotechnology topics. The first paper addresses performance and reliability analysis of logic circuits using graphene nanoribbon FETs. The second paper discusses a memory structure based on magnetoresistive RAMs. The final paper in this session presents a novel droplet-routing method for microfluidic biochips.

16.1 Technology Exploration for Graphene Nanoribbon FETs
Mihir Choudhury, Kartik Mohanram - *Rice Univ., Houston, TX*
Youngki Yoon, Jing Guo - *Univ. of Florida, Gainesville, FL*

16.2 Modeling of Failure Probability and Statistical Design of Spin-torque Transfer Magnetic Random Access Memory (STT MRAM) Array for Yield Enhancement
Jing Li, Charles Augustine, Sayeef Salahuddin, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

16.3 A Progressive-ILP Based Routing Algorithm for Cross-referencing Biochips
Ping-Hung Yuh, Chia-Lin Yang, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*
Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

TOPIC AREA: NEW AND EMERGING TECHNOLOGIES

SESSION 17 — RM: 210AB

CACHE OPTIMIZATION AND EMBEDDED SYSTEMS MODELING

Chair:
Stylianos Mamagkakis - *Interuniversity Micro-Electronics Center, Leuven, Belgium*

Predicting and optimizing performance is a key issue in embedded system design. CPUs, memory hierarchies and interconnects are critical components in this regard. Concerning the interconnects, one paper presents an analysis of latencies in real-time embedded system with clock drifts. With respect to CPUs and caches, this session presents an efficient simulator that times both components. Caches are also considered in two other papers. One paper presents a new caching technique for high-performance embedded systems, and another paper discusses how cache locking and partitioning can be used to make shared caches on multi-core chips more predictable.

17.1 High-performance Timing Simulation of Embedded Software
Jürgen Schnerr, Oliver Bringmann, Alexander Viehl - *Forschungszentrum Informatik, Karlsruhe, Germany*
Wolfgang Rosenstiel - *Univ. of Tübingen, Tübingen, Tübingen, Germany*

17.2s Model Checking Based Analysis of End-to-end Latency in Embedded, Real-time Systems with Clock Drifts
Swarup Mohalik, A. C. Rajeev, Manoj G. Dixit, S. Ramesh - *General Motors Corp., Bangalore, India*
P. Vijay Suman, Paritosh K. Pandya - *Tata Institute of Fundamental Research, Mumbai, India*
Shengbing Jiang - *General Motors Corp., Warren, MI*

17.3s Exploring Locking and Partitioning for Predictable Shared Caches on Multi-cores
Vivy Suhendra, Tulika Mitra - *National Univ. of Singapore, Singapore*

17.4 Miss Reduction in Embedded Processors Through Dynamic, Power-friendly Cache Design
Garo Bournoutian, Alex Orailoglu - *Univ. of California, San Diego, La Jolla, CA*

TOPIC AREA: SYSTEM-LEVEL AND EMBEDDED

SESSION 18 — FOR DESIGNERS — RM: 210CD

PANEL: ESL HAND-OFF: FACT OR EDA FICTION?

Chair:
Gary Smith - *Gary Smith EDA, Santa Clara, CA*
Organizers:
Hiroyuki Yagi - *STARC, Shin-Yokohama, Japan*
Eshel Haritan - *CoWare, Inc., San Jose, CA*

Moving up in the level of abstraction is the holy grail of EDA. Each transition to the next level of abstraction allows 100X improvement in simulation speed and 100X improvement in design productivity. ESL is being promoted as the next level above RTL but is it really happening? The questions this panel is going to address are: What is exactly ESL? What can be automated? Is ESL a new design entry level? What are the benefits of the new entry level? Why don't we see wide adoption by HW designers? Did we find another way to gain productivity? Is ESL finally enabling IP reuse? Are we going to see a transition from RTL signoff to ESL signoff? What does ESL signoff mean? Can ESL address the design of convergent (multiple) applications? Controversy: Do we really need the new ESL tools or are current RTL-based tools sufficient? If not ESL then what are the new methodologies/tools/languages required to move to the next level of productivity? Is ESL signoff the next step in design? Is there a common formalism/abstraction that captures ESL? Is it possible?

Panelists:

Nikil Dutt - *Univ. of California, Irvine, CA*
Tim Kogel - *CoWare, Inc., Aachen, Germany*
Giovanni Mancini - *The MathWorks, Inc., Natick, MA*
Michael McNamara - *Cadence Design Systems, Inc., San Jose, CA*
Wolfgang Roesner - *IBM Corp., Austin, TX*
Hidekazu Tangi - *Sony Corp., Kanagawa, Japan*

TOPIC AREA: SYSTEM-LEVEL AND EMBEDDED

s - indicates short paper

SESSION 19

ANALYTICAL MODELING AND SIMULATION OF COMPLEX PROCESSING SYSTEMS

Chair:
Luciano Lavagno - *Politecnico di Torino, Torino, Italy*

The first paper proposes a model to characterize throughput of chip-multiprocessors with frequency islands and uses it to evaluate the variability tolerance of given designs. The second paper presents a probabilistic model of instruction cache to statically analyze execution time. The second half of the session proposes methods to improve simulation speed of software code, where the first paper combines instruction-set simulation with native simulation using trace recording, and the second paper parallelizes synchronous dataflow graphs.

19.1 * Characterizing Chip-multiprocessor Variability-tolerance
Sebastian X. Herbert, Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh , PA*

19.2 Cache Modeling in Probabilistic Execution Time Analysis
Yun Liang, Tulika Mitra - *National Univ. of Singapore, Singapore*

19.3 Multiprocessor Performance Estimation Using Hybrid Simulation
Lei Gao, Kingshuk Karuri, Stefan Kraemer, Rainer Leupers, Gerd Ascheid, Heinrich Meyr - *RWTH Aachen Univ., Germany*

19.4 Multithreaded Simulation for Synchronous Dataflow Graphs
Chia-Jui Hsu, José Luis Pino - *Agilent Tech., Inc., Westlake Village, CA*
Shuvra S. Bhattacharyya - *Univ. of Maryland, College Park, MD*

SESSION 20

SPECIAL SESSION: WILD AND CRAZY IDEAS

Chair:
Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

What is wackier than last year's WACI? This year's WACI! The WACI session is full of Wild And Crazy Ideas, intended to stimulate discussion. The WACI session provides ideas that appear to be promising and thought-provoking, but are not fully developed to the point of full papers. There will be a small award for the WAClest question!

20.1 Design of a Mask-programmable Memory/Multiplier Array Using G4-FET Technology
Jay B. Brockman, Peter Kogge, Sheng Li, Amit Kashyap - *Univ. of Notre Dame, IN*
Mohammad Mojarradi - *NASA, Pasadena, CA*

20.2 Programmable Logic Circuits Based on Ambipolar CNFET
David Atienza - *DACYA, Madrid, Spain*
Haykel Ben Jamaa, Yusef Leblebici, Giovanni De Micheli - *École Polytéchnique Fédérale de Lausanne, Lausanne, Switzerland*

20.3 Analog Parallelism in Ring-based VCOs
Daeik Kim, Choongyeun Cho - *IBM Corp., Hopewell Junction, NY*
Jonghae Kim - *Qualcomm, Inc., San Diego, CA*

20.4 Techniques for Fully Integrated Intra-/Inter-chip Optical Communication
Edoardo Charbon, Claudio Favi - *École Polytéchnique Fédérale de Lausanne, Lausanne, Switzerland*

20.5 How to Let Instruction Set Processor Beat ASIC for Low Power Wireless Baseband Implementation: A System-level Approach
Min Li, Bruno Bougard, David Novo, Liesbet Van Der Perre, Francky Catthoor - *IMEC, Leuven, Belgium*

20.6 Bounded Lifetime Integrated Circuits
Puneet Gupta - *Univ. of California, Los Angeles, CA*
Andrew B. Kahng - *Univ. of California, San Diego, La Jolla, CA*

20.7 Collective Computing Based On Swarm Intelligence
Seetharam Narasimhan, Somnath Paul, Swarup Bhunia - *Case Western Reserve Univ., Cleveland, OH*

20.8 (Bio)-Behavioral CAD
Farinaz Koushanfar - *Rice Univ., Houston, TX*
Miodrag Potkonjak - *Univ. of California, Los Angeles, CA*

SESSION 21 FOR DESIGNERS

PANEL: NEXT GENERATION WIRELESS-MULTIMEDIA DEVICES - WHO IS UP FOR THE CHALLENGE?

Chair:
Jan Rabaey - *Univ. of California, Berkeley, CA*
Organizers:
Andreas Kuehlmann - *Cadence Design Systems, Inc., Berkeley, CA*
Juan Rey - *Mentor Graphics Corp., San Jose, CA,*

Yesterday's cell phones have rapidly evolved into versatile multi-media computers heavily loaded with a wide spectrum of technologies to support many functions and use modes. Designing and verifying such complex devices becomes increasingly challenging. Some of the main drivers are: Increasing number of functions and highly diverse use modes Increasing bandwidth Low power and high reliability Use of multimedia devices with high resolution and new methods for user interactions Convergence of wireless radio algorithms Lots of functionality moving into SW Controversy - some sample questions: Are we seeing a convergence of HW and low-level SW "platforms" with the differentiator being in SW applications or will HW remain core of the competitive edge? If platforms are the future, will we see an emergence of horizontal businesses splitting HW, from OS layer, from applications Will verification remain a "mixed bag" of methods and tools or will a more holistic approach be required to be successful?

Panelists:
Cormac Conroy - *Qualcomm, Inc., Sunnyvale, CA*
Ikuya Kawasaki - *Renesas Tech. Corp., Tokyo, Japan*
John Shen - *Nokia, Palo Alto, CA*
Tuna Tarim - *Texas Instruments, Inc., Dallas, TX*
Ted Vucurevich - *Cadence Design Systems, Inc., San Jose, CA*

TOPIC AREA: SYSTEM-LEVEL AND EMBEDDED

TOPIC AREA: NEW AND EMERGING TECHNOLOGIES

TOPIC AREA: WIRELESS

s - indicates short paper

* indicates Best Paper Candidate

SESSION 22

DIAGNOSIS AND DEBUG

Chair:
Ian Harris - *Univ. of California, Irvine, CA*

Diagnosis of failing chips is an increasingly important part of IC manufacturing and provides essential information for yield improvement and enhancement. Post-silicon debug is equally important and is needed to locate design errors that have escaped pre-silicon verification. This session includes four papers that address a broad spectrum of debug and diagnosis topics, ranging from layout-oriented diagnosis, through multiple defect diagnosis, unmodeled systematic timing effects, and a method for identifying hardware bugs in microprocessors.

22.1 Statistical Diagnosis of Unmodeled Systematic Timing Effects
Pouria Bastani, Nicholas Callegari, Li-C. Wang - *Univ. of California, Santa Barbara, CA*
Magdy Abadir - *Freescale Semiconductor, Inc., Austin, TX*

22.2 Multiple Defect Diagnosis Using No Assumptions on Failing Pattern Characteristics
Xiaochun Yu, R.D. Shawn Blanton - *Carnegie Mellon Univ., Pittsburgh, PA*

22.3 Precise Failure Localization Using Automated Layout Analysis of Diagnosis Candidates
Wing Chiu Tam, Osei Poku, R.D. Shawn Blanton - *Carnegie Mellon Univ., Pittsburgh, PA*

22.4* IFRA: Instruction Footprint Recording and Analysis for Post-silicon Bug Localization in Processors
Sung-Boem Park, Subhasish Mitra - *Stanford Univ., Palo Alto, CA*

SESSION 23

ARCHITECTURAL AND PRECISION OPTIMIZATION IN HIGH-LEVEL SYNTHESIS

Chair:
Rishiyur Nikhil - *Bluespec, Inc., Waltham, MA*

This high level design session contains two sets of novel papers on improved efficiencies in architectural and mathematical precision optimization. The first two papers focus on automating architectural choices to generate high quality circuits from within a corresponding architectural framework. The second set of papers presents contrasting approaches for the mathematical analysis and optimization of fixed point arithmetic designs.

23.1 Automatic Architecture Refinement Techniques for Customizing Processing Elements
Bita Gorjiara, Daniel D. Gajski - *Univ. of California, Irvine, CA*

23.2* Formal Datapath Representation and Manipulation for Implementing DSP Transforms
Peter A. Milder, Franz Franchetti, James C. Hoe, Markus Pueschel - *Carnegie Mellon Univ., Pittsburgh, PA*

23.3 Symbolic Noise Analysis Approach to Computational Hardware Optimization
Arash Ahmadi, Mark Zwolinski - *Univ. of Southampton, United Kingdom*

23.4 Optimizing Imprecise Fixed-point Arithmetic Circuits Specified by Taylor Series Through Arithmetic Transform
Yu Pang, Katarzyna Radecka - *McGill Univ., Montréal, QC, Canada*

SESSION 24

EXTRACTION, INTERCONNECT AND TIMING

Chair:
L. Miguel Silveira - *Technical Univ. of Lisbon / INESC-ID, Lisbon, Portugal*

This session merges important topics in parasitic extraction, interconnect modeling, and timing analysis. At the physical level two papers focus on parasitic extraction, proposing techniques that address the problems of surface roughness and cylindrical conductors for 3-D packaging. At the circuit level, one paper proposes a solution for interconnect model-order-reduction that can handle a large number of ports and another proposes an algorithm for nonlinear gate+interconnect analysis. Finally, a statistical timing analysis paper develops a method to efficiently handle non-linear and non-Gaussian variation models.

24.1 Parameterized Timing Analysis with General Delay Models and Arbitrary Variation Sources
Khaled R. Heloue, Farid N. Najm - *Univ. of Toronto, ON, Canada*

24.2 DeMOR: Decentralized Model Order Reduction of Linear Networks with Massive Ports
Boyuan Yan, Lingfei Zhou, Sheldon X.-D. Tan, Jie Chen - *Univ. of California, Riverside, CA*
Bruce McGaughy - *Cadence Design Systems, Inc., San Jose, CA*

24.3 Stochastic Integral Equation Solver for Efficient Variation Aware Interconnect Extraction
Tarek A. El-Moselhy, Luca Daniel - *Massachusetts Institute of Tech., Cambridge, MA*

24.4s Electric Field Integral Equation Combined with Cylindrical Conduction Mode Basis Functions for Electrical Modeling of Three-dimensional Interconnects
Ki Jin Han, Madhavan Swaminathan, Ege Engin - *Georgia Institute of Tech., Atlanta, GA*

24.5s Driver Waveform Computation for Timing Analysis with Multiple Voltage Threshold Driver Models
Peter Feldmann - *IBM Corp., Yorktown Hts., NY*
Debjit Sinha - *IBM Corp., Wappingers Falls, NY*
Gregory Schaeffer, Revanta Banerji, Hemlata Gupta, Soroush Abbaspour - *IBM Corp., Hopewell Junction, NY*

TOPIC AREA: VERIFICATION AND TEST

TOPIC AREA: SYNTHESIS AND FPGA

TOPIC AREA: INTERCONNECT AND RELIABILITY

* indicates Best Paper Candidate

s - indicates short paper

SESSION 25 — RM: 206AB

ARCHITECTURES FOR ON-CHIP COMMUNICATION

Chair:
Radu Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*

This session presents novel architectures and design techniques for on-chip communication. The first two papers focus on topology design with, the first paper providing a solution for LDPC decoders and the second one providing a hybrid topology solution. The remaining two papers focus on fault tolerance and parallelization of memory accesses.

25.1 Binary de Bruijn On-chip Network for a Flexible Multiprocessor LDPC Decoder
Hazem Moussa, Amer Baghdadi, Michel Jézéquel - *TELECOM, Brest, France*

25.2 An Area-efficient High-throughput Hybrid Interconnection Network for Single-chip Parallel Processing
Aydin O. Balkan, Gang Qu, Uzi Vishkin - *Univ. of Maryland, College Park, MD*

25.3 A Reconfigurable Routing Algorithm For A Fault-tolerant 2-D-mesh Network-on-Chip
Alain Greiner, Sami Taktak, Zhen Zhang - *Univ. Pierre et Marie Curie, Paris, France*

25.4 A Practical Approach of Memory Access Parallelization to Exploit Multiple Off-chip DDR Memories
Woo-Cheol Kwon, Sungjoo Yoo, Sung-Min Hong, Kyu-Myung Choi, Soo-Kwan Eo, Byeong Min - *Samsung, Yongin, Republic of Korea*

SESSION 26 — RM: 207ABC

SPECIAL SESSION: CMOS GATE MODELING FOR TIMING, NOISE, AND POWER: RAPIDLY CHANGING PARADIGM

Chairs:
Martin Wong - *Univ. of Illinois, Urbana - Champaign, Urbana, IL*
Organizers: Vladimir Zolotov - *IBM Corp., Yorktown Hts., NY*

This is a technical session in the mini-tutorial plus format: The first talk is a 30 or 45 minute mini-tutorial outlining the CMOS gate modeling problem, followed by 15 or 30 minute talks which cover various solutions or experiments looking for solutions in the topic area.

26.1s Towards a More Physical Approach to Gate Modeling for Timing, Noise, and Power
Peter Feldmann - *IBM Corp., Yorktown Hts., NY*
Soroush Abbaspour - *IBM Corp., Hopewell Junction, NY*

26.2s Transistor Level Gate Modeling for Accurate and Fast Timing, Noise, and Power Analysis
Murat Becer, Shiva Raja, Ferenc Varadi, Joao Geada - *CLK Design Automation, Inc., Littleton, MA*

26.3 A "True" Non-behavioral (Electrical) Cell Model for Timing, Noise, and Power Grid Verification
Noel Menezes, Chandramouli V. Kashyap, Chirayu Amin - *Intel Corp., Hillsboro, OR*

26.4 Challenges in Gate Level Modeling for Delay and SI at 65nm and Below
Igor Keller, King Ho Tam, Vinod Kariat - *Cadence Design Systems, Inc., San Jose, CA*

26.5 Addressing Library Creation Challenges from Recent Liberty Extensions
Richard Trihy - *Synopsys, Inc., Mountain View, CA*

SESSION 27 — FOR DESIGNERS — RM: 208AB

ADVANCED WIRELESS DESIGN

Chair:
Rami Ahola - *Mentor Graphics Corp., Dallas, TX*

This session presents solutions to wireless design problems ranging from architectural exploration of wireless systems to configurable impedance matching of RF frontends. The first paper describes a system analysis framework for designing wireless systems. The second paper extends the RFID protocol to deliver an audio stream to a wireless headset with extremely low power. The third paper introduces a methodology to dynamically adapt the performance of an RF frontend to lowest possible power dissipation in the presence of process variations and a varying operating environment. Finally, the fourth paper describes an automated methodology for designing tunable impedance matching networks for reconfigurable wireless frontends.

27.1 SystemClick - A Domain-specific Framework for Early Exploration Using Functional Performance Models
Christian Sauer, Hans-Peter Loeb - *Infineon Tech. AG, Munich, Germany*
Matthias C. Gries - *Intel Corp., Braunschweig, Germany*

27.2 Applying Passive RFID System to Wireless Headphones for Extreme Low Power Consumption
Joon Goo Lee, Dongha Jung, Jiho Chu, Seok Joong Hwang, Jong-Kook Kim, Seon Wook Kim - *Republic of Korea Univ., Seoul, Republic of Korea*
Janam Ku - *Samsung, Yongin-si, Republic of Korea*

27.3 Pro-VIZOR: Process Tunable Virtually Zero Margin Low Power Adaptive RF for Wireless Systems
Shreyas Sen, Vishwanath Natarajan, Rajarajan Senguttuvan, Abhijit Chatterjee - *Georgia Institute of Tech., Atlanta, GA*

27.4* Automated Design of Tunable Impedance Matching Networks for Reconfigurable Wireless Applications
Jamil Kawa - *Synopsys, Inc., Mountain View, CA*
Arthur Nieuwoudt, Yehia Massoud - *Rice Univ., Houston, TX*

TOPIC AREA: SYSTEM-LEVEL AND EMBEDDED

TOPIC AREA: SYNTHESIS AND FPGA

TOPIC AREA: WIRELESS

s - indicates short paper

* indicates Best Paper Candidate

SESSION 28 RM: 209AB

MANUFACTURING AWARE DESIGN AND DESIGN AWARE MANUFACTURING

Chair:
Emrah Acar - *IBM Corp., Yorktown Hts., NY*

In the nanometer technology era, continuing lithography improvement is not readily available beyond the immediate immersion lithography. The manufacturability impact due to lithography needs to be addressed during the design phase in order to minimize post-tape-out issues. In addition, and the circuit parameters need to be considered during the mask preparation phase in order to be more effective. The first two papers in the session addressed OPC aware routing, the third paper proposed timing improvement using dose map information, and the last paper considered circuit performance during mask preparation.

28.1 ELIAD: Efficient Lithography Aware Detailed Router with Compact Post-OPC Printability Prediction
Minsik Cho, **Kun Yuan, Yongchan Ban, David Z. Pan** - *Univ. of Texas, Austin, TX*

28.2* Predictive Formulae for OPC with Applications to Lithography-friendly Routing
Tai-Chen Chen - *National Taiwan Univ., Taipei, Taiwan and National Central Univ., Taoyuan, Taiwan*
Guang-Wan Liao, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

28.3 Dose Map and Placement Co-optimization for Timing Yield Enhancement and Leakage Power Reduction
Kwangok Jeong, Andrew B. Kahng, Chul-Hong Park, Hailong Yao - *Univ. of California, San Diego, La Jolla, CA*

28.4 Design-process Integration for Performance-based OPC Framework
Siew-Hong Teh, Chun-Huat Heng, Arthur Tay - *National Univ. of Singapore, Singapore*

SESSION 29 RM: 210AB

ADVANCES IN SEQUENTIAL OPTIMIZATION

Chair:
Masahiro Fujita - *Univ. of Tokyo, Tokyo, Japan*

This section presents two papers on retiming and two papers on novel ideas in sequential synthesis. The first paper presents an efficient method that dynamically constructs active timing constraints. The second paper presents runtime and memory improvements to timing constrained min area retiming. The third paper presents a new type of sequential technology independent synthesis. The fourth paper proposes the first method for designing N-variant sequential circuits.

29.1 An Efficient Incremental Algorithm for Min-area Retiming
Jia Wang, Hai Zhou - *Northwestern Univ., Evanston, IL*

29.2 Scalable Min-register Retiming Under Timing and Initializability Constraints
Aaron P. Hurst, Alan Mishchenko, Robert Brayton - *Univ. of California, Berkeley, CA*

29.3 Merging Nodes Under Sequential Observability
Michael L. Case - *Univ. of California, Berkeley, CA and IBM Corp., Austin, TX*
Victor N. Kravets - *IBM Corp., Yorktown Hts., NY*
Alan Mishchenko, Robert Brayton - *Univ. of California, Berkeley, CA*

29.4 N-Variant Design: Methodology and Applications
Yousra Alkabani, Farinaz Koushanfar - *Rice Univ., Houston, TX*

SESSION 30 RM: 210CD

PANEL: VERIFYING REALLY COMPLEX SYSTEMS: ON EARTH AND BEYOND

Chair:
Rob A. Rutenbar - *Carnegie Mellon Univ., Pittsburgh, PA*
Organizer:
Andreas Kuehlmann - *Cadence Design Systems, Inc., Berkeley, CA*

Functional verification is a major part of the effort to design electronic systems. Over the years, EDA has developed a suite of tools and methods to address the verification challenges by a patchwork of approaches. However, as the system complexity continues to increase, traditional methods may not be adequate to ensure flawless behavior. In this educational panel, we will explore how complex systems are validated in other areas. Four speakers will cover the verification challenges in airplane design, complex Mars exploration missions, modeling and rendering of movie animations, and the design of continent-wide national power grids. Using real-life examples, each speaker will introduce the general topic, outline the specific verification challenges, and discuss how they are approached in their specific domain. The following discussion will analyze commonalities and differences between the areas and explore lessons to be learned from them for EDA.

Panelists:
Anjan Bose - *Washington State Univ. , Pullman, WA*
David E. Corman - *Boeing, St. Louis, MO*
Robert M. Manning - *NASA, Pasadena, CA*
Anna Newman - *DreamWorks, Redwood City, CA*

TOPIC AREA: DFM AND THE MANUFACTURING INTERFACE

TOPIC AREA: SYNTHESIS AND FPGA

TOPIC AREA: VERIFICATION AND TEST

* indicates Best Paper Candidate

s - indicates short paper

BEYOND THE DIE - PACKAGING AND DIE STACKING

Chair: Mike Heimlich - *AWR, Pelham, NH*

Performance and design challenges don't end at the bond pads. This session looks at design flows, tools, and issues when the IC is just a piece of what is considered. Die stacking is addressed with magnetic RAM as a generic memory technology. At the packaging level, Multi-die SiP is explored with a focus on maximizing routability. Spanning both PCB and SiP are power and signal integrity in terms of EM-driven decap placement and low-power equalization design using predictive, analytical eye-opening and jitter..

31.1 Circuit and Microarchitecture Evaluation of 3-D Stacking Magnetic RAM (MRAM) as a Universal Memory Replacement

Xiangyu Dong, Xiaoxia Wu, Guangyu Sun, Yuan Xie - *Pennsylvania State Univ., University Park, PA*
Helen Li, Yiran Chen - *Seagate Tech., Bloomington, MN*

31.2 Automatic Package and Board Decoupling Capacitor Placement Using Genetic Algorithms and M-FDM

Krishna Bharath, Ege Engin, Madhavan Swaminathan - *Georgia Institute of Tech., Atlanta, GA*

31.3s Topological Routing to Maximize Routability for Package Substrate

Shenghua Liu, Xian-Long Hong - *Tsinghua Univ., Beijing, China*
Guoqiang Chen, Robi Dutta - *Magma Design Automation, Inc., San Jose, CA*
Tom Tong Jing, Lei He - *Univ. of California, Los Angeles, CA*
Tianpei Zhang - *Univ. of Minnesota, Minneapolis, MN*

31.4s Low Power Passive Equalizer Optimization Using Tritonic Step Response

Ling Zhang, Chung-Kuan Cheng - *Univ. of California, San Diego, La Jolla, CA*
Wenjian Yu - *Tsinghua Univ., Beijing, China*
Haikun Zhu - *Qualcomm, Inc., San Diego, CA*
Alina Deutsch - *IBM Corp., Yorktown Hts., NY*
George A. Katopis - *IBM Corp., Poughkeepsie, NY*
Daniel M. Dreps - *IBM Corp., Austin, TX*
Ernest Kuh - *Univ. of California, Berkeley, CA*

SPECIAL SESSION: ESL METHODOLOGIES FOR PLATFORM-BASED SYNTHESIS

Chair: Jürgen Teich - *Univ. of Erlangen-Nuremberg, Erlangen, Germany*
Organizers: Jürgen Teich - *Univ. of Erlangen-Nuremberg, Erlangen, Germany*
Florian Schäefer - *Cadence Design Systems, Inc., Feldkirchen, Germany*

This special session brings together a unique combination of international academic expertise and industrial and EDA vendor experiences in adopting ESL methodologies for industrial design flows. In the above context, a dedication is given to platform-based synthesis methodologies where a platform can be seen as an abstraction layer in the design flow promoting a meet-in-the-middle paradigm. The program is composed of presentations showing modern ESL methodologies ranging from specification, exploration to refinement and synthesis.

32.1 Daedalus: Toward Composable Multimedia MP-SoC Design

Hristo Nikolov, Todor Stefanov, Ed F. Deprettere - *Leiden Univ., Leiden, Netherlands*
Andy Pimentel, Simon Polstra, Mark Thompson - *Univ. of Amsterdam, Amsterdam, Netherlands*
Raj Bose, Claudiu Zissulescu - *Chess B.V., Haarlem, Netherlands*

32.2 SystemCoDesigner: Automatic Design Space Exploration and Rapid Prototyping from Behavioral Models

Christian Haubelt, Thomas Schlichter, Joachim Keinert - *Univ. of Erlangen-Nuremberg, Erlangen, Germany*
Michael Meredith - *Forte Design Systems, Redmond, WA*

32.3 Specify-Explore-Refine (SER): From Specification to Implementation

Andreas Gerstlauer, Junyu Peng, Dongwan Shin, Daniel D. Gajski - *Univ. of California, Irvine, CA*
Atsushi Nakamura, Dai Araki - *InterDesign Tech., Inc., Tokyo, Japan*
Yuuji Nishihara - *Japanese Aerospace Exploration Agency (JAXA), Ibaraki, Japan*

SPECIAL SESSION: WIRELESS: BUSINESS MEETS TECHNOLOGY

Chair:
Rami Ahola - *Mentor Graphics Corp., Dallas, TX*
Organizer:
Rami Ahola - *Mentor Graphics Corp., Dallas, TX*

This session will take you from wireless market trends down to the impact on technology and design methodologies. The first presentation will address the wireless markets and future trends by a Gardner analyst. Nokia will show what that means for actual devices and show a virtual tear down of various devices to illustrate what parts go into these designs and what system-level tradeoffs need to be made. The final presentation brings this down to the requirements on individual chips and technology. How does one find a path through the many advanced technology options and design tradeoffs to find the best design point to meet these needs in time?

33.1 Analyst Perspective of Wireless Market

Jon Erensen - *Gartner, Inc., Stamford, CT*

33.2 Standard Interfaces in Mobile Terminals - Increasing the Efficiency of Device Design and Accelerating Innovation

Risto Savolainen - *Nokia, Helsinki, Finland*
Tero Rissa - *Nokia, Tampere, Finland*

33.3 Holistic Pathfinding: Virtual Wireless Chip Design for Advanced Technology and Design Exploration

Matt Nowak, Riko Radojcic, Christopher Chun, Jose Corleto - *Qualcomm, Inc., San Diego, CA*

TOPIC AREA: INTERCONNECT AND RELIABILITY

TOPIC AREA: SYSTEM-LEVEL AND EMBEDDED

TOPIC AREA: WIRELESS

s - indicates short paper

SESSION 34 — RM: 209AB

LEAKAGE ANALYSIS AND OPTIMIZATION

Chair:
Clive Bittlestone - *Texas Instruments, Inc., Allen, TX*

This session includes papers on topics related to leakage analysis and optimization ranging from the use of input vector for leakage control to leakage-aware clock skew scheduling.

34.1 Full-chip Leakage Analysis in Nano-scale Technologies: Mechanisms: Variation Sources, and Modeling
Tao Li, Wenjun Zhang, Zhiping Yu - *Tsinghua Univ., Beijing, China*

34.2 Multiobjective Optimization of Sleep Vector for Zigzag Power-gated Circuits in Standard Cell Elements
Seungwhun Paik, Youngsoo Shin - *KAIST, Daejeon, Republic of Korea*

34.3s Input Vector Control for Post-silicon Leakage Current Minimization in the Presence of Manufacturing Variability
Yousra Alkabani, Farinaz Koushanfar - *Rice Univ., Houston, TX*
Tammara Massey, Miodrag Potkonjak - *Univ. of California, Los Angeles, CA*

34.4s Leakage Power-aware Clock Skew Scheduling: Converting Stolen Time into Leakage Power Reduction
Min Ni, Seda Ogrenci Memik - *Northwestern Univ., Evanston, IL*

SESSION 35 — RM: 210AB

DESIGN METHODS FOR ON-CHIP COMMUNICATION

Chair:
Tony Givargis - *Univ. of California, Irvine, CA*

On-chip communication will play a dominant role in upcoming generations of on-chip systems. This session presents four novel design methodologies with respect to communication-centric designs. Covered in this session are relevant topics on adaption for variation, mapping and routing.

35.1* Variation-adaptive Feedback Control for Networks-on-Chip with Multiple Clock Domains
Umit Y. Ogras, Radu Marculescu, Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh , PA*

35.2 Application Mapping for Chip Multiprocessors
Guangyu Chen - *Microsoft Corp., Redmond, WA*
Feihui Li - *NVIDIA Corp., Santa Clara, CA*
Seung Woo Son, Mahmut Kandemir - *Pennsylvania State Univ., University Park, PA*

35.3s Concurrent Topology and Routing Optimization in Automotive Network Integration
Martin Lukasiewycz, Michael Glaß, Christian Haubelt, Jürgen Teich - *Univ. of Erlangen-Nuremberg, Erlangen, Germany*
Richard Regler, Bardo Lang - *AUDI AG, Ingolstadt, Germany*

35.4s A Dynamically-allocated Virtual Channel Architecture with Congestion Awareness for On-chip Routers
Mingche Lai, Zhiying Wang, Lei Gao, Hongyi Lu, Kui Dai - *National Univ. of Defense Tech., Changsha, China*

SESSION 36 — FOR DESIGNERS — RM: 210CD

PANEL: KEEPING HOT CHIPS COOL: ARE IC THERMAL PROBLEMS HOT AIR?

Chair:
Devadas Varma - *Calypto, Santa Clara, CA*
Organizers:
Ruchir Puri - *IBM Corp., Yorktown Hts., NY*
Nagaraj NS - *Texas Instruments, Inc., Dallas, TX*

Thermal issues are becoming more important but is the hype getting better of the fact. Does this deserve more attention than for some niche designs and technologies such as 3-D. Does the broader design community need to worry about it at 32nm and beyond or it will only impact a small segment of designs. In short, does the severity of power issues coupled with pakaging complexity translate into a thermal crisis in future? This panel is an educational panel with a little bit of controversy that will address the "thermal" issue in IC design. When will the issue be emerging as a crucial concern if at all. What are the solutions?

Panelists:
Darvin Edwards - *Texas Instruments, Inc., Dallas, TX*
Paul Franzon - *North Carolina State Univ., Raleigh, NC*
Stephen Kosonocky - *Advanced Micro Devices, Inc., Fort Collins, CO*
Alan Weger - *IBM Corp., Yorktown Hts., NY*
Andrew Yang - *Apache Design Solutions, Inc., Mountain View, CA*

TOPIC AREA: LOW POWER DESIGN

TOPIC AREA: SYSTEM-LEVEL AND EMBEDDED

TOPIC AREA: LOW POWER DESIGN

* indicates Best Paper Candidate

s - indicates short paper

SESSION 37 RM: 206AB

NEW ADVANCES IN LOGIC SYNTHESIS

Chair:
Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

This session presents new techniques for synthesis of Boolean functions, error-tolerant designs and clock gating. The first paper presents a SAT-based functional decomposition technique. The second paper describes a new signature-based Boolean matching technique for incompletely specified functions. The third paper presents a novel error-tolerant technique to synthesize polynomials with stochastic logic. The last two papers propose new advances in clock gating.

37.1 Bi-decomposing Large Boolean Functions via Interpolation and Satisfiability Solving
Ruei-Rung Lee, Jie-Hong R. Jiang, Wei-Lun Hung - *National Taiwan Univ., Taipei, Taiwan*

37.2 Signature Based Boolean Matching in the Presence of Don't Cares
Afshin Abdollahi - *Univ. of California, Riverside, CA*

37.3 The Synthesis of Robust Polynomial Arithmetic with Stochastic Logic
Weikang Qian, Marc D. Riedel - *Univ. of Minnesota, Minneapolis, MN*

37.4s Automatic Synthesis of Clock Gating Logic with Controlled Netlist Perturbation
Aaron P. Hurst - *Univ. of California, Berkeley, CA*

37.5s A New Paradigm for Synthesis and Propagation of Clock Gating Conditions
Ranan Fraer, Gila Kamhi, Muhammad K. Mhameed - *Intel Corp., Haifa, Israel*

SESSION 38 RM: 207ABC

SPECIAL SESSION: 3-D SEMICONDUCTOR INTEGRATION AND PACKAGING

Chair:
Eli Chiprout - *Intel Corp., Hillsboro, OR*
Organizers:
Howard Chen, Ruchir Puri - *IBM Corp., Yorktown Hts., NY*

3-D integration is based on the system performance gains that can be achieved by vertical interconnection of stacked chips. Replacing 2-D interconnects with short vertical 3-D interconnects can alleviate interconnect delay issues, reduce die size, and integrate different circuit types on separate device layers. Memory applications are currently driving implementation of 3-D technologies, and other major applications will follow soon.

38.1 The Long Road to 3-D Integration: Are We There Yet?
Ted Vucurevich - *Cadence Design Systems, Inc., San Jose, CA*

38.2 Tera-scale Computing - Interconnect Requirements and Challenges
Jerry Bautista - *Intel Corp., Santa Clara, CA*

38.3 Thermal Modeling of 3-D Integrated Circuits
Paul Franzon, W. Rhett Davis, Michael B. Steer, Steve Lipa, Sonali Luniya, Thor Thorolfsson, Eun Chu Oh, Samson Melamed, Sonali Lunayi - *North Carolina State Univ., Raleigh, NC*
Kurt Obermiller, Tad Doxsee, Stephen Berkeley, Ben Shani - *Parametric Tech. Corp., Needham, MA*

38.4 Why Should We Do Three-dimensional Integration?
Wilfried Haensch - *IBM Corp., Yorktown Hts., NY*

SESSION 39 RM: 208AB

STATISTICAL TIMING ANALYSIS

Chair:
Tao Lin - *Magma Design Automation, Inc., Santa Clara, CA*

Various innovations in statistical timing analysis are introduced in this session. This includes the use of Monte Carlo techniques, fast computation of reduced-order models, propagation of sensitivity metrics, refinement of spatial correlation models, and non-parametric techniques.

39.1 Efficient Monte Carlo Based Incremental Statistical Timing Analysis
Vineeth Veetil, Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*

39.2 Generalized Krylov Recycling Methods for Solution of Multiple Related Linear Equation Systems in Electromagnetic Analysis
Zuochang Ye, Zhenhai Zhu, Joel R. Phillips - *Cadence Design Systems, Inc., Berkeley, CA*

39.3 A Framework for Block-based Timing Sensitivity Analysis
Sanjay V. Kumar, Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*
Chandramouli V. Kashyap - *Intel Corp., Hillsboro, OR*

39.4s Accurate and Analytical Statistical Spatial Correlation Modeling for VLSI DFM Applications
Jui-Hsiang Liu, Ming-Feng Tsai, Lumdo Chen, Charlie Chung-Ping Chen - *National Taiwan Univ., Taipei, Taiwan*
Lumdo Chen - *United Microelectronics Corp., Hsinchu, Taiwan*

39.5s Non-parametric Statistical Static Timing Analysis: An SSTA Framework for Arbitrary Distribution
Masanori Imai, Takashi Sato, Noriaki Nakayama, Kazuya Masu - *Tokyo Institute of Tech., Kanagawa, Japan*

TOPIC AREA: SYNTHESIS AND FPGA

TOPIC AREA: PHYSICAL DESIGN

TOPIC AREA: DFM AND THE MANUFACTURING INTERFACE

s - indicates short paper

SESSION 40 RM: 209AB

PERFORMANCE DRIVEN LAYOUT OPTIMIZATION

Chair:
Matthew Guthaus - *Univ. of California, Santa Cruz, CA*

The focus of this session is performance driven physical synthesis and clock tree optimization. The first paper incorporates buffering and congestion into an analytical placer. The second paper presents a linear programming based scheme for circuit-wide optimization. The next two papers deal with clock tree optimization (CTS), and address the problems of robustness to variation and chip level CTs for SoCs, respectively. The final paper presents a branch and bound scheme for localized circuit and layout optimization.

40.1 An Integrated Nonlinear Placement Framework with Congestion and Porosity Aware Buffer Planning
Tung-Chieh Chen - *National Taiwan Univ., Taipei, Taiwan*
Ashutosh Chakraborty, David Z. Pan - *Univ. of Texas, Austin, TX*

40.2 Circuit-wise Buffer Insertion and Gate Sizing Algorithm with Scalability
Zhanyuan Jiang - *Atoptech, Inc., Santa Clara , CA*
Weiping Shi - *Texas A&M Univ., College Station, TX*

40.3 Type-matching Clock Tree for Zero Skew Clock Gating
Chia-Ming Chang, Shih-Hsu Huang, Yuan-Kai Ho, Jia-Zong Lin - *Chung Yuan Christian Univ., Chung Li, Taiwan*
Hsin-Po Wang, Yu-Sheng Lu - *SpringSoft, Inc., Hsinchu, Taiwan*

40.4s Robust Chip-level Clock Tree Synthesis for SoC Designs
David Z. Pan, Anand Rajaram - *Univ. of Texas, Austin, TX*

40.5s Path Smoothing via Discrete Optimization
Michael D. Moffitt, David A. Papa, Zhuo Li, Charles J. Alpert - *IBM Corp., Austin, TX*

SESSION 41 RM: 210AB

POWER AND THERMAL CONSIDERATIONS IN SINGLE - AND MULTI-CORE SYSTEMS

Chair:
Davide Pandini - *STMicroelectronics, Agrate Brianza, Italy*

This session includes several exciting topics in power and thermal management for single-and multi-core systems, ranging from dynamic thermal management for multi-core systems to dynamic voltage scaling for interactive 3-D game applications and compiler-driven register re-assignment.

41.1 Stochastic Modeling of a Thermally-managed Multi-core System
Hwisung Jung, Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*
Peng Rong - *Brocade Communications, San Jose, CA*

41.2 Predictive Dynamic Thermal Management for Multi-core Systems
Inchoon Yeo, Chih Chun Liu, Eun Jung Kim - *Texas A&M Univ., College Station, TX*

41.3 Control Theory-based DVS for Interactive 3-D Games
Yan Gu, Samarjit Chakraborty - *National Univ. of Singapore, Singapore*

41.4s Many-core Design from a Thermal Perspective
Wei Huang, Mircea Stan, Karthik Sankaranarayanan, Robert Ribando Kevin Skadron - *Univ. of Virginia, Charlottesville, VA*

41.5s Compiler-driven Register Re-assignment for Register File Power-density and Temperature Reduction
Xiangrong Zhou, Chenjie Yu, Peter Petrov - *Univ. of Maryland, College Park, MD*

SESSION 42 RM: 210CD

MULTI-CORE DESIGN TOOLS AND ARCHITECTURES

Chair:
Roman Lysecky - *Univ. of Arizona, Tucson, AZ*

The papers present innovative design tools and architectural enhancements for optimizing the performance of embedded applications on multi-core processors. The design tools address parallelization of single threaded code, performance constrained energy optimization, and run-time thread management/migration environment. The architecture enhancements include optimized cache coherence protocol, and harnessing multiple scalar cores for multi-way instruction execution.

42.1 MAPS: An Integrated Framework for MPSoC Application Parallelization
Jianjiang Ceng, Jeronimo Castrillon, Weihua Sheng, Hanno Scharwächter, Rainer Leupers, Gerd Ascheid, Heinrich Meyr - *RWTH Aachen Univ., Aachen, Germany*
Tsuyoshi Isshiki, Hiroaki Kunieda - *Tokyo Institute of Tech., Japan*

42.2 ADAM: Run-time Agent-based Distributed Application Mapping for On-chip Communication
Mohammad A. Al Faruque, Rudolf Krist, Jöerg Henkel - *Univ. of Karlsruhe, Karlsruhe, Germany*

42.3 Latency and Bandwidth Efficient Communication through System Customization for Embedded Multiprocessors
Chenjie Yu, Peter Petrov - *Univ. of Maryland, College Park, MD*

42.4s Federation: Repurposing Scalar Cores for Out-of-Order Instruction Issue
David Tarjan, Michael Boyer, Kevin Skadron - *Univ. of Virginia, Charlottesville, VA*

42.5s ETAHM: An Energy-aware Task Allocation Algorithm for Heterogeneous Multiprocessor
Po-Chun Chang, I-Wei Wu, Jyh-Jiun Shann, Chung-Ping Chung - *National Chaio Tung Univ., Hsinchu, Taiwan*

TOPIC AREA: PHYSICAL DESIGN | TOPIC AREA: LOW POWER DESIGN | TOPIC AREA: SYSTEM-LEVEL AND EMBEDDED

s - indicates short paper

SESSION 43: RECONFIGURABLE ARCHITECTURE OPTIMIZATIONS

Chair:
Herman Schmit - *eASIC, Santa Clara, CA*

Reconfigurable architectures balance customization and programmability across multiple levels of the design hierarchy. This session presents techniques including a system-level architecture for Boolean satisfiability, a novel reconfigurable architecture based on content addressable memory, and circuit optimizations for FPGAs.

43.1 A Practical Reconfigurable Hardware Accelerator for Boolean Satisfiability Solvers

Zhangxi Tan - *Univ. of California, Berkeley, CA*
John Davis, Fang Yu, Lintao Zhang - *Microsoft Corp., Mountain View, CA*

43.2 Reconfigurable Computing Using Content Addressable Memory for Improved Performance and Resource Usage

Somnath Paul, Swarup Bhunia - *Case Western Reserve Univ., Cleveland, OH*

43.3s Automated Transistor Sizing for FPGA Architecture Exploration

Ian Kuon, Jonathan Rose - *Univ. of Toronto, ON, Canada*

43.4s TuneFPGA: Post-silicon Tuning of Dual-Vdd FPGAs

Stephen Bijansky, Adnan Aziz - *Univ. of Texas, Austin, TX*

SESSION 44: SPECIAL SESSION: FORMAL VERIFICATION: DUDE OR DUD? EXPERIENCES FROM THE TRENCHES

Chair:
Alan Hu - *Univ. of British Columbia, Vancouver, British Columbia, Canada*
Organizer:
Anmol Mathur - *Calypto Design Systems, Inc., Santa Clara, CA*

Formal verification has held out the promise of reducing the need to simulate billions of vectors through designs by comprehensively verifying properties of the design or equivalence checking a design against a golden model. Several techniques based on formal methods have been deployed for RTL verification and for verification of more abstract system models.

This session will focus on :

(1) Real-world experiences in deploying FV-based verification in design teams. What works and what does not? What is the real return on investment to designers and design managers? What methodology needs to be in place to leverage FV-based tools? How can formal methods be put together with simulation-based techniques in a synergistic fashion?

(2) Looking forward, what are some of the key lessons from the past and what capabilities are needed in FV tools as well as design flows to fully exploit formal techniques in design verification?

44.1 Strategies for Mainstream Usage of Formal Verification

Raj S. Mitra - *Texas Instruments, Inc., Bangalore, India*

44.2 Pre-RTL Formal Verification: An Intel Experience

Robert Beers - *Intel Corp., Hillsboro, OR*

44.3 Challenges in Using System-level Models for RTL Verification

Kelvin Ng - *NVIDIA Corp., Santa Clara, CA*

44.4 Leveraging Sequential Equivalence Checking to Enable System-level to RTL Flows

Pascal Urard, Asma Maalej, Roberto Guizzetti - *STMicroelectronics, Crolles, France*
Nitin Chawla - *STMicroelectronics, Noida, India*
Venkatram Krishnaswamy - *Calypto Design Systems, Inc., Santa Clara, CA*

SESSION 45: RANDOM TOPICS IN TESTING

Chair:
Erik Larsson - *Linköping Univ., Linköping, Sweden*

The papers in this section represent a broad sampling of the test field and include works on fault simulation using a GPU for acceleration, a design for testability technique for low power, the interface between a chip and automated test equipment, and the physical defects that underly test. Each of these topics is important in its own right and together they give a good picture of the state of the art in test.

45.1 Towards Acceleration of Fault Simulation Using Graphics Processing Units

Kanupriya Gulati, Sunil P. Khatri - *Texas A&M Univ., College Station, TX*

45.2 Scan Chain Clustering for Test Power Reduction

Melanie Elm, Michael E. Imhof, Hans-Joachim Wunderlich, Christian G. Zoellin - *Univ. of Stuttgart, Stuttgart, Germany*
Jens Leenstra, Nicolas Maeding - *IBM Corp., Boeblingen, Germany*

45.3 On Reliable Modular Testing with Vulnerable Test Access Mechanisms

Lin Huang, Feng Yuan, Qiang Xu - *The Chinese Univ. of Hong Kong, Shatin, Hong Kong*

45.4 On Tests to Detect Via Opens in Digital CMOS Circuits

Sudhakar M. Reddy, Chen Liu - *Univ. of Iowa, Iowa City, IA*
Irith Pomeranz - *Purdue Univ., West Lafayette, IN*

TOPIC AREA: SYNTHESIS AND FPGA

TOPIC AREA: VERIFICATION AND TEST

TOPIC AREA: VERIFICATION AND TEST

s - indicates short paper

SESSION 46 RM: 209AB

SECURING AND DEBUGGING EMBEDDED SYSTEMS

Chair:
Ingrid Verbauwhede - *Katholieke Univ., Leuven, Belgium*

Security and design validation are two critically important aspects of modern embedded system design. The first three papers of this session address design security: an IP protechtion scheme for design vendors, designs for intrusion detection and a software architecture that is resilient to code injection attacks. The remaining two papers present advances in embedded systems diagnostics: a real-time trace scheme for on-chip buses increases design visibility and, in the final paper, we consider diagnostics for DSP platforms.

46.1 Protecting Bus-based Hardware IP by Secret Sharing
Jarrod A. Roy, Igor L. Markov - *Univ. of Michigan, Ann Arbor, MI*
Farinaz Koushanfar - *Rice Univ., Houston, TX*

46.2 Design of High Performance Pattern Matching Engine Through Compact Deterministic Finite Automata
Piti Piyachon, Yan Luo - *Univ. of Massachusetts, Lowell, MA*

46.3s SHIELD: A Software Hardware Design Methodology for Security and Reliability of MPSoCs
Krutartha Patel, Sridevan Parameswaran - *Univ. of New South Wales, Sydney, Australia*

46.4s A Multi-resolution AHB Bus Tracer for Real-time Compression of Forward/Backward Traces in a Circular Buffer
Yi-Ting Lin, Wen-Chi Shiue, Ing-Jer Huang - *National Sun Yat-Sen Univ., Kaohsiung, Taiwan*

46.5 An Embedded Infrastructure of Debug and Trace Interface for the DSP Platform
Ming-Chang Hsieh, Chih-Tsun Huang - *National Tsing Hua Univ., Hsinchu, Taiwan*

SESSION 47 RM: 210AB

TOPICS IN POWER AND THERMAL MANAGEMENT

Chair:
Barry Pangrle - *Consultant, San Jose, CA*

This session includes papers on topics ranging from battery-aware power management, temperature and power aware DRAM design, to temperature management in systems-on-chip and dynamic voltage scaling for loop accelerators.

47.1 IntellBatt: Towards Smarter Battery Design
Suman K. Mandal, Rabi N. Mahapatra - *Texas A&M Univ., College Station, TX*
Praveen S. Bhojwani - *Sun Microsystems, Inc., Santa Clara , CA*
Saraju P. Mohanty - *Univ. of N. Texas, Denton, TX*

47.2 A Power and Temperature Aware DRAM Architecture
Song Liu, Seda Ogrenci Memik, Gokhan Memik - *Northwestern Univ., Evanston, IL*
Yu Zhang - *Synopsys, Inc., Mountain View, CA*

47.3 Phase-adjustable Error Detection Flip-flops with 2-Stage Hold Driven Optimization and Slack Based Grouping Scheme for Dynamic Voltage Scaling
Masanori Kurimoto, Hiroaki Suzuki, Rei Akiyama, Tadao Yamanaka, Haruyuki Ohkuma, Hidehiro Takata, Hirofumi Shinohara - *Renesas Tech. Corp., Itami, Japan*

47.4s Temperature Management in Multiprocessor SoCs Using Online Learning
Ayse K. Coskun, Tajana Simunic Rosing - *Univ. of California, San Diego, La Jolla, CA*
Kenny C. Gross - *Sun Microsystems, Inc., San Diego, CA*

47.5s DVFS in Loop Accelerators Using BLADES
Ganesh Dasika, Shidhartha Das, Kevin Fan, Scott Mahlke - *Univ. of Michigan, Ann Arbor, MI*
David Bull - *ARM, Cambridge, United Kingdom*

SESSION 48 FOR DESIGNERS RM: 210CD

PANEL: DFM IN PRACTICE: HIT OR HYPE

Chairs:
Andrew B. Kahng - *Univ. of California, San Diego, La Jolla, CA*
Organizers:
Nagaraj NS - *Texas Instruments, Inc., Dallas, TX*
Juan Rey - *Mentor Graphics Corp., San Jose, CA*

DFM has taken shape by virtue of manufacturers defining a series of "DFM activities", related to parametric and stochastic yield analysis and recommendations for design changes to improve yield. The picture is made more complex because the view from integrated device manufacturers, pure play foundries, and fabless semiconductor companies is not necessarily the same as they have different needs and constrains. This panel brings together DFM practitioners from each of these communities to discuss real experiences on the adoption level achieved so far as well as the impact in the manufactured products. The panel should be of interest of designers moving to advanced nodes (to learn from the experience of those that have "done it already") as well as those in the leading edge (such that they can compare experiences).

Panelists:
Robert Aitken - *ARM, Sunnyvale, CA*
Luigi Capodieci - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Cliff Hou - *Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan*
Fabian Klass - *PA Semi, Santa Clara, CA*
Vivek Singh - *Intel Corp., Hillsboro, OR*

TOPIC AREA: SYSTEM-LEVEL AND EMBEDDED

TOPIC AREA: LOW POWER DESIGN

TOPIC AREA: DFM AND THE MANUFACTURING INTERFACE

s - indicates short paper

SESSION 49 RM: 206AB

PHYSICAL EFFECTS OF VARIABILITY

Chair:
Nagib Hakim - *Intel Corp., Santa Clara, CA*

This session addresses the common agenda of modeling and optimizing designs in the presence of physical effects of variability and imperfect manufacturing. The first paper discusses SPICE simulation methods and statistical transistor model for accurate prediction of threshold voltage variability in presence of dopant fluctuations and line edge roughness. The second paper discusses efficient methods of computing on-chip capacitance sensitivity w.r.t large number of design parameters. The last paper presents leakage optimization techniques using stress enhanced layouts.

49.1 Statistical Modeling and Simulation of Threshold Variation Under Dopant Fluctuations and Line-edge Roughness
Yun Ye, Yu (Kevin) Cao - *Arizona State Univ., Tempe, AZ*
Frank Liu, Sani R. Nassif - *IBM Corp., Austin, TX*

49.2 Efficient Algorithm for the Computation of On-chip Capacitance Sensitivities With Respect to a Large Set of Parameters
Tarek A. El-Moselhy - *Massachusetts Institute of Tech., Cambridge, MA*
Abe Elfadel - *IBM Corp., Yorktown Hts., NY*
David Widiger - *IBM Corp., Austin, TX*

49.3 Leakage Power Reduction Using Stress-enhanced Layouts
Vivek Joshi, Brian Cline, Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*
Kanak Agarwal - *IBM Corp., Austin, TX*

SESSION 50 RM: 207ABC

SOFT ERROR IN SCALED CMOS DESIGN

Chair:
Subhasish Mitra - *Stanford Univ., Palo Alto, CA*

Soft error has become an increasingly important concern in scaled CMOS design. This session presents modeling and analysis techniques to diagnose the reliability of combinational circuits and memory under soft errors. To improve the efficiency, the first paper develops an analytical solution that predicts the voltage pulse induced by a particle strike. The second paper investigates the effect of timing masking in logic circuits, improving the accuracy of reliability analysis. The final paper studies the impact of multiple-bit-upset on SRAM and its interaction with physical factors. These efforts significantly enhance the understanding and tool capability to deal with soft errors.

50.1 A Fast, Analytical Estimator for the SEU-induced Pulse Width in Combinational Designs
Rajesh Garg, Charu Nagpal, Sunil P. Khatri - *Texas A&M Univ., College Station, TX*

50.2 On the Role of Timing Masking in Reliable Logic Circuit Design
Smita Krishnaswamy, Igor L. Markov, John P. Hayes - *Univ. of Michigan, Ann Arbor, MI*

50.3 Study of the Effects of MBUs on the Reliability of a 150 nm SRAM Device
Juan Antonio Maestro, Pedro Reviriego - *Univ. Antonio de Nebrija, Madrid, Spain*

SESSION 51 RM: 208AB

ADVANCES IN VERIFICATION OF ABSTRACT (PRE-RTL) MODELS

Chair:
Bhaskar J. Karmakar - *Texas Instruments, Inc., Bangalore, India*

An important direction in addressing current gaps in functional verification is raising the abstraction level of design entry. In this session, we will hear about advances in functional verification of these abstract SystemC/C++ models. The papers cover both simulation and formal verification techniques, with special focus on handling concurrency.

51.1 Partial Order Reduction for Scalable Testing of SystemC TLM Designs
Sudipta Kundu, Rajesh Gupta - *Univ. of California, San Diego, La Jolla, CA*
Malay Ganai - *NEC Labs America, Princeton, NJ*

51.2 Construction of Concrete Verification Models from C++
Malay Haldar, Gagandeep Singh, Saurabh Prabhakar, Basant Dwivedi, Antara Ghosh - *Calypto Design Systems, Inc., Noida, India*

51.3 Predictive Runtime Verification of Multi-processor SoCs in SystemC
Alper Sen, Magdy Abadir - *Freescale Semiconductor, Inc., Austin, TX*
Vinit Ogale - *Univ. of Texas, Austin, TX*

TOPIC AREA: DFM AND THE MANUFACTURING INTERFACE

TOPIC AREA: INTERCONNECT AND RELIABILITY

TOPIC AREA: VERIFICATION AND TEST

s - indicates short paper

SESSION 52

DESIGN SPACE EXPLORATION

Chair:
Tony Givargis - *Univ. of California, Irvine, CA*

In order to come up with efficient implementation architectures, it is first necessary to characterize the application. This session contains four papers that either identify the necessary characteristics or ways that information can be used to explore the architectural alternatives. The first paper looks at the automatic extraction of hardware-independent scenarios for media applications. The second paper is an optimization approach utilizing genetically programmed response surfaces. The third paper utilized machine learning to estimate the performance of systems when exploring a small fraction of the total design space. The final paper proposes a method of sub setting benchmarks.

52.1 Automated Hardware-Independent Scenario Identification
Juan Hamers, Lieven Eeckhout - *Ghent Univ., Ghent, Belgium*

52.2 Predictive Design Space Exploration Using Genetically Programmed Response Surfaces
Henry M. Cook - *Univ. of California, Berkeley, CA*
Kevin Skadron - *Univ. of Virginia, Charlottesville, VA*

52.3s Efficient System Design Space Exploration Using Machine Learning Techniques
Berkin Ozisikyilmaz, Gokhan Memik, Alok Choudhary - *Northwestern Univ., Evanston, IL*

52.4s Improve Simulation Efficiency Using Statistical Benchmark Subsetting - An Implant Bench Case Study
Zhanpeng Jin, Allen C. Cheng - *Univ. of Pittsburgh, Pittsburgh, PA*

SESSION 53

NOISE RELIABILITY ENHANCEMENT

Chair:
Makoto Nagata - *Kobe Univ., Kobe, Japan*

Scaling has created circuits which are increasingly vulnerable to crosstalk and power delivery noise. This session presents methods to avoid or mitigate the effects. The first paper presents a method to handle the effects of variability in delay noise. The second paper proposes an algorithm to mitigate the effects of dynamic power gating on power delivery noise. The final paper proposes an implemented algorithm for CODEC design that reduces crosstalk noise.

53.1 Modeling Crosstalk in Statistical Static Timing Analysis
Ravikishore Gandikota - David Blaauw, Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*

53.2 Power Gating Scheduling for Power/Ground Noise Reduction
Hailin Jiang, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara, CA*

53.3 Forbidden Transition Free Crosstalk Avoidance CODEC Design
Chunjie Duan - *Mitsubishi North America, Inc., Cambridge, MA*
Chengyu Zhu - *Polaris Microelectronics, Shanghai, China*
Sunil P. Khatri - *Texas A&M Univ., College Station, TX*

SESSION 54

PANEL: CUSTOM IS FROM MARS AND SYNTHESIS FROM VENUS

Chair:
William H. Joyner, Jr. - *Semiconductor Research Corp., Research Triangle Park, NC*
Organizers:
Nagaraj NS - *Texas Instruments, Inc., Dallas, TX*
Ruchir Puri - *IBM Corp., Yorktown Hts., NY*

The ever-increasing cost of doing design has become a major bottleneck in large-scale projects. Because of this cost crunch, automated synthesis techniques have been gaining ground on manual and cost intensive custom techniques (which potentially yield higher quality results). The push towards system level performance with multiple lower performance cores is also making the pursuit of frequency at any cost meaningless. Synthesis vs Custom has traditionally been a lively debate in microprocessor companies; now it is becoming more widespread with the desire of fabless companies to take advantage of technology to compete with IDMs by using more custom techniques. This panel will present this internal debate in a public forum. Custom fanatics will argue that we can't afford to leave performance or power on the table while spending $3 billion on a fab – we need to get the maximum benefit possible. Synthesis advocates will argue that we need to get over the last few picoseconds and nanowatts – time to market, cost, and system performance are the new drivers. Panelists will "come out swinging" and will be prepared to take on each other and the audience in this controversial debate.

Panelists:
Shekhar Borkar - *Intel Corp., Hillsboro, OR*
Ty Garibay - *Texas Instruments, Inc., Dallas , TX*
Jonathan Lotz - *Advanced Micro Devices, Inc., Fort Collins, CO*
Bob Montoye - *IBM Corp., Yorktown Hts., NY*

TOPIC AREA: SYSTEM-LEVEL AND EMBEDDED

TOPIC AREA: INTERCONNECT AND RELIABILITY

TOPIC AREA: SYNTHESIS AND FPGA

s - indicates short paper

TUTORIAL 1: BRIDGING A VERIFICATION GAP: C++ TO RTL FOR PRACTICAL DESIGN

RM: 210AB

Organizer:
Carl Pixley - *Synopsys, Inc., Hillsboro , OR*

Our thesis has long been that the reason High Level (HL) synthesis has not succeeded very well in the past is because of the lack of formal tools to decide correctness. Almost every serious design company that uses RTL-to-gate synthesis also uses formal verification to check the correctness of the translation. Until fairly recently, this has been lacking for HL synthesis. Few design managers will use HL synthesis or even by-hand RTL from HL models unless they can formally verify the correctness of the design. It is very important that the verification be independent of the synthesis; it can take hints from the synthesis but absolutely must not rely on any information from synthesis unless it is checked independently.

This tutorial is about high level (C/C++) design, synthesis and verification. We will present talks from several design houses as well as one synthesis vendor (Synfora) and one EDA company (Synopsys). The design companies will talk about how high-level design fits in their design process. Interestingly, they have radically different methodologies. One uses synthesis heavily and one does not. They will give design examples to illustrate their claims. The presentation from Synfora will talk about the technology, applicability and methodology around their tool. Synopsys will talk about the technological issues related to HL-to-RTL verification for both synthesis and ad hoc design methodologies.

This subject will be relevant to any company doing SoC design or ESL design. We hope that it will reignite interest in these subjects. The emphasis will be on verification, synthesis and methodology. It will be interesting to the audience to see how design groups are using high-level design in their flows.

There will be an aspect of survey in the talks as well. While the speakers will talk from their own experiences, they will attempt to make it as generic as possible.

Speakers:
Vinod Kathail - *Synfora, Inc., Mountain View, CA*
Mike Keating - *Synopsys, Inc., Mountain View, CA*
Emmanuel Chiaruzzi - *STMicroelectronics, Grenoble, France*
Alfred Koelbl - *Synopsys, Inc., Hillsboro, OR*
Kelvin Ng - *NVIDIA Corp., Santa Clara, CA*
Kees Vissers - *Xilinx, Inc., San Jose, CA*

TUTORIAL 2: PROGRAMMING MASSIVELY PARALLEL PROCESSORS: THE NVIDIA EXPERIENCE

RM: 209AB

Organizer:
Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh , PA*

This tutorial is meant to be a six hour accelerated course on software development for modern computer architectures with emphasis on the NVIDIA processors and the CUDA (Compute Unified Device Architecture) programming tools. Virtually all semiconductor market domains, including PCs, game consoles, mobile handsets, servers, supercomputers, and networks, are converging to concurrent platforms. There are two important reasons for this trend. First, these concurrent processors can potentially offer more effective use of chip space and power than traditional monolithic microprocessors for many demanding applications. Second, an increasing number of applications that traditionally used Application Specific Integrated Circuits (ASICs) are now implemented with concurrent processors in order to improve functionality and reduce engineering cost. The real challenge is to develop applications software that effectively uses these concurrent processors to achieve efficiency and performance goals.

The aim of this tutorial is to provide attendees with knowledge necessary for developing applications software for processors with massively parallel computing resources. Effectively programming these processors will require in-depth knowledge about parallel programming principles, as well as the parallelism models, communication models, and resource limitations of these processors. The target audiences of the course are professionals who want to develop exciting applications for these processors, as well as those who want to develop programming tools.

Speakers:
Wen-mei W. Hwu - *Univ. of Illinois, Urbana-Champaign, Urbana, IL*
David Kirk - *NVIDIA Corp., Santa Clara, CA*
Damir A. Jamsek - *IBM Corp., Austin, TX*

All Tutorials Include:		
Continental Breakfast	8:00 - 9:00am	Rm:210CD
Lunch	12:00 - 1:00pm	Rm:210CD
(Breakfast and lunch are included in the tutorial fee)		

TUTORIAL 3: ROBUST ANALOG/MIXED-SIGNAL DESIGN

RM: 208AB

Organizer:
Joel Phillips - *Cadence Design Systems, Inc., Berkeley , CA*

This tutorial will present a perspective on challenges facing analog/mixed-signal (AMS) designers as well as practical advice on getting to robust, functional circuits. It will feature a strong component of practical design methodology and illustrative examples that will be useful for practicing design engineers and managers, as well as a trends overview to provide necessary background for EDA professionals and academics.

Radu Zlatanovici will present an overview of digital techniques used in analog circuits for compensation and calibration, and analog techniques used in digital circuits to deal with problems such as power and clock distribution.

Ken Kundert will discuss the rapidly changing topic of AMS verification, and present a practical and proven methodology for performing the complete functional verification of complex analog SoCs.

Jaeha Kim will discuss analysis of difficult to simulate circuits, specifically how to speed up various circuit analyses using RF small-signal circuit analyses.

Trent McConaghy will survey new statistical AMS tools emphasizing statistical knowledge extraction, and fixing problems in a timely fashion in the presence of new effects such as well proximity and STI stress.

Speakers:
Jaeha Kim - *Rambus, Inc., Los Altos , CA*
Trent McConaghy - *Solido Design Automation, Inc., Saskatoon , ON, CA*
Ken Kundert - *Designer's Guide Consulting, Los Altos , CA*
Radu Zlatanovici - *Cadence Design Systems, Inc., Berkeley , CA*

All Tutorials Include:		
Continental Breakfast	8:00 - 9:00am	Rm:204ABC
Lunch	12:00 - 1:00pm	Rm:204ABC
(Breakfast and lunch are included in the tutorial fee)		

TUTORIAL 4: DFM REVISITED: A COMPREHENSIVE ANALYSIS OF VARIABILITY AT ALL LEVELS OF ABSTRACTION

RM: 210AB

Organizers:
Lars Liebmann - *IBM Corp., Hopewell Junction, NY*
Praveen Elakkumanan - *IBM Corp., Hopewell Junction, NY*

This full-day tutorial will discuss in detail the variability and consequent manufacturing challenges at all levels of abstraction in the nanoscale VLSI flow. It takes a holistic approach in analyzing and addressing different effects in sub-45nm process/technology, devices, modeling, physical/circuit design, architecture/system and test. The goals of the tutorial are:

1. Review variations in semiconductor manufacturing processes, their impact on layout quality, and mitigating techniques practiced to date

2. Classify and categorize the process variations into different groups based on several spatial characteristics; discuss how to model and account for some of these process variations at different length scales

3. Discuss various manufacturing-aware physical and circuit design methodologies and techniques for parametric yield improvement. This includes correct-by-construction methodologies such as Restricted Design Rules (RDRs) as well as measure-model-mitigate (3M concept) approaches

4. Discuss analysis and optimization strategies at the microarchitecure/architecture and system-levels capable of capturing variability effects for both performance and power

5. Present a brief background of VLSI test concepts and challenges involved in product functional testing, and discuss some of the techniques for adapting test to address variability

The presenters have worked together on different aspects of this subject, assuring a consistency of presentation.

Speakers:
Lars Liebmann - *IBM Corp., Hopewell Junction, NY*
Dureseti Chidambarrao - *IBM Corp., Hopewell Junction, NY*
Puneet Gupta - *Univ. of California, Los Angeles, CA*
Praveen Elakkumanan - *IBM Corp., Hopewell Junction, NY*
Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*
Nagesh Tamarapalli - *Advanced Micro Devices, Inc., Bangalore, Karnataka, India*

All Tutorials Include:		
Continental Breakfast	8:00 - 9:00am	Rm:204ABC
Lunch	12:00 - 1:00pm	Rm:204ABC
(Breakfast and lunch are included in the tutorial fee)		

TUTORIAL 5: LOW POWER TECHNIQUES FOR SoC DESIGN

RM: 209AB

Organizer:
Mike Keating - *Synopsys, Inc., Mountain View, CA*

Based on the best-selling Low Power Methodology Manual, this tutorial describes the key techniques engineers can use to minimize static and dynamic power in SoC designs.

The tutorial begins with a brief description of static and dynamic power and well-established approaches to minimizing each.

The tutorial then provides an extensive and detailed discussion of power gating. It starts with an overview of power gating, describing the basic goals and algorithms for shutting down sections of the chip while leaving the rest of the chip powered up. It then goes on to address design issues such as signal isolation, state retention and restoration methods, and power gating control. It also addresses the design of the switching network and design for test issues. To address the challenges of verifying power gating designs, we will present a case study of verifying a commercial low-power design. The tutorial also includes a discussion of Dynamic Voltage and Frequency Scaling, including measured results from silicon. The tutorial concludes with a case study of implementing voltage scaling and power gating on a commercial processor.

Speakers:
Robert Aitken - *ARM, Sunnyvale, CA*
David Flynn - *ARM, Cambridge,United Kingdom*
Alan Gibbons - *Synopsys, Inc., Reading,United Kingdom*
Mike Keating - *Synopsys, Inc., Mountain View, CA*
Nobuyuki Nishiguchi - *STARC, Yokohama, Japan*
Kaijian Shi - *Synopsys, Inc., Dallas, TX*

All Tutorials Include:		
Continental Breakfast	8:00 - 9:00am	Rm:204ABC
Lunch	12:00 - 1:00pm	Rm:204ABC
(Breakfast and lunch are included in the tutorial fee)		

TUTORIAL 6: SYSTEM-LEVEL DESIGN FOR EMBEDDED SYSTEMS

RM: 210CD

Organizer:
Mike Woodward - *The MathWorks, Inc., Natick, MA*

System-level design offers the prospect of improving the productivity and quality of embedded systems development and this tutorial provides guidance and insight on how this can be achieved in practice.

The tutorial provides a comprehensive introduction to the use of system-level design techniques for high-productivity hardware and software embedded systems development. The emphasis is on proven design techniques and technologies that can be applied to existing design processes. Our aim is for attendees to learn about practices and techniques they can apply immediately and to give a view of the directions the industry is taking for the longer term.

We will examine the use and impact of system-level design on every stage of the design process, from conception through to implementation. Techniques to be covered will include multi-domain simulation, rapid-prototyping techniques, hardware deployment, platform dependent and independent design, and the inclusion of implementation effects in high-level models.

The speakers all have substantial industry experience gathered from different parts of the embedded systems industry. They will present case studies based on their experience with using system-level design in the field.

Speakers:
Chris Dick - *Xilinx, Inc., San Jose, CA*
Jim Hwang - *Xilinx, Inc., San Jose, CA*
Stephen Koffman - *Boeing, El Segundo, CA*
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*
Mike Woodward - *The MathWorks, Inc., Natick, MA*

Workshop - Sunday, June 8 / 8:30am - 5:30pm

HIGH-LEVEL SYNTHESIS: BACK TO THE FUTURE

RM: 208A - 208B LUNCH

Workshop Registration Required
$100 - ACM/IEEE Member
$150 - Non-member

Organizers:
Adam Morawiec - *ECSI, Grenoble, France*
Philippe Coussy - *Univ. of S. Brittany, Lorient, France*

The successful usage of Hardware Description Languages like VHDL and Verilog in design flows is mainly due to the availability of efficient synthesis methods and tools that enable the translation of RTL designs into optimized gate-level implementations. Many expect that the same approach could be effectively adapted at higher levels of abstraction. In the SoCs context, the traditional IC design methodology relying on EDA tools used in a two stages design flow - a VHDL/Verilog RTL specification, followed by logical and physical synthesis - is indeed no more suitable. Thus, actual complex SoCs need new ESL level tools in order to raise the specification abstraction level up to the algorithmic / behavioral one. However, in order to provide the designers with an efficient automated path to implementation, new high-level synthesis tools are required.

The main expectations from the system design teams concern both methods and tools supporting better management of the design complexity and reduction of the design cycle all together, breaking the trend to compromise evaluation of various design implementation options. Designing at higher levels of abstraction is an obvious way as it allows a better coping with the system design complexity, to verify earlier in the design process and to increase code reuse.

Target Audience:

This workshop on high-level Synthesis will provide an overview of existing and emerging solutions provided by both industrial partners (EDA companies) and research institutions in this domain. It will give an outline of HLS methods and tools available currently on the market and bring the details on their applicability, performance, and strengths. Finally, the event will create a discussion platform for experience exchange between providers of synthesis technology and industry users.

8:30 - 8:40am Introduction
Philippe Coussy - Univ. of South Brittany, France
Adam Morawiec, ECSI, France

8:40 -10:10am Session 1: Architecture and Design Flow I

8:40 - 9:00am The Real High-level Synthesis
Daniel D. Gajski - *Univ. of California, Irvine, CA*

9:00 - 9:20am From Executable Specifications to High-quality Implementations Using Bluespec
Rishiyur S. Nikhil - *Bluespec, Inc., Waltham, MA*

9:20 - 9:40am Integrating Post-programmability Into the High-level Synthesis Equation
Scott Mahlke - *Univ. of Michigan, Ann Arbor, MI*

9:40 - 10:00am Synthesis and Optimization Foundation for ESL 2.0
Jason Cong - *AutoESL Design Tech., Inc., Los Angeles, CA*

10:00 - 10:20am BREAK

10:20am-12:00pm Session 2: Low-power and Thermal Aware High-level Synthesis

10:20 - 10:40am System-level Power Management
Rajesh Gupta - *Univ. of California, San Diego, CA*

10:40 - 11:00am High-level Synthesis: Optimizing for Low Power Design
Andres Takach - *Mentor Graphics Corp., Wilsonville, OR*

11:00 -11:20am When High-level Synthesis Meets Power, Thermal, and Reliability Challenges
Li Shang - *Univ. of Colorado, Boulder, CO*

Robert P. Dick, *Northwestern Univ., Evanston, IL*

11:20 -11:50am Power Optimizing High-level Synthesis
Eike Schmidt - *ChipVision Design Systems, Oldenburg, Germany*

12:00 - 1:30pm Session 3: Posters / Demonstrations / Interactive presentations (with Lunch Buffet - Rm:208B)

1:30 - 3:00pm Session 4: Architecture and Design Flow II

1:30-1:50pm HLS as an Enabling Technology: Some Complex Examples
Arvind - *Massachusetts Institute of Tech., Cambridge, MA*

1:50-2:10pm Applying SystemC Synthesis to All Your Design Challenges
Michael Meredith - *Forte Design Systems, Redmond, VA*

2:10-2:30pm Latency Insensitive Scalable System Synthesis
Forrest Brewer - *Univ. of California, Santa Barbara, CA*

2:30 - 2:50pm ESL: A Picture Paints A Thousand Words
Chris Eddington - *Synplicity, Inc., Cupertino, CA*

3:00 - 3:15pm BREAK

3:15 - 4:25pm Session 5: Design Flow and User Needs

3:15 - 3:35pm C-based SoC Design Flow with "CyberWorkBench"
Kazutoshi Wakabayashi - *NEC Corp., Tokyo, Japan*

3:35 - 3:55pm How to Make Algorithmic Synthesis as Ubiquitous as Logic Synthesis
Vinod Kathail - *Synfora, Inc., Mountain View, CA*

3:55 - 4:10pm Industrial Usage of High-level Synthesis
Nitin Chawla - *STMicroelectronics, Noida, India*

4:10 - 4:25pm HLS for SoC: How to Integrate new Class of Algorithms in Existing Platform
Gael Clave - *Texas Instruments, Inc., Villeneuve-Loubet, France*

4:25 - 5:10pm Panel with participants from User Companies, EDA and Academia

5:10 - 5:30pm Wrap-up and Close

5TH INTERNATIONAL UML FOR SoC DESIGN WORKSHOP: UML IN APPLICATION

RM: 209A - 209B LUNCH

Organizers:
John Wolfe - *Mentor Graphics Corp., Tucson, AZ*
Wolfgang Mueller - *Paderborn Univ., Paderborn, Germany*

Workshop Registration Required
$100 - ACM/IEEE Member
$150 - Non-member

In recent years, interest in the application of UML to engineering problems has steadily increased. However only a few case studies of complex systems have been reported in technical detail. The 5th International UML for SoC design workshop will focus on UML applications beyond simple examples. The workshop is open to anyone interested in learning more about UML for SoC and embedded systems design for complex applications. Morning presentations will consist of tutorials on the application of UML to general SoC and embedded system design, the MARTE extension and the AUTOSAR standard. Afternoon sessions will (a) cover the most recent trend to apply UML in the context of SPIRIT IP-XACT for design interchange and (b) present complex UML designs. A complementary tool session will exhibit UML tools in the afternoon.

Opening and Morning Tutorials

9:00am Welcome and Introduction by the Workshop Organizers

9:15am UML for SoC and Embedded Systems Design - An Introduction

Wolfgang Mueller - *Paderborn Univ., Paderborn, Germany*

Yves Vanderperren, Wim Dehaene - *Katholieke Univ., Leuven, Belgium*

10:00am MARTE - Modeling and Analysis of Real-time and Embedded Systems

Francois Terrier, Sebastien Gerard - *CEA LIST, Fontenay aux Roses, France*

11:00am Break

11:15am UML for Automotive Applications - Introduction to AUTOSAR

Bill Chown - *Mentor Graphics Corp., Wilsonville, OR*

12:15pm Lunch in room 209B

IP-XACT and UML for IP Integration and Management

1:15pm Model-driven Approach for Automatic SPIRIT IP Integration

Tero Arpinen, Erno Salminen, Marko Hännikäinen, Timo D. Hämäläinen - *Tampere Univ. of Tech., Tampere, Finland*

1:45pm UML and IP-XACT for Integrated SPRINT IP Management

Tim Schattkowsky, Tao Xie - *Paderborn Univ., Paderborn, Germany*

2:15pm UML/MARTE for SPIRIT-ed SoC

Frédéric Mallet, Robert de Simone - *INRIA, Sophia Antipolis, France*

2:45pm UML based Code Generation for the HW/SW Interface

Wolfgang Ecker, Volkan Esen, Thomas Steininger, Michael Velten - *Infineon Tech. AG, Munich, Germany*

3:15 Break

UML in Complex Applications

3:30pm The UML-based Design of a Hardware H.264/MPEG4 AVC Video Decompression Core

Robert Thomson - *Axilica Limited, Loughborough, United Kingdom*

Scott Moyers, David Mulvaney, Vassilios Chouliaras - *Loughborough Univ., Loughborough, United Kingdom*

4:00pm UML-based Specification Level Design and Property Checking Methodology of SoC

Yeonbok Lee, Yuji Ishikawa, Tasuku Nishihara, Yoshihisa Kojima, Takeshi Matsumoto - *Univ. of Tokyo, Tokyo, Japan*

Hiroaki Yoshida, Masahiro Fujita - *VLSI Design and Education Center, Univ. of Tokyo, Tokyo, Japan*

Hisashi Yomiya - *Toshiba Corp., Kawasaki, Japan*

4:30pm Functionality Capture and Structuring in SYSML for a Combined Automotive Hardware and Software Application

Florian Schäefer - *Cadence Design Systems, Inc., Feldkirchen, Germany*

Tool Demos

5:00pm Tool Demonstrations by Axilica, CEA-LIST, Mentor Graphics Corp., Technical Univ. of Tampere and others

Workshop Closing

6:00pm Workshop Closing and Wrap-up by the Organizers

SYSTEM AND SoC DEBUG

RM: 303B - 303A LUNCH

Chairs:
Adam Morawiec - *ECSI, Grenoble, France*
Neal Stollon - *HDL Dynamics, Dallas, TX*

Workshop Registration Required
$100 - ACM/IEEE Member
$150 - Non-member

Debug is one of the biggest factors in delaying shipment of a product. The problem is exacerbated with the introduction of multi-core technology. SoC-level multi-core debug is a topic that has received considerable visibility, due to its importance in improving the verification and analysis of SoCs and improving time to market of silicon products. A fair amount of activity has gone into standardization of the interfaces, features, and methodologies related to multi-core debug. There is also considerable discussions and development work going into the standardization of the software interfaces used to debug multi-core applications. This represents a challenge in scaling software development tools such as debuggers and simulators to support chips with 10s or 100s of cores. This workshop, based on the two successful workshops organized by ECSI in 2007 and in early 2008, provides an overview into several standards efforts related to multi-core debug with representation from IEEE working groups including Nexus Forum, IJTAG (IEEE P1687), as well as working groups within the OCP-IP, Multi-core Association, SPIRIT, and Eclipse consortiums. In addition industrial project SPRINT contribution to standardization will be presented. The workshop also shows a vast set of requirements expressed by the system and SoC companies with regard to debug methods and tools. Furthermore, the event will also present and contrast existing commercial debug tools.

Preliminary Agenda:

9:00 - 9:30am Session 1: Introduction to Challenges in System and SoC Debug

This session will present major problems in the area of debug of complex systems. An overview of emerging solutions and a "topology map" of the existing standardization activities will be presented, as well as their relations to industry initiatives and de facto standards.

Presenter:

Neal Stollon - *HDL Dynamics, Dallas, TX*

9:30 - 11:00am

Session 2: Industry Requirements

Industry partners from system companies, SoC providers, and IP providers will express their needs for methods, tools, interfaces, and standards for pre-silicon debug of complex multi-core systems. Current practice and available solutions will be discussed, as well as future directions to be undertaken in research, development, and standardization.

Presenters:

- LSI Corp. - **Gary Delp** - *LSI Corp., Rochester, MN*
- Debug IP for SoC Debug - **Mark Woods** - *ARM, Sunnyvale, CA*
- Freescale - **Robert Oshana** - *Freescale Semiconductor, Inc., Austin, TX*
- SPRINT Debug Working Group - Requirements from Infineon, ST, NXP on Debug Methods - **Michael Velten** - *Infineon Tech. AG, Munich, Germany*

11:00 - 11:15am Break and Networking

11:15am - 12:45pm Session 3: Debug Standardization Activities

In this session existing active standardization initiatives will be presented together with their achievements, roadmaps, current evolution, and industry support.

Presenters:

- OCP Debug Socket for Multi-core Debugging - **Neal Stollon** - *HDL Dynamics, Dallas, TX*
- IEEE Nexus 5001 - **Neal Stollon** - *HDL Dynamics, Dallas, TX*
- SPIRIT IP-XACT Debug WG - **Gary Delp** - *SPIRIT Consortium, Rochester, MN*
- Linking the Worlds of SystemC and Eclipse, the GreenSoCs VPP Project - **Mark Burton** - *Greensocs, Cambridge,United Kingdom*

12:45 - 1:30pm Lunch, Rm: 303A

1:30 - 3:45pm Session 4: Debug Tools and Implementations Presentations

Available tool solutions will be introduced in this session, these short (10-15min) presentations will be followed by demonstrations in the Session 6.

Presenters:

- ARM RealView Debug Tools - **Mark Woods** - *ARM, Sunnyvale, CA*
- The Confirma Platform for ASIC, SoC and IP debug in FPGA - **Doug Amos** - *Synplicity, Henley on Thames, United Kingdom*
- Magillem: IP-XACT Flow Control for Debug - **Emmanuel Vaumorin** - *Magillem Design Services, Paris, France*
- Post-Silicon System Validation and Debug - **Paul Bradley** - *DAFCA, Framingham, MA*
- Flexible Debugging of SoC and IP Hardware and System Software on the PROC_SoC Platform - **Ralph Zak, Shyam Uma Chander** - *GiDEL, Inc., Santa Clara, CA*
- Debugging Using the SHAPES Virtual Platform - **Rainer Leupers, Lei Gao, Stefan Kraemer** - *RWTH-Aachen Univ., Aachen, Germany*
- Nexus-5001 Compatible Real-time Trace for SoC Debug - **Akilesh Parameswar, Marc Gauthier, Dhanendra Jani** - *Tensilica, Inc., Santa Clara, CA*
- CJTAG Block/Chip Level Verification Engine - **Stylianos Diamantidis** - *GlobalTech Solutions, Austin, TX*

3:45 - 4:00pm Break

4:00 - 4:30pm Session 5: Panel: Are we developing right debug solutions to tackle with the real challenges of complex MP SoCs?

The panel will gather opinions from all industry sectors on possible future evolutions required to enable efficient SoC debug able to scale to current and future technology. It will discuss the overlaps in standardization activities that make the entire picture of future industry proven standards very difficult to draw.

4:30 - 5:15pm

Session 6: Demos + Networking

This session will enable parallel demonstrations of EDA tools, free discussion, and networking between participants of the workshop.

BIOCHIPS TO INTERFACE AND MONITOR HUMAN BIOLOGICAL FUNCTIONS

RM: 210AB - 210C LUNCH

Workshop Registration Required
$100 - ACM/IEEE Member
$150 - Non-member

Chairs:
Raymond Campagnolo - *CEA LETI, Grenoble, France*
Steven P. Levitan - *Univ. of Pittsburgh, Pittsburgh, PA*
Organizer:
Ahmed Jerraya - *CEA LETI, Grenoble, France*

Biochips provide interfaces between living systems and electro-mechanical and computational devices. These chips may be used in such varied applications as artificial sensors, prosthesis, portable/disposable laboratories or even as implantable devices to enhance human life. Biochips promise dramatic changes in future medical science and human life in general. With the advances of bio and nano technologies two strong paradigms of integrated electronic and life are emerging. Biosensor chips can provide the construction of sophisticated human sensing systems such as nose and ears. The second paradigm is chips for sensing biology that will provide for interactions with living bodies and build new diagnosis tools (such as diabetes glucose meters) or new medicines (such as a bio-assay chip). This full-day workshop brings together key researchers from the fields of biochip technologies and applications to understand the potential of these new bio inspired chips. The program includes a keynote to present strategic directions, two technical sessions to explore state-of-the-art research, and a panel session to discuss major implication of these new technologies on our lives.

9:30am SESSION 1: KEYNOTE
Neurological Interface Chips - **Jan Rabaey** - *Univ. of California, Berkeley, CA*

10:30am Break

11:00am SESSION 2: Bio Sensor chips

Chair:
Steven P. Levitan - *Univ. of Pittsburgh, Pittsburgh, PA*

Artificial Nose Chip - **Ed Myers** - *California Institute of Tech., Pasadena, CA*
Brain Computer Interface- **Régis Guillemaud,** *CEA LETI, Grenoble, France*

12:00pm Lunch served in Room 210C

1:00pm SESSION 3: Chips for sensing biology

Chair:
Ahmed Jerraya - *CEA LETI, Grenoble, France*

Virus Assay Chip - **Donald Chiarulli** - *Univ. of Pittsburgh, Pittsburgh, PA*
Bacteria on Chip - **Sylvain Martel** - *École Polytéchnique de Montréal, Montréal, QC, Canada*
Nanotechnology in Cancer Diagnosis and Treatment - **Michael Heller** - *Univ. of California, San Diego, La Jolla, CA*

2:30pm Break

3:00pm SESSION 4: Panel on Chip Human Interfaces
Discussion with all speakers

4:30pm Close

Workshop - Sunday, June 8 / 2:00 - 5:00pm

DESIGN AND VERIFICATION OF LOW POWER SoCs: AN APPLICATION ORIENTED APPROACH

RM: 303C

Organizer:
Yatin Trivedi - *Magma Design Automation, Inc., San Jose, CA*

Workshop Registration Required
$75 - ACM/IEEE Member
$100 - Non-member

Power management is critical in IC design, especially for mobile devices, battery-operated systems, and non-portable systems with power consumption constraints. However, not all applications have the same requirements for addressing power management.

In this workshop, experts from different application areas will discuss the requirements and solutions for power management, including design, verification and analysis. The areas chosen for this workshop include wireless (main theme for DAC 2008), automotive (main theme for DAC 2007), IP (ubiquitous component of all large designs today), and EDA flows (inherently integral part of all design environments). A general overview of low power design and verification challenges for SoC designers will set the context for each of the application areas.

All of the speakers have actively participated in the development of IEEE standard for low power format (IEEE P1801), and have made significant contribution to help address the challenges for their respective application areas. In addition to their insights, interoperable EDA flows based on IEEE P1801 low power format will be demonstrated so the attendees can see how they can build and deploy low power solutions from one or more EDA tool vendors for design, verification and analysis.

2:00 - 2:05pm Introduction
Stephen Bailey - *Product Marketing Manager, Verification, Mentor Graphics Corp., Longmont, CO*

2:05 - 2:30pm Low Power Challenges for SoC Design and Verification
Gary Delp - *LSI Corp., Rochester, MN*

2:30 - 2:55pm Low Power Challenges for Wireless IPs - From ESL to GDS

2:55 - 3:20pm Low Power Challenges in Automotive Applications
Juergen Karmann - *Senior Staff Engineer Design Methodology, Automotive, Industrial and Multimarket, Infineon Tech. AG, Munich, Germany*

3:20 - 3:45pm Requirements and Solutions for Low Power Commercial Processor Cores
John Biggs - *Staff Engineer, ARM, Cambridge,United Kingdom*

3:45 - 4:00pm Low Power Flow for Design and Verification
Ed Huijbregts - *Vice President, Design Implementation Products, Magma Design Automation, Inc., Eindhoven, Netherlands*

4:00 - 4:45pm Deploying Low Power Design Flows
A Multi-vendor Collaborative Solution

4:45 - 5:00pm Roundtable and Wrap-up

LOW POWER COALITION WORKSHOP - ADVANCES IN LOW POWER DESIGN FOR CIRCUITS AND SYSTEMS

RM: 206B

Organizers:
Sumit DasGupta - *Si2, Austin, TX*
Nick English - *Si2, Austin, TX*
Bill Bayer - *Si2, Austin, TX*

Workshop Registration Required
$75 - ACM/IEEE Member
$100 - Non-member

The economic and environmental requirements for electronic circuits and systems to consume less power per function are going to endure with the electronic and EDA industries for the foreseeable future. Each year, advances must be made to continue this required trend.

The Low power Coalition (LPC) at Si2 is steadily making the required advances across the entire design flow; from Electronic system-level (ESL) all the way through implementation. Work is being done to define a complete power-aware reference flow that will be recommended to the industry. To aid in automating many of the steps along the tool chain, a data model and associated Application Procedural Interface (API) are being defined that will work seamlessly with the OpenAccess API and information model. In addition, enhancements are being defined to extend the Common Power Format (CPF), an Si2 standard first released in March 2007.

This workshop will present the steps forward since the last Low Power Workshop at DAC 2007 and discuss future directions and end-user experiences with the technology developed and implemented so far. A selection of advanced tools that have been developed by some of the EDA companies will be presented to provide tangible progress in power-aware design.

4:00 - 4:10pm Introduction to the Low Power Coalition
Gill Watt - *Advanced Micro Devices, Inc., Boxborough, MA - Chairman of the LPC*

4:10 - 4:25pm Low Power Design Format Requirements: Looking Ahead!
Milind Padhye - *Freescale Semiconductor, Austin, TX*

4:25 - 4:40pm LPC Low Power Reference Flow
Nagu Dhanwada - *IBM Corp., Fishkill, NY - Chair, Flow Working Group*

4:40 - 4:55pm LPC Data Model and API
David Hathaway - *IBM Corp., Essex Junction, VT - Co-chair, Data Model and API WG*

4:55 - 5:10pm BREAK

5:10 - 5:50pm End-user Experiences
David Hui - *Advanced Micro Devices, Inc., Yardley, PA*

5:50 - 6:30pm EDA Tool Developers for Low Power
Koorosh Nazifi - *Cadence Design Systems, Inc., San Jose, CA*
Jerry Frenkil - *Sequence Design, Inc., Santa Clara, CA*
Anmol Mathur - *Calypto Design Systems, Inc., Santa Clara, CA*

6:30 - 7:00pm Panel Discussion (all presenters)

Workshop - Monday, June 9 / 8:30am - 4:30pm

CROSS-LAYER POWER AND THERMAL MANAGEMENT

RM: 212A - 212B LUNCH

Organizers:
Yung-Hsiang Lu - *Purdue Univ., West Lafayette, IN*
Ricardo Bianchini - *Rutgers Univ., Piscataway, NJ*

Workshop Registration Required
$100 - ACM/IEEE Member
$150 - Non-member

Reducing power consumption and managing temperature have become two most critical issues in electronic designs. This is reflected in the topics of many conference and journal papers. However, there are insufficient opportunities for researchers in different areas to interact. This workshop will serve the purpose of "creating conversations" among researchers with different backgrounds. A wide range of topics are covered in this workshop; the topics are divided into five different layers: circuits and devices, packaging, architectures, systems, and software design. Five experts, from academia and industry, are invited to present their views on existing solutions and future challenges in power and thermal management. Each speaker will explain the state-of-the-art technology, relationships and interactions with other layers in electronic design, and point out directions for future research. This workshop is the first of its kind and will bring together many researchers from different areas to develop new visions for research on power and thermal management.

The workshop is partially sponsored by the Low Power Technical Committee of ACM Special Interest Group on Design Automation.

8:30 - 8:50am Breakfast

8:50 - 9:00am Welcome: Yung-Hsiang Lu and Ricardo Bianchini

9:00 - 9:45am Session 1: Low-voltage Low-power CMOS: Device and Circuit Perspective

Chair:

Barry Pangrle - *Consultant, San Jose, CA*

Speaker:

Kaushik Roy - *Purdue Univ., West Lafayette, IN*

9:45 -10:30am Session 2: System on Package (SoP): A Platform for Micro, Nano and Bio Convergence

Chair:

Robert P. Dick - *Northwestern Univ., Evanston, IL*

Speaker:

Madhavan Swaminathan - *Georgia Insititute Tech., Atlanta, Georgia*

10:30 - 11:00am Break

11:00 - 11:45am Session 3: Multi-core and Energy

Chair:

Tajana Simunic Rosing - *Univ. of California, San Diego, La Jolla, CA*

Speaker:

Edward Grochowski - *Intel Corp., Santa Clara, CA*

11:45am - 12:30pm Session 4: Power Management: A System-level Concern Demanding System-wide Solutions

Chair:

Eugene Gorbatov - *Intel Corp., Santa Clara, CA*

Speaker:

Karthick Rajamani - *IBM Corp., Austin, TX*

12:30 - 2:00pm Lunch, Rm: 212B

2:00 - 2:45pm Session 5: Abstracting Physical Effects

Chair:

Yuan Xie - *Pennsylvania State Univ., University Park, PA*

Speaker:

Frank Bellosa - *Univ. of Karlsruhe, Karlsruhe, Germany*

2:45 - 3:55pm Panel Session

Moderator:

Yung-Hsiang Lu - *Purdue Univ., West Lafayette, IN*

Panelists:

Kaushik Roy, Madhavan Swaminathan, Edward Grochowski, Karthick Rajamani, Frank Bellosa

3:55 - 4:00pm Break

4:00 - 4:25pm ACM SIGDA LPTC

Speaker:

Naehyuck Chang - *Seoul National Univ., Seoul, Republic of Korea*

4:25 - 4:30pm Closing Remarks: Yung-Hsiang Lu and Ricardo Bianchini

WOMEN IN DESIGN AUTOMATION: NETWORKING, NEGOTIATION, AND NONSENSE: ACHIEVING CAREER BALANCE IN AN UNBALANCED WORLD

RM: 205A - 205B LUNCH

The 2008 WWINDA will offer DAC attendees a valuable half-day session focused on how to successfully, and happily, navigate their careers. Speakers and panelists will discuss the critical, yet often challenging-to-master, business skills of networking and negotiating to achieve personal satisfaction and professional visibility. In addition, attendees will hear various perspectives on the importance of nonsense, and how to consciously incorporate humor and joy into their work lives. The workshop is an informative and inspiring event for people at any stage in their careers, and provides valuable opportunities for industry peers to meet and share ideas. The half-day session will conclude with the presentation of the 2008 Marie R. Pistilli Achievement Award, given each year to an outstanding role model and mentor to women in EDA.

The 2008 WWINDA Committee extends a sincere invitation to all members of the EDA community - men and women of all ages and all levels of professional development - to join us as we discuss "Networking, Negotiating, and Nonsense in an Unbalanced World". Breakfast and lunch are included.

Workshop for Women in Design Automation: MISSION STATEMENT

To be a workshop of relevance to women in Electronic Design Automation, by providing a forum for the exchange of ideas for successful careers in the EDA profession, to address the particular needs of professional women, and to provide an opportunity for peer networking.

WWINDA Chair: Peggy Aycinena - *Editor, EDA Confidential*

WWINDA Vice Chair: Karla Reynolds

Workshop Registration Required
$50 - ACM/IEEE Member
$75 - Non-member

STEERING COMMITTEE

Nanette Collins - *Publicity Chair, 45th DAC*

Marie R. Pistilli - *Co-chair, Board of Directors, MP Associates, Inc.*

Sabina Burns - *Vice President, Corporate Marketing and Communications, Virage Logic Corp.*

KEYNOTE SPEAKER:

Mar Hershenson - *Vice President, Product Development, Custom Design Business Unit, Magma Design Automation, Inc.*

Mar Hershenson joined Magma through the acquisition of Sabio Labs, where she was the CEO and a co-founder. Sabio Labs offered an equation-based design environment for mixed-signal ICs. Prior to Sabio Labs, she was CTO and co-founder of Barcelona Design, where she commercialized her graduate research in the application of convex optimization to analog circuit design. She also worked at leading Silicon Valley companies such as Linear Technology Corp. and Apple Computer. Hershenson has been awarded eight patents and has several other patents pending. She is also a Consulting Professor at Stanford Univ., teaching analog circuit design courses. In 2002, she received the prestigious award TR100 Young Investigator from MIT. She served on the executive committee at ICCAD in 2007 and 2008.

Mar Hershenson graduated with honors with a B.S. in electrical engineering from the Universidad Pontificia de Comillas in Madrid, and received her M.S. and Ph.D. degrees in electrical engineering from Stanford University.

Panel Moderator:

Karla Reynolds - *Vice Chair 2008 WWINDA*

Panelists:

Ann Marie Rincon - *ON Semiconductor, Senior Scientist*

Gila Kamhi - *Intel Corp., Principal Engineer*

Sabina Burns - *Virage Logic Corp., Vice President Corporate Marketing*

Elizabeth Abraham - *Carbon Design Systems, Vice President Consulting Services & Marketing*

INTRODUCTION TO CHIPS AND EDA FOR A NON-TECHNICAL AUDIENCE

RM: 206B

Workshop Registration Required
$10 - ACM/IEEE Member
$10 - Non-member

Organizer:
Karen Bartleson - *Synopsys, Inc., Mountain View, CA*

Electronics are truly amazing, and our industry is one of the most advanced and complex in the world. For non-technical people in the business, the technology can seem daunting. Are you one of these people who want to know what the techies are talking about? Would you like to have a simple understanding of how the phenomenal little devices called computer chips are able to make modern electronic gadgets work?

If you're a non-technical member of the electronics industry and want to know more about how chips are designed and manufactured, this workshop is for you. Whether you're just starting out or you've been in the business for a while, this two-hour session will give you just what you need to gain a basic understanding of chips and how they are designed with Electronic Design Automation (EDA). You'll come away more informed and comfortable in the fascinating and fast-paced world of chips and EDA.

This workshop provides: a simplified explanation of how chips are designed and manufactured, an understanding of how essential EDA is to chip design, an opportunity to see and touch the parts that make up chips and electronic products, a non-threatening, fun event with working knowledge to take away.

This workshop is for: Non-engineering staff from technology companies, analysts and media people unfamiliar with EDA and semiconductor industries, educators and students who are curious about chip technology and design automation friends and relatives of technical people.

Workshop objectives: Provide a basic understanding of EDA and semiconductors to non-technical people. Present information in simple, easy-to-understand terms. Use hands-on parts (wafers, chips, masks . . .) for enhanced experience. Encourage people to join and invest in the EDA industry, address ongoing requests to help non-technical people understand the EDA industry.

Please Note: This workshop is similar to the one presented at DAC 2007. The workshop is for non-technical attendees.

Maximum Attendance is 50.

Speaker:
Pamela McDaniel - *Synopsys, Inc., Mountain View, CA*

4TH INTEGRATED DESIGN SYSTEMS WORKSHOP - OPENACCESS: A PLATFORM FOR CONTINUOUS EVOLUTION AND INNOVATION

RM: 208A - 208B LUNCH

Organizers:
Nick English - *Si2, Austin, TX*
Bill Bayer - *Si2, Austin, TX*
Sumit DasGupta - *Si2, Austin, TX*

Workshop Registration Required
$100 - ACM/IEEE Member
$150 - Non-member

As OpenAccess continues to deliver on the promise of interoperable EDA tools, its rich ecosystem is leading to exciting innovations that are changing the future of IC design systems. This workshop will explore some of these areas which are right now being developed by the OpenAccess community. Presentations and demonstrations will highlight these innovations and provide details on current functionality as well as planned progress. They include:

1. Electronic system-level (ESL) Extensions: Proposed extensions to OpenAccess will allow ESL design systems to directly interface to OpenAccess-based physical analysis capabilities. These extensions will enable the mapping of system-level design representations on to their physical counterparts in OpenAccess to facilitate this analysis.

2. OpenEngines: This proposed program would allow the interoperation of software engines and components that sit on top of the OpenAccess application programming interface (API) and information model. EDA vendors, academia, and end-user tool developers could write these engines without the need to build complete applications, and EDA users could integrate them into their OpenAccess-based design systems.

3. Open Modeling Calculation Interface: The OpenAccess Coalition is working with the Open Modeling Coalition to develop a common interface to support consistent and accurate computation of library models for all EDA applications. This system provides direct access and bi-directional communication between OpenAccess applications and executable library models and parameters.

4. Interoperable PCell Libraries (IPL): The IPL Initiative is creating and distributing an open-source IPL that resides in the OpenAccess database. For the first time in semiconductor industry history, IC designers will be able to operate on the same PCell libraries with tools from multiple vendors and any tools that they developed in-house.

Lunch served at 12:00pm in room 208B
Meeting time: 1:00 - 4:00pm

Requirements for Electronic System-level (ESL) Extensions: 40 minutes
John Darringer - *IBM Corp., Yorktown Hts., NY*
Luca Carloni - *Columbia Univ., New York, NY*

OpenEngines: 30 minutes
Rob Mains - *Sun Microsystems, Inc., Santa Clara, CA*

Open Modeling Calculation Interface: 30 minutes
Martin Foltin - *Hewlett-Packard Co., Fort Collins, CO*

BREAK 15 minutes

Interoperable PCell Libraries (IPL): 40 minutes
Ed Lechner - *Synopsys, Inc., Mountain View, CA*
Ed Petrus - *Ciranova, Inc., Santa Clara, CA*

Panel Discussion: All speakers 30 minutes

DIAGNOSTIC SERVICES IN NETWORK-ON-CHIPS (DSNOC)

RM: 303AB - 303C LUNCH

Organizers:
Erik Jan Marinissen - *NXP Semiconductors, Eindhoven, Netherlands*
Nicola Nicolici - *McMaster Univ., Hamilton, Canada*
Axel Jantsch - *Royal Institute of Tech., Kista, Sweden*

Workshop Registration Required
$100 - ACM/IEEE Member
$150 - Non-member

DSNOC is a one-day workshop devoted to Diagnostic Services in Network-on-Chips. DSNOC'08 is the second edition of this workshop and is organized in conjunction with the Design Automation Conference (DAC). For the Workshop Digest of the first edition, see http://www.date-conference.com/conference/2007/digest/.

Network-on-Chips (NoCs) are emerging as a new on-chip communication paradigm. Diagnostic services, such as test, debug, and on-line monitoring, are becoming important factors in designing next-generation NoC-based systems. The NoC infrastructure itself requires diagnostic services, and can also be used to support those for the entire system. Although significant research has been done in NoC design, there are many open and pressing issues regarding diagnostic services. The focus of this workshop is to explore them and their implications on system design.

9:00am SESSION 1: OPENING SESSION

9:00am Welcome Address

9:15am Keynote Address: Intelligent On-chip Interconnects: The 80-tile NoC and Beyond

Sriram R. Vangal - *Intel Corp., Hillsboro, OR*

The talk describes Intel's motivation to build an 80-tile teraflop research processor and details the prototype's modular, tiled design and NoC fabric. Challenges with performance validation of NoCs, along with I/O and memory bandwidth rationing in face of increasing communication demands will be addressed. We consider key objectives in the realization of future intelligent on-chip interconnects.

10:00am SESSION 2: FIRST INVITED TALK

Silicon Validation and Performance Monitoring for NoCs and SoCs

Miron Abramovici - *DAFCA , Framingham, MA*

Drew Wingard - *Sonics, Inc., Mountain View, CA*

We review an existing solution for in-system silicon validation and debug for SoCs and discuss its applicability to NoCs. We argue that real-time infrastructure functions such as validation, debug, diagnosis, and performance monitoring should be non-intrusive and hence should not use the NoC system at the time they analyze it. We present several performance monitoring applications that we have developed for the Sonics NoC and their integration in the reconfigurable infrastructure platform for SoCs.

10:30am POSTER SESSION AND COFFEE BREAK

11:00am SESSION 3

11:00am Dealing with Variability in NoC Links

Carles Hernández, Federico Silla, Vicente Santonja, José Duato - *Technical Univ. of Valencia, Valencia, Spain*

11:20am Agent-monitored Fault-tolerant Network-on-Chips: Concept, Hierarchy, and Case Study with FFT Application

Pekka Rantalla, Jouni Isoaho, Guang Liang, Hannu Tenhunen - *Univ. of Turku, Turku, Finland*

11:40am Performance and Reliability Monitoring in Network-on-Chips

Thilo Pionteck, Carsten Albrecht, Roman Koch, Erik Maehle - *Univ. of Lübeck, Lübeck, Germany*

12:00pm Monitoring Agent-based Autonomous Reconfigurable Network-on-Chip

Alexander W. Yin, Pasi Liljeberg, Zhonghai Lu, Hannu Tenhunen - *Univ. of Turku, Finland*

12:20pm Role of Error Control Coding in On-chip Communication Network: Advantages and Design Trade-offs

Amlan Ganguly, Partha Pratim Pande, Benjamin Belzer - *Washington State Univ., Pullman, WA*

12:40pm Luncheon Break in Room 303C

1:40pm SESSION 4: SECOND INVITED TALK

Physical Design Issues and Technology Trends in Networks-on-Chips

Eby G. Friedman - *Univ. of Rochester, Rochester, NY*

This presentation focuses on the physical level of the NoC design process. At this level, the global interconnects and routers are critical to NoC communication. Synchronization, clock distribution, and power delivery in complex on-chip systems are also primary areas that must be addressed in NoC-based systems. Possible trends in NoC development include merging 3-D integration and optical interconnect with NoC architectures.

2:10pm SESSION 5

2:10pm Hybrid NoC with Traffic Monitoring and Adaptive Routing for Future 3-D Integrated Chips

Ville Rantala, Teijo Lehtonen, Pasi Liljeberg, Juha Plosila - *Univ. of Turku, Finland*

2:30pm Early Fault Avoidance and Detection Techniques for Network-on-Chips

Kuei-Chung Chang - *Feng Chia Univ., Taichung, Taiwan*

2:50pm Design-for-Testability for Application of External Test Patterns in NoC

Vineeth Govind, Jaan Raik - *Tallinn Univ. of Tech., Tallinn, Estonia*

3:10pm Test Response Compression for Diagnosis in Volume Production

Mikael Söderbom, Erik Larsson - *Linköping Univ., Sweden*

3:30pm POSTER SESSION AND COFFEE BREAK

4:00pm PANEL SESSION

Is the Autonomous, Self-monitoring, Self-healing, Totally Reliable NoC the Building Block of Future Complex Electronic Systems?

Moderator:

Wayne Wolfe – *Georgia Institute of Tech., Atlanta, GA*

Panelists:

Partha Kundu – *Intel Corp., Santa Clara, CA*

Subhashish Mitra - *Stanford Univ., Palo Alto, CA*

Neal Stollon - *HDL Dynamics, Dallas, TX*

Drew Wingard - *Sonics, Inc., Mountain View, CA*

Since resources in future 2-D and 3-D NoCs are abundant, we build in lots of self-diagnostic and reconfiguration logic that makes the device degrade gradually. In the beginning of its life-time, 90-100% of its resources work. When more and more errors accumulate, fewer and fewer resources are operating correctly. But even after 20 years and 90% of its resources knocked-out, it still does useful work, only slower. This process of graceful degradation is entirely transparent to the users; only the degradation of performance is observed. NoC-based platforms exhibit a natural redundancy, but will they turn out to be the basic building blocks for future electronic systems?

5:00pm Closure

BEYOND SYNTAX AND SEMANTICS: INDUSTRY EXPERIENCES WITH OVL/SVA/PSL

RM: 207D

Organizer:
Harry Foster - *Mentor Graphics Corp., Addison, TX*

Workshop Registration Required
$75 - ACM/IEEE Member
$100 - Non-member

With the emergence of assertion language and library standards - such as the IEEE SystemVerilog Assertions (SVA), the IEEE Property Specification Language (PSL), and the Accellera Open Verification Library (OVL) - many design teams are investigating the possibility of integrating both simulation and formal verification's assertion-based verification techniques into their flow. Yet successful application of these standards in an industrial setting requires additional project team member skills and verification process maturity beyond a simple understanding of assertion language syntax and semantics. Hence, this workshop shares multiple experiences of applying the assertion standards on various industry projects - with a focus on answering these questions:

- What is required to mature a project team's ABV skills for successful adoption?
- What needs to be considered in terms of a project's ABV infrastructure (beyond commercial tools)?
- What metrics need to be defined (and gathered) to measure progress?
- What benefits are real industry projects seeing using OVL/SVA/PSL?

While selecting a property and assertion language standard is an integral step for adopting assertion-based techniques, it is not the entire solution. Methodology is equally important to effectively applying ABV. In fact, without enforcing a consistent methodology across multiple design and verification engineers (for example, a consistent means of reporting errors, enabling or disabling assertions, and assigning actions performed upon error detection), the ad hoc use of assertions can end up being unmanageable and disruptive to the overall verification process. Hence, this highly interactive workshop is designed to address these methodology concerns through examples by experienced practitioners, allowing the attendee the opportunity to ask detailed methodological and process questions.

The workshop begins with a brief historical introduction to Accellera's assertion language and library standards. Next, we introduce assertion patterns and timing diagrams, which are a powerful project training tool for assertion specification. We then present details on the role that the OVL played as a key component of a formal property methodology for an ASIC project. We present statistics on the common patterns used on the project. Next, we share experiences of adopting a SystemVerilog assertion methodology within an existing mature ASIC/SoC ABV flow. We present best practices and methodological recommendations from this experience. Then, we present best practices and process improvement metrics from the use of PSL within an advanced ASIC/SoC flow. Finally, we discuss reuse strategies for creating assertion-based IP and conclude with a brief roadmap presentation on the assertion language and library standards.

This session is organized and supported by Accellera's members and technical sub-committee members.

Speakers:
Sivan Rabinovich - *IBM Corp., Haifa, Israel*
Harry Foster - *Mentor Graphics Corp., Addison, TX*
Mike Turpin - *ARM, Cambridge,United Kingdom*
Erik Seligman - *Intel Corp., Hillsboro, OR*
Scott Meeth - *Sun Microsystems, Inc., Santa Clara, CA*
Joe Richards - *Broadcom Inc., Santa Clara, CA*

EFFECTIVE TECHNICAL WRITING

RM: 212A

Workshop Registration Required
$50 - ACM/IEEE Member
$75 - Non-member

Organizer:
Ann Marie Rincon - *ON Semiconductor, Pocatello, ID*

My technical work is outstanding - why didn't my paper get accepted? I thought my description was very clear - why was my thesis misunderstood? This class will provide answers to these questions and help engineers and programmers write clear, concise technical papers. The writing do's and don'ts covered in this class can be applied to other technical documents such as application notes, product specifications and emails.

The class will provide:

- A standard technical paper outline and a description of each section
- Tips for submitting a paper to an external conference
- General writing tips including do's and don'ts

Several lucky attendees will receive a copy of "The Elements of Style" by William Strunk Jr. and E.B. White.

Speaker:
Ann Marie Rincon - *ON Semiconductor, Pocatello, ID*

MAXIMIZING EFFICIENCY IN THE DEVELOPMENT CYCLE

RM: 303A

Workshop Registration Required
$50 - ACM/IEEE Member
$75 - Non-member

Organizer:
Marc Georges - *Ricochet PR, New York, NY*

Staying ahead in the global electronics industry means hitting shortened windows of opportunity with the best designs in order to be the first to market with a superior product. At the same time, businesses need to control the costs associated with managing their IT infrastructure. However, meeting those goals requires overcoming a number of technical challenges and business demands, including increased demand for computing power and licenses, shortened design cycles, demand for improved IT productivity. With no or little visibility into how IT resources are being used, companies are forced to make difficult decisions between productivity and quality to maintain a competitive advantage. This workshop will cover how grid solutions allow engineers and developers to focus on business-critical design and testing rather than IT resource provisioning and availability leading to higher revenues and profits and an overall increased competitive advantage.

Grid solutions provide businesses scalability across silos for a faster time to market with new designs. By leveraging the full capability of existing engineering infrastructure resources to run the most complex comprehensive simulations, tests, and models, users are able to accelerate the product development cycle and achieve a higher quality of results. In addition, virtualized IT resources impose sharing policies based on your business priorities. To manage IT assets more intelligently and reduce total cost of ownership, the most important projects receive the resources they need first, eliminating group and departmental resource silos. Plug and play integrations for leading applications enable more simulations and verifications in a shorter amount of time, reducing management complexity and deployment costs. By simplifying and streamlining your IT environment, grid solutions allow their users to fully utilize existing hardware and software assets without thinking about it.

Speakers:
Mike Broxterman - *Qualcomm, Inc., San Diego, CA*
MinQi Bao - *Cadence Design Systems, Inc., San Diego, CA*

ELEVATING CONFIDENCE IN DESIGN IP THROUGH MUTATION-BASED ANALYSIS TECHNOLOGY

Monday, June 9 / 9:00am - 12:00pm

***Presented by:* Certess, Inc. / STMicroelectronics / Brian Bailey Consulting**

Reuse of Intellectual Property (design IP) has taken center stage in the effort to enable today's SoC design. One of the most critical of these challenges is the functional verification of the design IPs and integrating it into an SoC.

STMicroelectronics and Certess, formed a partnership to identify issues in the verification of design IP that resulted in the advent of Certitude, an innovative verification solution using Mutation-based analysis.

Certitude delivers greater visibility into functions of the design IPs which are not sufficiently verified. It highlights areas of the design for which checking is insufficient, features for which tests do not exist, and provides an overall measure of verification completeness.

Participants in the session will be introduced to Certitude. They will gain hands-on experience in setting up Certitude for an existent verification environment, analyzing specific verification weaknesses, and improving the verification strategy.

IP VALIDATION FOR MACRO AND EMBEDDED SoC

Monday, June 9 / 2:00 - 5:00pm

***Presented by:* Apache Design Solutions, Inc.**

Increasing complexity of custom designed IPs in SoCs drives the need for a power noise verification flow that allows the capture of information in the presence and the impact of the IP to the SoC. Using IP models based on port-based abstract views or rule-based current distribution when simulating SoC power and noise does not provide the complete picture and often times results in designs with inadequate connections of the top-level power grid to these IP blocks.

A transistor-accurate power and noise analysis flow based on Apache's RedHawk platform enables designers to verify the power integrity of IPs at the block-level and creates a comprehensive model of varying levels of complexity for SoC-level analysis. Reduced models can be used for quick top-level analyses and early power grid planning whereas detailed models can be used for chip-level signoff verification. This IP validation methodology allows designers to verify power grid connection problems, identify high voltage drop causing mechanisms, and isolate electo-migration bottlenecks. To further ensure the integrity of IP operation, package models should be included in the SoC level analysis.

ADVANCED METHODOLOGIES IN VALIDATING AND INTEGRATING HIGH SPEED SERIAL INTERCONNECTS IN THE ULTRA DEEP SUB-MICRON CMOS ERA

Tuesday, June 10 / 2:00 - 5:00pm

***Presented by:* Synopsys, Inc. / Open-Silicon, Inc.**

Multi-gigabit per second serial interconnects such as PCIe 2.0, SATA II and "double-rate" XAUI, with speeds up-to 6.25 Gb/s are being integrated into 65-nm and 45-nm CMOS, mostly digital SoCs, causing designers to re-think the integration, verification and validation tasks. Integration issues today involve a much closer interactions between design, packaging, testing and signoff domains. Pre-layout verification in terms of device mismatch and Monte Carlo simulations is becoming a poor predictor of performance necessitating new methodologies for verification. This requires an understanding of the impact of systematic variations based on physical changes to the device. Silicon validation of SerDes IP now requires new techniques including real-time visibility into the serial link performance with the addition of substrate/supply noise generators. System-level validation now requires many more customized steps using the multiple types of real-time performance monitors available in the base IP.

INTEGRATION, TEST, REPAIR AND DEBUG OF EMBEDDED MEMORY IP IN AN SoC

Wednesday, June 11 / 8:00 - 11:00am

Presented by: ***Virage Logic Corp.***

Selecting optimal memory IP becomes one of the critical choices that an SoC designer must make for the success of the chip. Post tape out, issues can arise in silicon and manifest themselves in embedded memories, so having the ability to quickly and easily locate the source of the silicon issue is paramount to realizing aggressive yield targets and meeting profitability.

But, what are the key criteria for choosing memory IP besides the main characteristics - speed, area, power, and leakage? Without a doubt, the most important criteria is the test and repair solution of the embedded memory IP. The right solution choice can result in higher reliability, higher yield, and overall lower cost of the chip.

This session will guide users through Virage Logic's silicon proven STAR™ Memory System solution; providing hands on experience for the creation, integration, and verification of the IP into a sample design.

WHAT, WHY AND HOW: USING A CHIP PREDICTION SYSTEM TO FIND THE BEST IP SOLUTION FOR YOUR NEXT CHIP

Wednesday, June 11 / 2:00 - 5:00pm

Presented by: ***ChipEstimate.com / Chartered Semiconductor Manufacturing, Inc. / Virage Logic Corp.***

This hands-on tutorial will guide attendees in using the InCyte system to meet the challenges of finding relevant IP, assessing why some IP addresses requirements while other IP may not, and then exploring how that IP will impact their next chip project. All this is done before the traditional IC design flow begins, as the methodology shown uses automation software to make the chip project "go, no-go" decision, and to refine and optimize a specification at the earliest stage of the process. Better decisions earlier translate into lowered risk, faster design turn-around time, and lower overall chip cost.

Attendees will learn how to find IP and run an InCyte chip estimation, perform a what-if analysis on size, power, leakage and cost figures to optimize the specifications, and share results with management, colleagues and customers.

HARDENED DDR PHY INTEGRATION

Thursday, June 12 / 9:00am - 12:00pm

Presented by: ***Denali Software / SiSoft, Inc.***

DDR PHY design has become increasingly complex as memory speeds race to DDR3-1600 MT/s and beyond. Integrating an IP provider's PHY saves some of the headache of understanding complex memory sub-system timing, but the package and board must be analyzed as well. This tutorial highlights the issues involved with integrating a DDR hardened PHY into a complete system, which includes the package and board. SiSoft Quantum-SI will be used to explore these issues when working with a hardened PHY design provided by Denali's Databahn IP group. Tutorial attendees will learn how to:

1. Use a structured process to choose I/Os, package type (wirebond or flipchip), and board requirements
2. Explore various signal-to-power ratios and decoupling capacitance
3. Perform signoff analysis to ensure the entire memory sub-system will meet timing and signal integrity requirements for JEDEC DDR operation

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Association for Computing Machinery (ACM)

ACM is an educational and scientific society uniting the world's computing educators, researchers and professionals to inspire dialogue, share resources and address the field's challenges. ACM strengthens the profession's collective voice through strong leadership, promotion of the highest standards, and recognition of technical excellence. ACM supports the professional growth of its members by providing opportunities for life-long learning, career development, and professional networking. For more information, please visit http://www.acm.org.

The ACM Digital Library and Guide to Computing Literature are the definitive online resources for computing professionals. Richly interlinked, they provide access to ACM's collection of publications and bibliographic citations from the universe of published computing literature. http://www.acm.org/dl

Additionally, ACM has 34 Special Interest Groups (SIGs) that focus on different computing disciplines. More than half of all ACM members join one or more of these Special Interest Groups. The SIGs publish newsletters and sponsor important conferences such as SIGGRAPH, OOPSLA, DAC, SC and CHI, giving members opportunities to meet experts in their fields of interest and network with other knowledgeable members. http://www.acm.org/sigs. Become an ACM member today and join thousands of other leading professionals, researchers and academics who benefit from all ACM has to offer. Join ACM online at http://www.acm.org, or contact ACM directly by phone: 800-342-6626 (Us and Canada) or 212-626-0500 (Global), by fax: 212 - 944-1318, or by e-mail: acmhelp@acm.org. Hours of operation are from 8:30am - 4:30pm Eastern Time.

ACM/SIGDA

The Resource for EDA Professionals ACM/SIGDA (Special Interest Group on Design Automation) has a tradition of over forty years of supporting conferences and the EDA profession. In addition to sponsoring DAC, SIGDA sponsors ICCAD, DATE, and ASP-DAC, plus approximately 15 smaller symposia and workshops. SIGDA provides a broad array of additional resources to our members, to students and professors, and to the EDA profession in general. SIGDA organizes the Univ. Booth and Ph.D. Forum at DAC and the CADathlon at ICCAD, and funds various scholarships and awards. SIGDA provides its members with full access to SIGDA-sponsored conference proceedings in the ACM Digital Library and the SIGDA E-Newsletter containing information on upcoming conferences and funding opportunities, emailed to SIGDA members twice each month. The SIGDA E-Newsletter also includes SIGDA News which highlights the most relevant events in the EDA and semiconductor industry, and the "What is...?" column that brings to the attention of EDA professionals the most recent topics of interest in design automation. SIGDA has recently initiated the creation of eight Technical Committees in various areas of EDA, ranging from Physical Design and Logic Synthesis, to system-level Design, Low Power Design, Reconfigurable Computing, Testing, Verification, and Emerging Technologies. Attend the 11th Ph.D. Forum/Member Meeting on Tuesday evening to find out how the Technical Committees provide a link between SIGDA activities and various technical areas in EDA. Finally, SIGDA provides strong support for the ACM journal TODAEs (Transactions on Design Automation of Electronic Systems).

For further information on SIGDA's programs and resources, see http://www. sigda.org. In addition, SIGDA members may also want to consider joining our parent organization, ACM. ACM membership provides access to a variety of ACM products and resources, including discounts on conferences, subscriptions to ACM journals and magazines, and the ACM Digital Library, an invaluable IT resource. For further details, see ACM's home page at http://www.acm.org. As an EDA professional, isn't it time YOU joined SIGDA?

45th DAC Proceedings DVD

Additional copies of the 45th DAC Proceedings DVD may be ordered prepaid from:

ACM Order Department
P.O. Box 11414, New York, NY, 10286-1414
Fax: 1-800-342-6626 (US and Canada)
Fax: 1-212-944-1318 (all other countries)
email: orders@acm.org

SIGDA/DAC University Booth

This year marks the 21st University Booth at the Design Automation Conference. The booth is an opportunity for university researchers to display their results and to interact with visitors from industry. Priority is given to presentations that complement the conference technical program. Demos that highlight benchmark results are also encouraged. The Design Contest winners, DAC speakers, and PhD Forum participants are invited to give demonstrations presenting their work at the University Booth. This year, look for a completely redesigned booth courtesy of our sponsor, Mentor Graphics Corp. The schedule of presentations is published at the conference and is also available on the SIGDA website at http://www.sigda.org/programs/Ubooth/Ubooth2008/. The organizers thank the Design Automation Conference for its continued support of this project.

EDA Consortium

The EDA Consortium (EDAC) is the international industry association for the providers of tools and services that enable engineers to create the world's electronics products. Its mission is to promote the health of the EDA industry by addressing common industry needs and providing valued services. By publishing the Market Statistics Service (MSS) EDAC enables worldwide tracking of revenue for CAE, IP, PCB, ESL and DFM. By co-sponsoring the prestigious annual Phil Kaufman Award, the EDA Consortium and the IEEE Council on EDA bring industry-wide recognition to distinguished contributions to EDA. As a co-sponsor of DAC and DATE, the EDA Consortium represents the interests of exhibiting companies. EDAC members influence industry initiatives by participating on committees to address common needs as well as play a positive role in reducing costs for the industry and its customers. Examples of committee accomplishments include an EDA operating systems roadmap, anti-piracy education, licensing guidelines, and the reduction of governmental export controls. EDAC offers international forums and symposiums which are well attended by industry CEOs, executives, press, and analysts. These events cover topics of interest to emerging and large EDA companies alike. EDA Consortium members receive a 10% discount on DAC booth/suite space. For more information call 408-287-3322 or visit www.edac.org. EDAC is located in San Jose, CA, USA.

Design Automation Conference Sponsors

IEEE

A non-profit organization, IEEE is the world's leading professional association for the advancement of technology.

IEEE/Council on Electronic Design Automation

The Council on Electronic Design Automation (CEDA) is an IEEE Council formed in 2005 by the IEEE Technical Activities Board. CEDA aims to bring together the EDA-related activities that run through many of the IEEE's societies, conferences and workshops. CEDA's responsibilities include sponsorship of several conferences and publications, such as ICCAD, DAC, and the Transactions on CAD and the sponsorship of a Distinguished Speaker Series. Members of CEDA include the IEEE Antennas and Propagation, Computer, Circuits and Systems, Electron Devices, Microwave Theory and Techniques, and Solid State Circuits Societies. For more information on CEDA, go to www.ieee-ceda.org.

IEEE/Circuits and Systems Society

The IEEE Circuits and Systems Society (CASS) is one of the largest societies within IEEE and in the world devoted to the analysis, design, and applications of circuits, networks, and systems. It offers its members an extensive program of publications, meetings and technical and educational activities, encouraging an active exchange of information and ideas. The Society's peer reviewed publication activities include: Trans. on CAS-Part I: Regular Papers; Trans. on CAS-Part II: Express Briefs; and Trans. on CAS for Video Technology. In addition, there are Trans. on CAD; Trans. On VLSI; Trans. on Multimedia; Trans. on Mobile Computing; and Trans. on Biomedical Circuits and Systems which are co-sponsored with IEEE sister societies. Also available is the CASS Electronic Newsletter. CASS sponsors or co-sponsors a number of international conferences which include the Design Automation Conference (DAC), the Int'l Conference on Computer-Aided Design (ICCAD) and the Int'l Symposium on Circuits and Systems (ISCAS). A worldwide comprehensive program of advanced workshops including a new series on "Emerging Technologies in Circuits and Systems," as well as our continuing education short courses, bring to our worldwide membership the latest developments in cutting-edge technologies of interest to industry and academia alike.

The IEEE CASS has been serving its membership for over 50 years with such member benefits as:

- Discounts on Society publications, conferences and workshops (including co-sponsored publications and conferences)
- The Society Magazine which includes articles on emerging technologies, society news and current events
- Opportunities to network with peers and experts within our 17 focused committee meetings, the local events of over 60 chapters and more than 20 annual conferences/ workshops
- Opportunity to read and review papers, write articles and participate in the Society's government
- The CASS Electronic Newsletter
- And all the personal and professional benefits of IEEE CASS/CANDE/CEDA membership

IEEE/Computer Aided Network Design

Computer Aided Network Design (CANDE) is a joint technical committee of the IEEE Circuits and Systems Society and the Council on Electronic Design Automation. CANDE is dedicated to bringing design automation professionals together to further their education, to assist in building relationships, and to sponsor initiatives which grow the CAD/EDA industry. CANDE sponsors a workshop in the Fall to address emerging technologies and to provide an opportunity for the generation of new ideas. CANDE is the sponsoring technical committee from CASS for both DAC and ICCAD.

For more information, please contact:

IEEE/CASS/CANDE
445 Hoes Lane
Piscataway, NJ 08854
Phone: 732-465-5821
Email: cas-info@ieee.org
Web: www.ieee-cas.org

Marie R. Pistilli Women in EDA Achievement Award

Louise Trevillyan - *Research Staff Member, Design Automatin Dept., IBM T. J. Watson Research Center*

For her significant conrtibutions in helping women advance in the field of EDA technology.

P.O. Pistilli Undergraduate Scholarships for Advancement in Computer Science and Electrical Engineering

The objective of the P.O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering, and Computer Science from under-represented groups (women, African American, Hispanic, Native American, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship and SIGDA continues to administer the program for DAC. DAC normally funds two or more $4000 scholarships, renewable up to five years, to graduating high school seniors.

The 2008 winners are:

Tiffany Lynn Stokley - *Univ. of Richmond, VA*
Samantha Jo Skinger - *Carnegie Mellon Univ., Pittsburgh, PA*

For more information about the P.O. Pistilli scholarship, contact Cherrice Traver - *ECE Dept., Union College, Schenectady, NY 12308. email: traverc@union.edu.*

A. Richard Newton Graduate Scholarships

The DAC Executive Committee has chosen to name our existing DAC Graduate Scholarships after the late Professor A. Richard Newton. We feel that supporting young faculty and graduate research is an appropriate way to honor his vision and carry out some of his goals. Each year the Design Automation Conference sponsors several $24,000 scholarships to support graduate research and study in Design Automation (DA), with emphasis in "design and test automation of electronic and computer systems". Each scholarship is awarded directly to a Univ. for the Faculty Investigator to expend in direct support of one or more DA graduate students. The criteria for granting such a scholarship expanded in 1996 to include financial need. The criteria are: the academic credentials of the student(s); the quality and applicability of the proposed research; the impact of the award on the DA program at the institution; and financial need. Preference is given to institutions that are trying to establish new DA research programs.

Advisor:
Janet Meiling Wang - *Univ. of Arizona, Tucson, AZ*
Students:
Alexander V. Mitev, Jin Sun
Modeling and Analysis of Analog/Mixed-signal Designs with CMOS Device Mismatch due to Process Variations

Advisor:
Sangyeun Cho - *Univ. of Pittsburgh, Pittsburgh, PA*
Students:
Hyunjin Lee, Musfiq Niaz Rahman
Bridging Technology Fragility and Next-Generation Many-Core Processor Architectures and Systems Research

2007 Phil Kaufman Award for Distinguished Contributions to EDA

Sponsored by the EDA Consortium and IEEE Council on EDA

Dr. Robert K. Brayton, *Cadence Distinguished Professor of Electrical Engineering and Computer Science, Univ. of California, Berkeley, CA*

Robert K. Brayton is the recipient of the prestigious 2007 Phil Kaufman Award for his contributions to logic synthesis and formal verification which have aided the development of today's complex chips.

2008 IEEE Emanuel R. Piore Award

Dr. Richard F. Rashid - *Microsoft Corp., Redmond, WA*

For contribution the design of modern operating systems, and for innovation and leadership in industrial research.

2008 IEEE Fellows

Nikil Dutt - *Univ. of California, Irvine, CA*

For contributions to architecture description languages for the design and exploration of customized processors.

Laung-Terng Wang - *SynTest Tech., Inc., Sunnyvale, CA*

For leadership in practical design-for-test of integrated circuits.

ACM Turing Award

Edmund M. Clarke - *Carnegie Mellon Univ., Pittsburgh, PA*
E. Allen Emerson - *Univ. of Texas, Austin, TX*
Joseph Sifakis - *CNRS-Verimag Laboratory, Gieres, France*

For their role in developing model-checking into a highly effective verification technology, widely adopted in the hardware and software industries.

ACM Fellow

Donald E. Thomas - *Carnegie Mellon Univ., Pittsburgh, PA*

For contributions to computer-aided design of integrated circuits and systems.

Outstanding Contribution to ACM Award

Robert Walker - *Kent State Univ., Kent, OH*

For a sustained record of dedicated and conscientious leadership within the ACM Special Interest Groups, including service as Chair of the SIG Governing Board, Chair of SIGDA, SGB Representative to Council, as well as leadership in ACM conference organization.

SIGDA Distinguished Service Award

Sung Kyu Lim - *Georgia Institute of Tech., Atlanta, GA*

For exemplary service to ACM/SIGDA and the Design Automation Conference as director of the Univ. Booth program.

SIGDA Outstanding New Faculty Award

Subhasish Mitra - *Stanford Univ., Palo Alto, CA*

For a junior faculty member early in his/her academic career who demonstrates outstanding potential as an educator and/or researcher in the field of electronic design automation.

ACM Transactions on Design Automation of Electronic Systems (TODAES) 2008 Best Paper Award

Disjunctive image computation for software verification

ACM Transactions on Design Automation of Electronic Systems, Volume 12, Issue 2, April 2007, Article No. 10

Chao Wang, Franjo Ivančić, Aarti Gupta - *NEC Labs, Princeton, NJ*
Zijiang Yang - *Western Michigan Univ., Kalamazoo, MI*

Student Design Contest

AWARD CONTRIBUTORS

STUDENT DESIGN CONTEST CO-CHAIRS

Byunghoo Jung - *Purdue Univ., West Lafayette, IN*
William Bowhill - *Intel Corp., Hudson, MA*

The Student Design Contest promotes excellence in the design of electronic systems by providing a competition for graduate and undergraduate students at universities and colleges. It is co-organized by DAC and ISSCC. This year we received nearly 50 submissions in three categories: operational systems, operational chips and conceptual designs based on simulation. Nine award winners were selected. The Student Design Contest is co-sponsored by DAC, industry sponsors and ISSCC.

Awards will be presented in the DAC Pavilion on the exhibit floor, Booth #364 on Monday, June 9 from 12:00 - 1:00pm. The ceremony will include brief overview presentations from each winning project team.

2008 DAC/ISSCC STUDENT DESIGN CONTEST WINNERS

- **A 242mW, 10mm^2 1080p H.264/AVC High Profile Encoder Chip**

Yu-Kun Lin, De-Wei Li, Chia-Chun Lin, Tzu-Yun Kuo, Sian-Jin Wu, Wei-Cheng Tai, Wei-Cheng Chang, Tian-Sheuan Chang - *National Chiao-Tung Univ., Hsinchu, Taiwan*

- **The Design of a Low Power Carbon Nanotube Chemical Sensor System**

Taeg Sang Cho, Kyeong-Jae Lee, Jing Kong, Anantha P. Chandrakasan - *Massachusetts Institute of Tech., Cambridge, MA*

- **iVisual: An Intelligent Visual Sensor SoC with 2790fps CMOS Image Sensor and 205GOPS/W Vision Processor**

Chih-Chi Cheng, Chia-Hua Lin, Chung-Te Li, Liang-Gee Chen - *National Taiwan Univ., Taipei, Taiwan*
Samuel C. Chang - *Massachusetts Institute of Tech., Cambridge, MA*

- **XCXO: An Ultra-low Cost Ultra-high Accuracy Clock System for Wireless Sensor Networks in Harsh Remote Outdoor Environments**

Thomas Schmid, Jonathan Friedman, Zainul Charbiwala, Young H. Cho, Mani B. Srivastava - *Univ. of California, Los Angeles, CA*

- **Vision Platform for Mobile Intelligent Robot Based on 81.6 GOPS Object Recognition Processor**

Donghyun Kim, Kwanho Kim, Joo-Young Kim, Seungjin Lee, Hoi-Jun Yoo - *KAIST, Daejon, Republic of Korea*

- **A MIPS R2000 Implementation**

Nathaniel Pinckney, Thomas Barr, Michael Dayringer, Matthew McKnett, Nan Jiang, Carl Nygaard, David Money Harris - *Harvey Mudd College, Claremont, CA*
Joel Stanley, Braden Phillips - *Univ. of Adelaide, Adelaide, Australia*

- **PicoCube: A 1cm$_3$ Sensor Node Powered by Harvested Energy**

Yuen-Hui Chee, Michael Koplow, Michael Mark, Nathan Pletcher, Michael Seeman, Fred Burghardt, Dan Steingart, Jan Rabaey, Paul Wright, Seth Sanders - *Univ. of California, Berkeley, CA*

- **A 3Gbps/30K-rule Virus-detection Processor Embedded with Adaptively Dividable Dual-port BiTCAM for Mobile Devices**

Chieh-Jen Cheng, Chao-Ching Wang, Kuan-Ching Chuang, Tai-An Chen, Tien-Fu Chen, Jinn-Shyan Wang - *National Chung-Cheng Univ., Chia-Yi, Taiwan*

- **Silicon Odometer: An On-chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits**

Tae-Hyoung Kim, Randy Persaud, Chris Hyung-il Kim - *Univ. of Minnesota, Minneapolis, MN*

GLOBAL SEMICONDUCTOR TEST CONSORTIUM CONFERENCE (GSC)

Wednesday, June 4 - Friday, June 6: Hilton Hotel, San Diego, CA

This year, the Semiconductor Test Consortium (STC) will host or participate in 19 international events, tradeshows and meetings, including the Global STC Conference, which will be held June 4 - 6, 2008, in San Diego, CA. Fittingly, this year's theme is "Collaborative Solutions Beyond 2010." One of the conference goals is to bring the worldwide design and test communities closer together to discuss the mutual challenges we face as an industry. Additional information regarding this unique event, can be found at: **http://www.semitest.org/events/GSC_2008/**.

MEMOCODE 2008: SIXTH ACM-IEEE INTERNATIONAL CONFERENCE ON FORMAL METHODS AND MODELS FOR CODESIGN

RM:304B

Thursday, June 5 - Saturday, June 7

The goal of MEMOCODE 2008, the sixth in a series of successful international conferences, is to gather together researchers and practitioners in the field of the design of modern hardware and software systems to explore ways in which future design methods can benefit from new results on formal methods.

MEMOCODE 2008 will be a relaxed, single-track conference bringing together practitioners from the Hardware, Software, and Embedded systems design and formal analysis communities. MEMOCODE will include the results of its recent month-long codesign contest in addition to invited speakers, and regular paper sessions. This year, MEMOCODE will feature a hands-on Saturday tutorial on Efficient System Codesign using Bluespec. This tutorial will also be available separately to DAC attendees for a nominal fee.

http://svl1.cs.pdx.edu/memocode08/

NANOARCH '08: IEEE/ACM SYMPOSIUM ON NANOSCALE ARCHITECTURES

RM: 212A

Thursday, June 12 - Friday, June 13 / 8:00am - 6:00pm

Registration Required
$250 - ACM/IEEE member $330 - Non-member $200 Student ACM/IEEE member

Moore's law based scaling is rapidly approaching a "brick wall" as we enter the nanoelectronic regime. Novel silicon and non-silicon nanoelectronic devices are being developed to explicitly address this problem. Similarly, while defect and fault-tolerance techniques are designed under the assumption that a system is composed largely of correctly functioning units, this is no longer true in emerging nanoelectronics. In addition, nanoelectronics offers massive parallelism on a scale significantly beyond anything we have seen before, yet very few commercial massively parallel applications are envisioned. Also, while current computer aided design tools and methodologies can barely manage billion-transistor chips, how can trillion-device chips that nanoelectronics promises be designed? Visit the NANOARCH website!

The purpose of the NANOARCH symposium is to be a forum for the presentation and discussion of novel architectures and design methodologies by considering these issues in future nanoscale implementations. The symposium seeks to build on the successes of NANOARCH in 2005, 2006 and 2007. NANOARCH is interested in novel architectures including massively parallel, biologically inspired as well as those that are defect and fault tolerant, case studies on defect, fault and yield models, experimental reliability evaluation, validation frameworks, computer aided simulation, design tools and emerging computational models for nanoelectronics.

General Co-chairs:
Ramesh Karri - *Polytechnic Univ., Brooklyn, NY*
Steven P. Levitan - *Univ. of Pittsburgh, Pittsburgh, PA*

Keynote Talk (Open to all DAC attendees)
Speaker:
R. Stanley Williams - *Hewlett Packard, Co., Palo Alto, CA*
Thursday, June 12 / 11:00am - 12:00pm

Panel Session (Open to all DAC attendees)
Non-CMOS NanoElectronics - Will It Ever Be Real?
Organizer/Moderator:
Paul D. Franzon - *North Carolina State Univ., Raleigh, NC*
Thursday, June 12 / 4:00 - 5:30pm

Keynote Talk (Open to all DAC attendees)
Speaker:
James R. Heath - *California Institute of Tech., Pasadena, CA*
Friday, June 13 / 11:00am - 12:00pm

In addition to technical and invited sessions, the program will include a keynote speaker and panel discussion, each open to all DAC participants.

The two day symposium will also include several technical sessions on topics such as reliable nanoarchitectures, CAD for nanoelectronic devices and circuits, defect tolerant memories and circuits, and nanoelectronic circuits. Website: **http://nanoarch.org**

7TH SYMPOSIUM ON ELECTRONIC SYSTEM-LEVEL DESIGN WITH SYSTEMC

Sunday, June 8, 4:00 - 7:00pm and Monday, June 9 / 12:00 - 5:00pm

ESL technologies continue to grow in importance for architectural exploration, performance analysis, the building of virtual platforms for software development and functional verification. The development of standards such as IEEE 1666, SystemC and the OSCI transaction-level modeling standard, TLM-2.0, mark significant milestones in enabling standards-based solutions.

Now in its 7th year, the Symposium on Electronic System-Level Design with SystemC provides an open forum for SystemC users, tool suppliers, and academia to interact and learn about the latest advances in system-level design with SystemC. Sponsored by the Open SystemC Initiative, the symposium features presentations from users and industry experts who discuss SystemC design methodology and real-world user experiences.

Free to Industry Professionals!

Opening Session and Reception – North American SystemC Users Group Meeting

Sunday, June 8 / 4:00 - 7:00pm, Hilton Anaheim Hotel, 777 Convention Way, Room: Pacific Ballroom A

NASCUG provides a unique forum for sharing SystemC experiences among business, research and universities, while influencing the growth and evolution of SystemC standards. The meeting includes technical presentations on the OSCI TLM-2.0 standard, SystemC and analog-mixed signal design, and SystemC tool flows and methodologies.

Panel Discussion: Real World Advantages of the OSCI TLM-2.0 Standard for Interoperability and IP Reuse

Monday, June 9 /12:00 - 2:00pm, Ballroom E, Anaheim Convention Center

Complimentary lunch provided; doors open at 11:30am

This informative lunch panel brings together a unique combination of thought leaders in electronic systems, software, and semiconductors for a lively discussion on the economic impact of ESL, SystemC and transaction-level modeling (TLM). Find out why the release of the OSCI TLM-2.0 standard is important to them and how their organization is using it today to increase design success and improve productivity. You'll also hear their predictions on the future of TLM-2.0 and how it can create new value by enabling significantly earlier architecture definition and software development for SoC designs.

Special Workshop: OSCI TLM-2.0 in 2008 – A Leap Forward for Transaction-Level Modeling Standards

Monday, June 9 / 2:00 - 5:00pm, Ballroom E, Anaheim Convention Center

This workshop presents details of the finalized OSCI TLM-2.0 standard. This standard marks the culmination of several years of intensive work by the OSCI TLM Working Group. TLM-2.0 explicitly addresses the interoperability of memory-mapped bus models at the transaction level and provides a foundation and framework for the transaction-level modeling of other protocols. Robust examples and documentation will be presented. Attendees will be provided with a comprehensive workshop guide containing course materials.

Open SystemC Initiative
www.systemc.org

Sponsored by:
ARM, Cadence Design Systems, Inc. , CoWare, Inc., Doulos, ESLX, Forte Design Systems, JEDA Tech., Mentor Graphics Corp., Synopsys, Inc., Virtutech

GIGASCALE SYSTEMS RESEARCH CENTER QUARTERLY WORKSHOP

Sunday, June 8 - Anaheim Hilton

www.gigascale.org

6TH IEEE SYMPOSIUM ON APPLICATION SPECIFIC PROCESSORS

RM: 204C - 204B LUNCH

Sunday, June 8 and Monday, June 9 / 8:30am - 6:30pm

Registration Required
$410 - IEEE Member
$525 - Non-member
$245 - Student

GENERAL CHAIRS:
Paolo Ienne - *École Polytéchnique Fédérale de Lausanne, Lausanne, Switzerland*
Peter Petrov - *Univ. of Maryland, College Park, MD*

PROGRAM CHAIRS:
Alex Orailoglu - *Univ. of California, San Diego, La Jolla, CA*
Laura Pozzi - *Univ. of Lugano, Lugano, Switzerland*

PUBLICITY CHAIR:
Cristina Silvano - *Politecnico di Milano, Milano, Italy*
SPECIAL SESSIONS CHAIR:
Grant Martin - *Tensilica, Santa Clara, CA*

PUBLICITY CHAIR:
Tulika Mitra - *National Univ. of Singapore, Singapore*

E-MEDIA CHAIR:
Ismet Bayraktaroglu - *Sun Microsystems, Inc., Santa Clara, CA*

Dramatic embedded systems volumes and associated market segments forcea reevaluation of the best way to satisfy the possibly conflicting demands placed on processor designs. Domain-specific embedded processors, such as network, automotive, cellular and others, present interesting architectural refinements, albeit at the cost of splintering the embedded processor market. Reprogrammable and/or reconfigurable embedded processors provide an alternative approach, capable of delivering single, fixed-silicon architectures, thus amortizing design and manufacturing costs across large volumes, yet necessitating an answer to the challenge of effective customization of embedded processors. The IEEE Symposium on Application Specific Processors explores (micro)architectural design approaches and trade-offs and compiler technologies, for both domain-specific and customizable embedded processors. The symposium is a forum wherein challenges and solutions are explored, discussed, and compared. The programme of this year's symposium is available on http://sasp-conference.org.

IEEE INTERNATIONAL WORKSHOP ON HARDWARE-ORIENTED SECURITY AND TRUST (HOST-2008)

RM: 204A - 206A LUNCH

Monday, June 9 / 8:30 - 5:45pm

Chip design and fabrication is becoming increasingly vulnerable to malicious activities and alterations with globalization. This has raised serious concerns regarding possible threats to military systems, financial infrastructures and even household appliances. An adversary can introduce a Trojan designed to disable and/or destroy a system at some future time (Time Bomb) or the Trojan may serve to leak confidential information covertly to the adversary. The 1st IEEE International Workshop on Hardware-Oriented Security and Trust (HOST 2008) is an open forum for discussions and innovations on these issues and others related to this year's theme "Trojan Detection and Isolation".

Themes covered at the workshop include:

- Trojan detection and isolation
- Authenicating foundry of origin
- Side channel analysis/attacks
- Watermarking
- IP security/FPGA design security
- Cryptographic techniques for hardware security
- Physical unclonable functions (PUFs)
- Embedded and distributed systems security
- Hardware intrusion detection and prevention
- Security engineering
- Scan-chain encryption

This workshop is for researchers in academia, industry and government agencies who are interested in hardware security and trust to attend this workshop.

Keynote and Invited Speakers:
Dean Collins - *Deputy Director, Microsystems Tech. Office, DARPA*

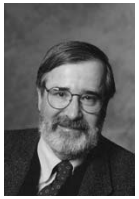
Registration Required
$410 - IEEE Member
$525 - Non-member
$245 - Student

2007 ACM TURING AWARD WINNERS

RM: BALLROOM ABC

Monday, June 9 / 2:00 - 4:00pm

We are privileged to have as guest speakers the ACM Turing Award winners who have been recognized with the highest honor in the area of computing for their role in developing Model-checking into a highly effective verification technology, widely adopted in the hardware and software industries.



Edmund M. Clarke is the FORE Systems University Professor of Computer Science and Professor of Electrical and Computer Engineering at Carnegie Mellon University. He is the former editor-in-chief of Formal Methods in Systems Design and a co-founder of the International Conference on Computer Aided Verification. He received a Technical Excellence Award from the Semiconductor Research Corporation in 1995. He was a co-winner with Randy Bryant, Allen Emerson, and Kenneth McCMillian of the ACM Kannellakis Award in 1998. In 1999 he received an Allen Newell Award for Excellence in Research from the Carnegie Mellon Computer Science Department. He received the IEEE Harry M. Goode Memorial Award in 2004, and was elected to the National Academy of Engineering in 2005. He was a recipient with Allen Emerson and Joseph Sifakis of the 2007 ACM Turing Award, and is the 2008 recipient of the Herbrand Award for Automated Reasoning. He is a Fellow of the ACM and IEEE and a member of Sigma Xi and Phi Beta Kappa. Dr. Clarke received a B.A. degree in mathematics from the University of Virginia, a M.A. degree in mathematics from Duke University, and a Ph.D. degree in computer science from Cornell University. He has taught at Duke and Harvard.

E. Allen Emerson is an endowed professor in computer sciences at the University of Texas at Austin. He was a recipient of the 2006 Test-of-Time Award from the IEEE Symposium on Logic in Computer Science (LICS) for his research on efficient model checking in highly expressive temporal logics. He is co-winner of the 1998 ACM Kanellakis Theory and Practice Award for his foundational role in the development of symbolic model checking. He has served on the editorial boards of several leading journals in applied logic and formal methods, including ACM Transactions on Computational Logic, Formal Aspects of Computing, and Formal Methods in Systems Design. He serves on the steering committee of the International Symposium on Automated Technology for Verification and Analysis (ATVA) as well as the International Conference on Verification, Model Checking, and Abstract Interpretation (VMCAI). Emerson received a B.S. degree in mathematics from University of Texas at Austin, and a Ph.D. in applied mathematics from Harvard University.

Joseph Sifakis is CNRS researcher and the Founder of Verimag laboratory, in Grenoble, France. He studied Electrical Engineering at the Technical University of Athens and Computer Science at the University of Grenoble. Joseph Sifakis is recognized for his pioneering work on both theoretical and practical aspects of Concurrent Systems Specification and Verification. He contributed to emergence of the area of model-checking, currently the most widely used method for the verification of industrial applications. Joseph Sifakis is the Scientific Coordinator of the European Network of Excellence ARTIST2 on Embedded Systems Design, the chair of "Chamber B" (Public Research Organisations) of ARTEMISIA, which is the Industrial Association within the ARTEMIS European Technology Platform on Embedded Systems, and the director of the Carnot Institute "Intelligent Software and Systems" in Grenoble. Joseph Sifakis is a member of the editorial board of several journals, co-founder of the International Conference on Computer Aided Verification (CAV) and a member of the Steering Committee of the EMSOFT (Embedded Software) conference. Joseph Sifakis has received with Ed Clarke and Allen Emerson for their contribution to Model Checking, the Turing Award for 2007. He is also the recipient of the CNRS Silver Medal in 2001.

Speakers:

Edmund M. Clarke - *Carnegie Mellon Univ., Pittsburgh , PA*

E. Allen Emerson - *Univ. of Texas, Austin, TX*

Joseph Sifakis - *CNRS - Verimag Labratory, Gieres, France*

EDA CONSORTIUM EXECUTIVE RECEPTION

Anaheim Hilton Hotel / Pacific Ballroom

Sunday, June 8 / 4:30 - 7:30pm

Co-sponsored by EDN Magazine and TSMC

Join the leaders of the EDA industry for a lively evening of networking and a panel discussion by distinguished members of the technology community. This EDA Consortium event, co-sponsored by EDN Magazine, TSMC, and representatives of the TSMC design ecosystem, will be an industry-wide welcome to DAC and an opportunity to re-connect with a diverse group of colleagues. Kick off DAC with EDAC!

IEEE COUNCIL ON EDA'S DISTINGUISHED SPEAKER LECTURE AND LUNCH

RM: 303AB

Tuesday, June 10 / 12:00 - 2:00pm

The IEEE Council on Electronic Design Automation (CEDA) is holding a lunch to honor Prof. Robert Brayton, the winner of the 2007 Phil Kaufman Award, for his demonstrable impact on the field of electronic design through contributions in Electronic Design Automation (EDA). Prof. Brayton will deliver an inspirational talk, highlighting his career path and challenges and shedding light on turning points while in industry and in academia. In addition to this lecture, EDA award recipients (e.g., IEEE Fellow, IEEE Technical Field Awards, etc.) will be recognized for their accomplishments during the luncheon. The first 125 attendees will receive free lunch. Standing room for all others.

11TH ANNUAL SIGDA PH. D. FORUM/MEMBER MEETING

RM:204FOYER

Tuesday, June 10 / 6:00 - 7:30pm

SIGDA invites you to attend our 11th annual PhD Forum and Member Meeting in DAC 2008. SIGDA members are invited, as are all members of the EDA Community. We will begin with an overview of SIGDA programs including newly created programs, followed by the presentation of this year's ACM/SIGDA Awards. However, the main focus of the meeting will be the Ph.D. Forum. Aimed at strengthening ties between academia and industry, students will present posters and discuss their Ph.D. dissertation research with interested attendees. The Ph.D. Forum gives students feedback on their research, and gives the EDA community a preview of work in progress. Light refreshments will be served at 6:45pm.

For more information, see http://www.sigda.org/daforum.

INTEROPERABLE PDK LIBRARIES "THE PROOF IS IN THE PUDDING!"

RM: BALLROOM D

Monday, June 9 / 12:00 - 1:30pm

At this lunch workshop, IPL members will present a user-validated, interoperable PDK. Attendees will hear about the challenges, features, and roadmap, as well as first-hand user experience with the interoperable PDK mechanism.

ACM/SIGDA SYMPOSIA/WORKSHOP LEADERS LUNCHEON

RM:201B

Monday, June 9 / 12:00 - 2:00pm

Organizers of symposia and workshops sponsored by ACM/SIGDA, as well as ACM/SIGDA volunteers and Technical Committee members are invited to a lunch get-together. ACM staff and SIGDA Board Members will be available for detailing and explaining the steps of starting or organizing an event. A brief overview of other new ACM/SIGDA activities will be presented followed by updates from SIGDA's Technical Committees.

SI2 MEMBERS MEETING

RM: 304B

Monday, June 9 / 6:00 - 8:00pm

The Annual Silicon Integration Initiative Members Meeting is open to both member and non-member companies and individuals who are interested in Si2 activities in such areas as OpenAccess, advanced library modeling systems, DFM and low-power. A Happy Hour will be held at the beginning and end of the meeting with refreshments and light hors d'oeuvres. To register for this event, leave a message at this link: http://www.si2.org/?page=3

SYNOPSYS/SUN UNIVERSITY RECEPTION

RM: MARRIOTT-PLATINUM 3 & 4

Monday, June 9 / 6:00 - 8:00pm

University professors and students are invited to join Synopsys and Sun Microsystems for an evening reception including drinks and hors d'oeuvres. Prize drawings will be held throughout the evening and the following keynote presentations will be featured.

The Landscape of Parallel Computing Research: The Berkeley View
Professor Kurt Keutzer, EECS - *Univ. of California, Berkeley, CA*

Simplicity and Complexity: the Challenges of Human-oriented Design in the Era of Billion Gate SoCs
Mike Keating - *Synopsys Fellow, Synopsys, Inc.*

Join us for a chance to win a Nintendo Wii!

IP-XACT 1.4 IN ACTION: OPEN PUBLIC MEETING OF THE SPIRIT CONSORTIUM

RM: BALLROOM A

Monday, June 9 / 6:00 - 9:00pm

The new IP-XACT 1.4 ESL-based specification from The SPIRIT Consortium expands the range of IP, enabling rapid, reliable deployment of IP into advanced design environments. The specification targets new applications, specifically those dealing with transactional modeling and advanced verification methodologies. Please join us for an update on the latest features included in this release that allow designers to automatically create many different expressions of a design in a consistent and correlated way. Attendees will hear the latest adoption stories, view vendor demos, and receive technical updates on practical approaches to more integrated design flows.

SEMINAR ON AUTOMATIC GENERATION OF MODELS FOR CoWARE PLATFORM ARCHITECT

RM: 202B

Tuesday, June 10 / 10:00 - 11:00am

Join CoWare and Carbon Design Systems as they demonstrate their solution for automatically generating models for use in the CoWare Platform Architect environment for SoC platform architecture design and software development. These high-speed models are generated directly from RTL and enable design teams to perform earlier, more accurate architectural exploration and develop firmware in a completely virtual environment. The Carbon Model Studio product will be demonstrated to show the model creation flow. The created model will be integrated into a SystemC TLM platform in CoWare Platform Architect to demonstrate the advanced performance profiling and hardware/software debugging features of the joint solution.

VERIFICATION LUNCHEON

RM: MARRIOTT-BALLROOM E

Tuesday, June 10 / 12:00 - 2:00pm

Synopsys invites you to join us for lunch and a highly informative session covering the latest verification trends, challenges and solutions. Listen to leading industry experts discuss best practices and present their views on the hottest verification topics. If you are a verification engineer or manager, you won't want to miss this special event.

IP-XACT USER'S GROUP MEETING

RM: 201A

Tuesday, June 10 / 2:00 - 4:00pm

The objective of the user's group is to facilitate the exchange of the experience on IP-XACT usage by system companies, SoC integrators, IP providers and EDA companies. The group has also the ambition to contribute to the adoption of the standard by industry and to enable feedback gathering from the community to the SPIRIT Consortium.

At DAC'08 a first meeting of the User's Group will take place and will be structured in the following way:

- SPIRIT Consortium status presentation and discussion on latest achievements, roadmaps and working group activities
- User perspectives from IP providers, SoC companies, system companies and research
- Panel and discussion session

Organizers:

Adam Morawiec - *ECSI , Gieres, France*
Loik Le Toumelin - *Texas Instruments, Inc., Villeneuve - Loubet, France*
Pierre Bricaud - *Synopsys, Inc., Sophia Antipolis, France*
Wido Kruijtzer - *NXP Semiconductors, Eindhoven, Netherlands*

RAIDERS OF THE LOCKED ART: OPENING THE TREASURE WITH INTEROPERABLE PDK - SYNOPSYS INTEROPERABILITY BREAKFAST

RM: MARRIOTT-MARQUIS

Wednesday, June 11 / 7:30 - 9:30am

Chi-Foon Chan, President and COO of Synopsys, invites you to join him on an adventure to unlock the treasure of custom analog design. Hold on to your fedora as you uncover the latest secrets and discover a gold mine of interoperability. The Tenzing Norgay Interoperability Achievement Award winner will be announced. Visit the IPL showcase during breakfast to reveal the latest developments in custom analog design interoperability.

VARIATION ROBUSTNESS FOR ANALOG/MIXED-SIGNAL, CUSTOM DIGITAL AND MEMORY DESIGN

ANAHEIM HILTON - EL CAPITAN AB

Wednesday, June 11 / 9:00 - 10:00am

As process technologies and supply voltages shrink, designers are faced with a pressing need to address systematic and random sources of variation in a more deliberate and thorough way. Accounting for variation within the flow of design has not progressed commensurate with the process technologies. We still rely on best-, worst- case corners, mismatch plots and maybe a Monte Carlo verification if there is enough time. It is time for a new approach. A brief review of the physical phenomena and industry standard device models for variation sources, including random local and global variations and systematic proximity effects, will be presented.

Presented by:
Patrick G. Drennan - *Chief Technology Officer, Solido Design Automation*

6TH ANNUAL ESL SYMPOSIUM - FINDING THE COMMON GROUND ON SUCCESSFUL ESL METHODOLOGIES: VIEWS FROM INDUSTRY EXPERTS

RM: BALLROOM E

Wednesday, June 11 / 12:00 - 2:00pm

The future of electronic system-level (ESL) implementation has been an ongoing and endless debate. However, mainstream companies have already applied a variety of ESL solutions into their core design processes. This panel, comprised of experts from a cross-section of the electronics industry, will explore the commonalities (as well as differences) from their own experiences. This session will prove to be eye-opening and of great value to anyone considering an ESL methodology.

ACM TODAES EDITORIAL BOARD LUNCHEON

RM: 204B

Wednesday, June 11 / 12:30 - 2:00pm

Annual Editorial Board Luncheon for Associate Editors and Guest Editors of ACM TODAES journal.

BIRDS-OF-A-FEATHER (BOF)

RM: 201B & 201C

Wednesday, June 11 / 6:00 - 7:30pm

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather". All BOF meetings are held at the Anaheim Convention Center, Wednesday, June 11 / 6:00 - 7:30pm. DAC will facilitate common interest group meetings to discuss DA related topics. To arrange a BOF meeting, sign up at the Information Desk located in the main lobby. A meeting room will only be assigned if ten or more people sign up. An LCD projector and screen will be provided. Check DACnet and the Birds-of-a-Feather board at the Information Desk.

CANDE MEETING

RM: 204A

Wednesday, June 11 / 6:00 - 7:00pm

CANDE is a joint Technical Committee on Design Automation for the IEEE Circuits and Systems Society (CASS) and the Council on Electronic Design Automation (CEDA). It is the sponsoring committee from CASS and CEDA for both ICCAD and DAC. CANDE brings design automation professionals together to build relationships, and to sponsor a workshop and initiatives that improve the CAD/EDA industry. Please visit the CANDE website: (http://www.cande.net/) for more information.

EDS FAIR BREAKFAST BRIEFING

RM: 204C

Thursday, June 12 / 8:00 - 8:45am

Want to seize your business success in Japan?

Electronic Design and Solution Fair 2009 is the perfect place to show your state-of-the-art technologies to decision-makers from top electronics companies. As for the emerging company, there will be a special section at low cost, ensuring of valuable exhibit experience. Join the "EDS Fair Breakfast Briefing" for details!

Please register at https://reg.mpassociates.com/reglive/register.aspx?confid=87

NEW MEDIA: WHAT DOES IT MEAN AND HOW HAVE WE STARTED TO USE IT TO REACH OUR DECISION MAKERS?

RM: 207D

Thursday, June 12 / 8:00 - 9:00am

Last year's Marketing Forum panel addressed the changes happening in the media covering EDA. This year with the changes that have occurred in the media landscape and research indicating that > 90% of new product information is first gathered through Internet searches, we find companies are experimenting with alternative ways to reach their audiences.

Join this panel of experts from the marketing, engineering, publishing, and new media distribution arenas for a discussion on how to work in the new and still-changing new media landscape. Panelists will describe how they are using both so-called "new media" (web, web 2.0, blogs, RSS, online videos, etc.) as well as traditional print media to get their messages out, and how they expect to evolve their message delivery in the coming months and years. The questions we will address include:

- How useful are these new media for a high-technology, high-price, long-sales-cycle product?
- How has the high tech industry, especially semiconductor and EDA , embraced this new media and what results are they seeing?
- What should a "new media press release" look like? Is this new format effective? Is there still a place for the traditional press release?
- Is there a cost savings with "new media" than traditional approaches?
- Is "new media" useful for a startup with limited bandwidth and $$ in terms of cost of production, interactivity, RSS feed responses, blog monitoring, etc.?

46th DAC Call for Papers

MOSCONE CONVENTION CENTER, SAN FRANCISCO, CA • JULY 26 - 31, 2009

DAC is the premier conference devoted to Design Automation (DA) and the application of DA tools in designing electronic systems. Five types of submissions are invited: regular papers, "Wild and Crazy Ideas" (WACI) topic papers, special sessions, panels, and tutorials. Submissions must be made electronically at www.dac.com. Panel and tutorial suggestions, and special session submissions are due no later than 5:00pm MST, November 3, 2008; regular papers and WACI papers are due no later than 5:00pm MST, December 19, 2008.

TOPICS OF INTEREST

DAC 2009 is seeking papers that deal with tools, algorithms and design techniques for all aspects of electronic circuit design. Apart from these core Electronic Design Automation topics, we are specifically soliciting papers in several focus areas. These include multi-core applications in design automation, embedded system and wireless design, high level design, IP design, new technologies, technology CAD, fab automation, as well as packaging and beyond-the-die design. In addition, our "Wild and Crazy Ideas" sessions cover interesting activities on a wide variety of topics that do not fit in the conventional mold. The WACI track features novel (and even unproven) technical ideas that create a buzz and get people talking. The aim of WACI is to promote revolutionary and way-out ideas that inspire discussion among conference attendees. Students worldwide are invited to submit their work for the design contest.

All Submissions must be made electronically at the DAC website, **www.dac.com**.

REGULAR PAPER SUBMISSIONS ARE DUE BEFORE 5:00PM MST, DECEMBER 19, 2008

Regular paper submissions MUST (1) be in PDF format only, (2) contain an abstract of approximately 60 words clearly stating the significant contribution, impact, and results of the submission, (3) be no more than six pages (including the abstract, figures, tables, and references), double columned, 9pt or 10pt font, and (4) MUST NOT include name(s) or affiliation(s) of the author(s) anywhere on the manuscript or abstract, and with any references to the author(s)'s own previous work or affiliations in the bibliographic citations being in the third person. Format templates are available on the DAC website for your convenience. WACI submissions may be no longer than two pages. Submissions not adhering to these rules, or those previously published or simultaneously under review by another conference, will be rejected. DAC will work cooperatively with other conferences and symposia in the field to check for double submissions. Additional submission guidelines will be available on the DAC website after September 3, 2008. All regular papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage, except for submissions to WACI. Authors of accepted papers must sign a copyright release form for their paper. Acceptance notices will be available by logging in on the DAC website after March 26, 2009. Complete author kits will be sent via email by April 6, 2009.

WACI PAPER SUBMISSIONS ARE DUE BEFORE 5:00pm MST, DECEMBER 19, 2008

Submissions to the Wild and Crazy Ideas track should not exceed 2 pages. Otherwise, they must follow the above rules and deadlines for the regular papers. A regular DAC paper explores a specific technology problem and proposes a complete solution to it, with a full table of results. In contrast, a WACI paper would present less developed, but highly innovative ideas related to areas relevant to DAC.

SPECIAL SESSION SUBMISSIONS ARE DUE BEFORE 5:00pm MST, NOVEMBER 3, 2008

Special session submissions must include descriptions of suggested papers and speakers, and the importance of the special session to the DAC audience. As the term implies, a special session covers an entire session on a special topic. This requires at least three inspiring speakers who address the topic from different angles. The topic must represent an emerging area that does not yet receive sufficient focus from regular papers. DAC reserves the right to restructure all special sessions.

PANEL AND TUTORIAL SUBMISSIONS ARE DUE BEFORE 5:00pm MST, NOVEMBER 3, 2008

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure all panel and tutorial proposals.

STUDENT DESIGN CONTEST SUBMISSIONS ARE DUE BEFORE 5:00pm MST, DECEMBER 8, 2008

Students are invited to submit descriptions of original electronic designs, either circuit level or system-level. Accepted contributions will be published in the proceedings and presented at DAC 2009. Therefore this is an excellent opportunity to showcase your design work to the world. Student Design Contest paper submissions must (1) be in PDF format only, (2) contain the title of the project, (3) contain an abstract of approximately 60 words, (4) provide a complete description of the project, and (5) be no more than six pages (including the abstract, maximum of 10 figures/tables and references), double columned, 9pt or 10pt font. The submission should clarify the originality, distinguishing features, and measured performance of the design. Three categories of designs - operational, system and conceptual - are eligible for awards. For operational designs, proof-of-implementation is required, while for conceptual designs, complete simulation and test plan is necessary. Designs must have taken place as part of the students' work at the university and must have been completed after June 2007. Submitted designs should not have received awards in other contests. Detailed rules and guidelines for all submissions are available on the DAC website.

SUBMITTERS ARE REQUIRED TO SPECIFY A CATEGORY FROM THE FOLLOWING LIST

1. System-level Design and Co-design

1.1 System specification, modeling, simulation, and performance analysis
1.2 Scheduling, HW-SW partitioning, HW-SW interface synthesis
1.3 IP and platform-based design, IP protection
1.4 System-on-Chip (SoC) and Multiprocessor SoC (MPSoC)
1.5 Application-specific processor design tools

2. System-level Communication and Networks on Chip

2.1 Modeling and performance analysis
2.2 Communications-based design, communication and network synthesis
2.3 Architectural synthesis, mapping, routing, scheduling
2.4 Optimization for energy, fault-tolerance, reliability
2.5 Interfacing and software issues, Beyond-the-die communication
2.6 NoC Design methodologies, case studies and prototyping

3. Embedded Hardware Design and Applications

3.1 Case studies of embedded system design
3.2 Flows and methods for specific applications and design domains

4. Embedded Software Tools and Design

4.1 Retargetable compilation

4.2 Memory/cache optimization

4.3 Real-time single - and multi-processor scheduling, linking, loading

4.4 Real-time operating systems

5. Power Analysis and Low-power Design

5.1 System-level power design and thermal management

5.2 Embedded low-power approaches: partitioning, scheduling, and resource management

5.3 High-level power estimation and optimization

5.4 Gate-level power analysis and optimization

5.5 Device and circuit techniques for low-power design

5.6 Power-aware and energy-efficient wireless protocols, algorithms and associated design techniques and methodologies

6. Verification

6.1 Functional, transaction-level, RTL, and gate-level modeling and verification of hardware design

6.2 Dynamic simulation, equivalence checking, formal (and semi-formal) verification model and property checking

6.3 Emulation and hardware simulators or accelerator engines

6.4 Modeling languages and related formalisms, verification plan development and implementation

6.5 Assertion-based verification, coverage analysis, constrained-random testbench generation

7. High-level Synthesis, Logic Synthesis and Circuit Optimization

7.1 Combinational, sequential, and asynchronous logic synthesis

7.2 Library mapping, cell-based design and optimization

7.3 Transistor and gate sizing and resynthesis

7.4 Interactions between logic design and layout or physical synthesis

7.5 High-level, behavioral, algorithmic, and architectural synthesis, "C" to gates tools and methods

7.6 Resource scheduling, allocation, and synthesis

8. Circuit, Interconnect and Manufacturing Simulation and Analysis

8.1 Electrical-level circuit simulation

8.2 Model-order reduction methods for linear systems

8.3 Interconnect and substrate modeling and extraction

8.4 High-frequency and electromagnetic simulation of circuits

8.5 Thermal and electrothermal simulation

8.6 Technology CAD and fab automation

9. Timing Analysis

9.1 Process technology characterization, and modeling

9.2 Deterministic static timing analysis and verification

9.3 Statistical performance analysis and optimization

10. Physical Design and Manufacturability

10.1 Physical floorplanning, partitioning, placement

10.2 Buffer insertion, routing, interconnect planning

10.3 Physical verification and design rule checking

10.4 Automated synthesis of clock networks

10.5 Reticle enhancement, lithography-related design optimizations

10.6 Design for manufacturability, yield, defect tolerance, cost issues, and impacts of DFM

10.7 3-D circuit design and algorithms

10.8 System-in-Package design, Chip-package-board codesign

10.9 Design for resilience under manufacturing variations

11. Signal Integrity and Design Reliability

11.1 Signal integrity, capacitive and inductive crosstalk

11.2 Reliability modeling and analysis

11.3 Novel clocking and power delivery schemes

11.4 Power grid robustness analysis and optimization

11.5 Soft errors and single-event upsets (SEUs)

11.6 Thermal reliability

12. Analog/Mixed-signal and RF

12.1 Analog, mixed-signal, and RF design methodologies

12.2 Automated synthesis and macromodeling

12.3 Analog, mixed-signal and RF simulation and optimization

12.4 High-frequency design and advanced antenna design for wireless

13. FPGA Design Tools and Applications

13.1 Rapid prototyping

13.2 Logic synthesis and physical design techniques for FPGAs

13.3 Configurable and reconfigurable computing

14. Testing

14.1 Test quality/reliability, current-based test, delay test, low power test

14.2 Digital fault modeling, automatic test generation, fault simulation

14.3 Digital design-for-test, test data compression, built-in self test

14.4 Memory test and repair, FPGA testing

14.5 Fault tolerance and on-line testing

14.6 Analog/mixed-signal/RF testing, System-in-Package (SiP) testing

14.7 Board - and system-level test, System-on-Chip (SoC) testing

14.8 Silicon debug, diagnosis, post-silicon design validation

15. New and Emerging Design Technologies, including but not restricted to

15.1 MEMS, sensors, actuators, imaging devices

15.2 Nanotechnologies, nanowires, nanotubes

15.3 Quantum computing

15.4 Biologically based or biologically inspired systems

15.5 Stacked devices for 3-D design, new transistor structures and devices, new or radical process technologies

15.6 Optical devices and communication

16. Cutting-edge Circuit Design and IP

16.1 Standard cell libraries and IP building blocks

16.2 I/O circuitry for high-speed communication

16.3 Design methodologies using IP blocks

16.4 Design flows for advanced SoC integration

17. Wild and Crazy Ideas

We invite papers with genuinely forward-looking, radical and innovative ideas in the area of electronic design or electronic design automation. Concepts that stimulate discussion are welcome candidates. Research that incrementally improves on prior work is not suited for this category.

DAC Technical Program Committee

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STARC
Shin-Yokohama, Japan

Tutorial Committee • SDC Judges

Tutorial Committee

Tutorial Chair
Narendra Shenoy
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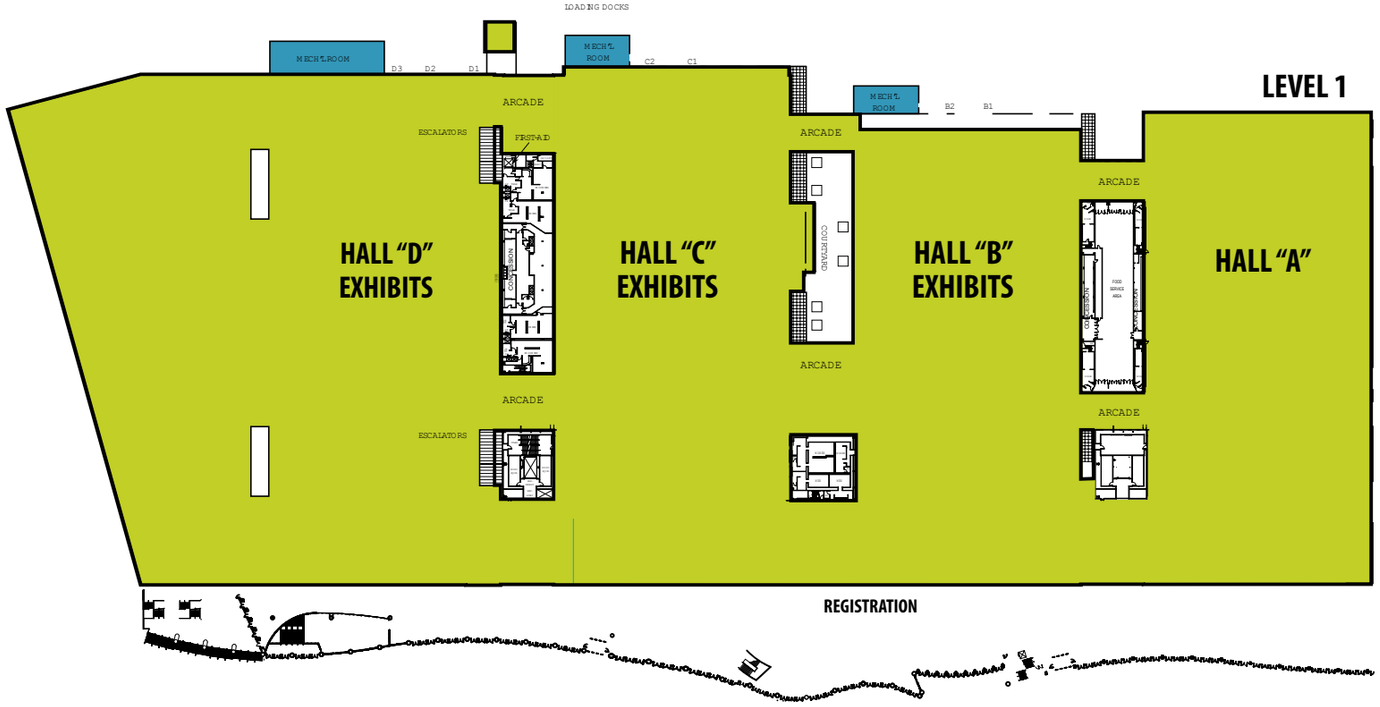

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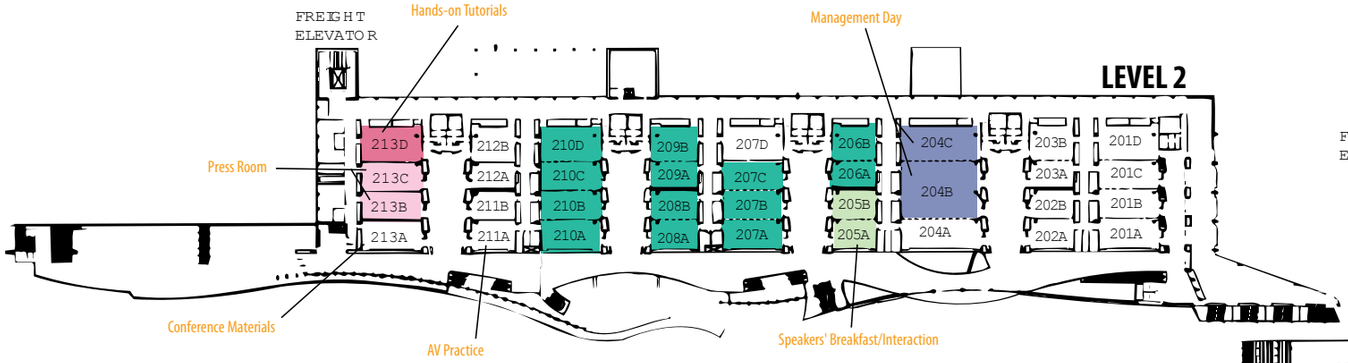

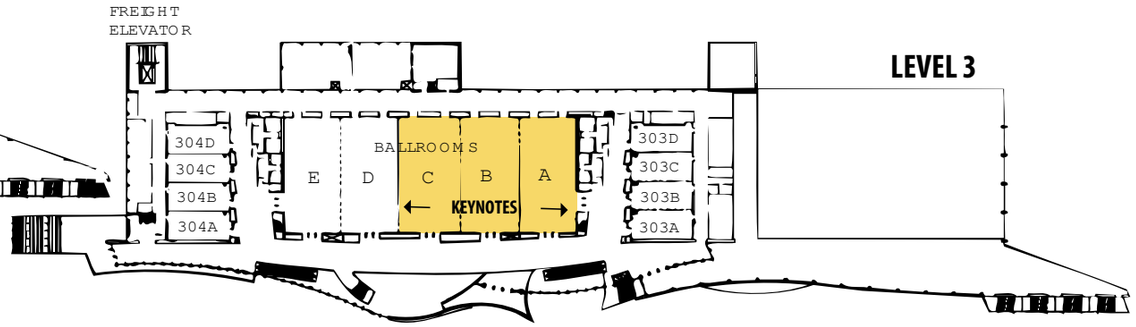

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