46 YEARS

DESIGN **AUTOMATION** CONFERENCE

Moscone Center

July 26 - 31, 2009

San Francisco

- *Keynotes*
- *Technical Sessions*
- *Special Sessions*
- *WACI*
- *Technical Panels*
- *Pavilion Panels*
- *Tutorials*
- *Student Design Contest*
- NEW! *User Track*
- *Workshops*
- *Colocated Events*
- *Exhibitor Forum*
- NEW! *IC Design Central Partner Pavilion*
- *Management Day*
- *Exhibitor Listing*

Final Program

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www.dac.com

DAC: Where The Electronic Design Community Meets…

Welcome to San Francisco and the 46th Design Automation Conference!

For thousands of us across the electronic design and design automation fields, DAC is a week of intense networking and learning. DAC is the one event each year where the entire life cycle of IC design technology is on display: new challenges in panels and special sessions; new technologies in research papers; new solutions in the exhibit suites of EDA startups; new insights into tools and methodologies at the Exhibitor Forum and the new User Track; new integrated reference flows from leading foundries and IP providers; continuing education in the form of full-day tutorials; . . . The opportunities for professional growth and new connections are truly endless. This is why business leaders, market leaders, technical leaders and thought leaders all converge at DAC.

The technical conference introduces DAC's new User Track – a three-day track of over 80 papers and posters that are written by, selected by, and targeted at users of design tools. In the User Track, attendees learn from their colleagues in leading-edge design organizations about the latest solutions to critical design and methodology challenges.

DAC's exhibition showcases approximately 200 companies, including all of the largest EDA vendors. The Exhibitor Forum theater returns with a full three-day schedule of focused technical presentations from exhibitors. The Best of DAC Contest also returns with additional Attendees' Choice categories: now you can vote on the web for your favorite vendors and new products. New this year in the exhibition is IC Design Central (ICDC) – a cluster of exhibitors and a presentation theater that brings together the entire ecosystem for SOC enablement. IP providers, design service providers, and foundry service providers can all be found in the ICDC.

DAC is also the meeting place for many EDA- and design-related organizations, workshops and events. Who meets at DAC? Standards bodies, such as Accellera and Si2. Roadmapping efforts, such as the ITRS Design Technology working group. Established symposia, such as SASP, NANOARCH, MSE, SLIP, DFM&Y, and HOST. Workshops on topics ranging from UML to low-power design to bio-design automation. A total of 18 workshops and colocated events will take place at DAC.

DAC 2009 is proud to present a stellar lineup of keynote and plenary sessions. In response to the recent upheavals in the macroeconomy as well as in the IC design and design automation industries, DAC opens its program with a special Monday afternoon panel that brings together the CEOs of the leading EDA companies. Attendees will hear our industry leaders' views on market, business, and technology futures, as well as the overall outlook for the EDA industry. DAC is also proud to present keynote presentations from outstanding industry leaders: Fu-Chieh Hsu, Vice President, Design and Technology Platform, TSMC; and William Dally, Chief Scientist, NVIDIA and Willard R. and Inez Kerr Bell Professor of Computer Science at Stanford University. Finally, a plenary panel on Thursday, moderated by Walden C. Rhines of Mentor Graphics Corp. will address the questions of "How Green is My Silicon Valley" and what 'green' means for our industry.

On behalf of DAC's sponsoring organizations and the many hundreds of volunteers who make DAC happen each year, I warmly welcome you to DAC 2009!

Best regards,

Andrew B. Kahng

General Chair, 46th Design Automation Conference

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Welcome to San Francisco

Guest/Family Program

An $80 registration fee will admit each guest or family member to the following: (Children under the age of 12 qualify for a $30 guest badge.)

1. Wednesday Night Party at the San Francisco Marriott.
2. Admission to the exhibit hall (when accompanied by an attendee).
3. Children under the age of 14 are not allowed in the exhibit hall area.

Registration for the Guest/Family Program will be at the Conference Registration desk on Sunday, July 26 through Wednesday, July 29.

A badge will be provided for each registered guest or family member. This badge must be worn to participate in the above activities.

On-site Information Desk

The Information Desk will be located on the North Concourse level of the Moscone Center, Phone: 415-978-3700.

First Aid

The First Aid rooms are located in North and South Halls of the Moscone Center.

For assistance, please call:

North First Aid: 415-974-4094

South First Aid: 415-974-4090

A nurse will be on duty at all times while meetings and exhibits are open.

Weather

San Francisco summers have scant in common with summers elsewhere. Marked by billowing white fog, the majestic product of sea spray, wind and Central Valley heat, San Francisco summers are characteristically overcast and cool, while the marine layer usually burns off by the afternoon. While June, July and August typify summer in most of the Northern hemisphere, San Francisco (as in many areas) does not conform to expectations.

Layers, layers, layers. Even in the warmest months, San Francisco visitors should always bring a light jacket. Unexpected upswells from the deep and frosty Pacific Ocean and chilling blasts sweep over San Francisco without notice and can change San Francisco's weather in an instant.

San Francisco Attractions

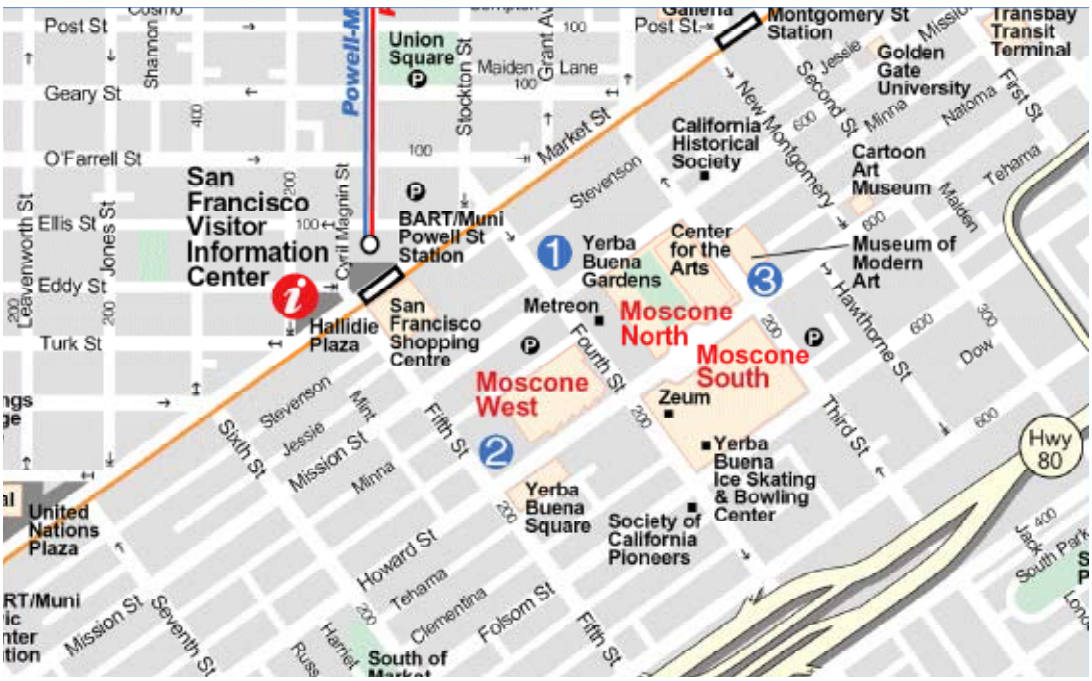
San Francisco's 43 hills, surrounding waters, narrow alleys, and busy streets invite you to explore. Take in the view from Coit Tower. Hop on a cable car and cruise through Russian Hill. Hike through Golden Gate Park, or check out the vibrant, ethnic enclaves such as the Mission and Chinatown. The city's distinct landscapes are dotted with iconic sites and have an unparalleled mix of breath-taking natural and human-made beauty. For more information on San Francisco, visit www.onlyinsanfrancisco.com or call the San Francisco Convention and Visitors Bureau at 415-391-2000.

Hotel Locations

1 - San Francisco Marriott Hotel

2 - Intercontinental Hotel

3 - W Hotel



Important Information At-A-Glance

Exhibit Hours

Monday, July 27	9:00am - 6:00pm
Tuesday, July 28	9:00am - 6:00pm
Wednesday, July 29	9:00am - 6:00pm
Thursday, July 30	9:00am - 1:00pm

Conference Registration Hours

Sunday, July 26	7:30am - 6:00pm
Monday, July 27	7:00am - 6:00pm
Tuesday, July 28	7:00am - 6:00pm
Wednesday, July 29	7:00am - 6:00pm
Thursday, July 30	7:00am - 6:00pm
Friday, July 31	7:30am - 6:00pm

Tutorial Registration

Monday Tutorial Registration

Monday, July 27, 7:00am - 6:00pm

You may register for tutorials at Conference Registration located in the North Lobby.

Friday Tutorial Registration

Friday, July 31, 7:30am - 6:00pm

Sunday through Thursday, you may add a Friday tutorial at Conference Registration located in the North Lobby. Beginning Friday morning, at 7:30am, Tutorial Registration will be located on the Concourse Level near rooms 131-133.

Stay Connected at DAC

Wireless Internet

DAC is offering complimentary wireless internet throughout the Moscone Center. Look for SSID: DAC2009. Co-Sponsored by:

Apache DESIGN SOLUTIONS

Mobile Devices

DAC has a special website built for access from handheld mobile devices. From your Windows Mobile or Blackberry device, log in to www.dac.com and you will be automatically redirected to the mobile site. Presentation schedules, the exhibitor listing and other useful information are available and optimized for viewing on small screens.

Daily Updates on DAC.com

Check the DAC website daily for a complete listing of each day's schedule, the latest exhibitor announcements, and press coverage.

Food Courts

Food courts are available in the North and South Hall exhibit floors. Each food court includes tables with power connections for laptop plug-in.

DACnet - 2009

DACnet internet stations are available on the Concourse Level by the Gateway Ballroom. Power for laptop plug-in is also available.

Wednesday Night Party

There will be a wide array of delictable foods along with plentiful amounts of wine, beer and assorted beverages. To join these festivities, you must register as a student or full conference attendee. You may also register for the Guest/Family Program.

Monday CEO Panel: Futures for EDA: The CEO View

Rm: Gateway Ballroom

Monday, July 27, 4:30 - 5:45pm

Aart de Geus
CEO and Chairman of the Board
Synopsys, Inc.

Walden C. Rhines
CEO and Chairman of the Board
Mentor Graphics Corp.

Lip-Bu Tan
President and CEO
Cadence Design Systems, Inc.

The IC design and EDA ecosystem has witnessed a number of structural and financial upheavals in recent years. Perennial challenges—new technologies and markets, R&D investment levels, business and revenue models, and interoperability—are magnified by the current economic downturn.

This year, DAC will open its program with a special Monday afternoon panel that brings together the CEOs of the leading EDA companies. The panelists will give their views on market, business and technology futures, as well as the overall outlook for the EDA industry.

Chair: **Juan-Antonio Carballo** - *IBM Corp., San Francisco, CA*

Keynote: Overcoming the New Design Complexity Barrier: Alignment of Technology and Business Models

Rm: Gateway Ballroom

Tuesday, July 28, 8:30 - 10:15am

Fu-Chieh Hsu
Vice President, Design and Technology Platform, Taiwan Semiconductor Manufacturing Company Ltd., Hsinchu, Taiwan

The semiconductor industry today faces a new design complexity barrier. Convergence of product features brings unprecedented complexities on process technology, architectural and gate-count. Integration and cost drivers bring 3-D stacking with through-silicon vias. Heterogeneity brings high-voltage devices, image sensors, and MEMS into a single product design optimization. From IP migration, to variability modeling and mitigation, to NRE cost, the new paradigm is that these are no longer discrete issues addressable by point-tool solutions. Overcoming this new design complexity barrier requires breakthrough technologies and integrated EDA solutions.

Funding the development of new EDA solutions must make business sense. But while traditional ROI assessments are based on "one company-centric" business models, the next stage of the industry's evolution requires ROI and business models that acknowledge coexistence, and even collaboration, of multiple companies. This is especially true during this unprecedented worldwide financial earthquake. A win-win-win future will depend on the emergence of an innovative business model that is realized collaboratively by key players across the IC design and manufacturing ecosystem. Fortunately, recent initiatives have the promise to meet this need.

Dr. Fu-Chieh Hsu has served as Vice President of Design and Technology Platform for Taiwan Semiconductor Manufacturing Company, Ltd. since April 2006. He is responsible for all design service operations at TSMC and works with the Marketing and R&D departments to provide customers with technology platform solutions.

Dr. Hsu founded Monolithic System Technology, Inc. (MoSys) in 1991 and served as its Chairman and Chief Executive Officer until retiring at the end of 2004. He was Chairman and President of Myson Technology Inc. (now Myson Century Inc.) from 1990 to 1991. Prior to that, Dr. Hsu worked at Integrated Device Technology, Inc. as Chief Technology Officer and Vice President as well as other senior positions. Dr. Hsu also served at Hewlett-Packard Labs.

Dr. Hsu has published or contributed to more than 40 papers and also holds 55 U.S. patents. Dr. Hsu received his Bachelor of Science degree in electrical engineering from National Taiwan Univ. in 1978, and Master of Science and Ph.D. degrees in electrical engineering and computer sciences from Univ. of California, Berkeley, in 1981 and 1983, respectively.

Keynote: The End of Denial Architecture and the Rise of Throughput Computing

Rm: Gateway Ballroom

Wednesday, July 29, 11:15am - 12:15pm

William J. Dally
Chief Scientist and Senior Vice President of Research, NVIDIA Corp., Santa Clara, CA,
Willard R. and Inez Kerr Bell Professor of Engineering, Stanford Univ., Stanford, CA

Throughput-optimized processors, such as graphics processing units (GPUs) have scaled at historic rates in recent years, and continue to do so along a design trajectory that is largely unhindered by conventional dogmas and legacies. These processors recognize that two critical aspects of machine organization are key to performance: parallel execution and hierarchical memory organization. Conventional processors, which present an illusion of sequential execution and uniform, flat memory, find their performance increasing only slowly over time, and their evolution is at an end. In contrast, throughput processors embrace, rather than deny, parallelism and memory hierarchy to realize large performance and efficiency advantages. Throughput processors have hundreds of cores today and will have thousands of cores by 2015. They will deliver most of the performance, and most of the user value, in future computer systems.

This talk will discuss some of the challenges and opportunities in the architecture and programming of future throughput processors, as it relates to the EDA world. First, CAD tools, flows, and methodologies are clearly crucial to the design of these processors, and these must adapt to support such designs. Second, in this changing landscape, CAD tools must need to evolve to run on throughput processors. In throughput processors, performance derives from the parallelism available from the plentiful arithmetic units, and efficiency derives from locality, overcoming restrictions stemming from communication bandwidth bottlenecks that dominate cost, performance, and power. This talk will discuss exploitation of parallelism and locality with examples drawn from the Imagine and Merrimac projects, from NVIDIA GPUs, and from three generations of stream programming systems.

William J. Dally is Chief Scientist and Senior Vice President of Research at NVIDIA Corp. and the Willard R. and Inez Kerr Bell Professor of Engineering at Stanford University. Dally and his group have developed system architecture, network architecture, signaling, routing, and synchronization technology that can be found in most large parallel computers today. While at Bell Labs Bill contributed to the BELLMAC32 microprocessor and designed the MARS hardware accelerator. At Caltech he designed the MOSSIM Simulation Engine and the Torus Routing Chip which pioneered wormhole routing and virtual-channel flow control. While a Professor of Electrical Engineering and Computer Science at the Massachusetts Institute of Technology his group built the J-Machine and the M-Machine, experimental parallel computer systems that pioneered the separation of mechanisms from programming models and demonstrated very low overhead synchronization and communication mechanisms. At Stanford Univ.his group has developed the Imagine processor, which introduced the concepts of stream processing and partitioned register organizations. Bill has worked with Cray Research and Intel Corp. to incorporate many of these innovations in commercial parallel computers, with Avici Systems to incorporate this technology into Internet routers, co-founded Velio Communications to commercialize high-speed signaling technology, and co-founded Stream Processors, Inc. to commercialize stream processor technology. He is a Member of the National Academy of Engineering, a Fellow of the IEEE, a Fellow of the ACM, and a Fellow of the American Academy of Arts and Sciences. He has received numerous honors including the IEEE Seymour Cray Award and the ACM Maurice Wilkes award. He currently leads projects on computer architecture, network architecture, and programming systems. He has published over 200 papers in these areas, holds over 50 issued patents, and is an author of the textbooks, Digital Systems Engineering and Principles and Practices of Interconnection Networks.

Special Plenary Panel: How Green Is My Silicon Valley

Rm: Gateway Ballroom

Thursday, July 30, 12:00 - 1:45pm

Walden C. Rhines
EDA Consortium, Chair, Mentor Graphics Corp., Wilsonville, OR

There has been a lot of talk about 'green' technology, and how it can save our economy and the electronics industry. But what is really being done about it in Silicon Valley—the spawning ground for all things high-tech?

This panel of experts—drawn from technology heavyweights, governmental agencies, venture capitalists and start-ups—will give their views on what 'green' means for our industry. For some, it means low-power chip and system design. Others focus on completely new solutions that go well beyond traditional electronics to help lower our collective carbon footprint. Green also means leverage of existing technologies in new eco-friendly applications ranging from water management to smokestack emission monitoring.

Innovation is the only answer to this, the preeminent challenge of the 21st century. And innovation is what Silicon Valley and the global high-tech industry are all about. Come hear the best and brightest talk about their favorite new color and how it will take our industry and the larger economy into a brighter, more sustainable future.

Ian Wright
CEO, Wrightspeed, San Francisco, CA

Thomas Jacoby
Director, California Clean Energy Fund
Chairman of the Board, Innovations Fuel, Inc.
CEO, Tymphany Corp., Cupertion, CA

John A. "Skip" Laitner
Director of Economic Analysis
American Council for an Energy Efficient Economy (ACEEE), Washington DC

Technical Program Highlights

Six hundred and eighty-two (682) regular papers were submitted (a seven percent jump from last year's 639 papers) and 22% were accepted. Areas with highest submission numbers are:

- System-level design and codesign (87 papers were submitted; accepted papers will be presented in five sessions)
- Power analysis and low-power design (83 papers were submitted; four sessions)
- Physical design and manufacturability (82 papers were submitted; four sessions)
- High-level and logic synthesis (54 papers were submitted; three sessions)

In addition to regular paper sessions, DAC's technical program consists of Special Sessions, Panels, Tutorials, Workshops, and Colocated Events. The introduction of the User Track, with its emphasis on design methodology and tool flows, is new this year. The User Track had 117 submissions, and the accepted papers will be presented in nine sessions (five for the front end, four for the back end) as well as in a new poster session on Wednesday afternoon.

Special Sessions will deal with a wide variety of themes such as preparing for design at 22nm, designing circuits in the face of uncertainty, verification of large, systems-on-chip, bug-tracking in complex designs, novel computation models, multicore computing and the impact of data centers on computing and EDA. The special sessions continue to include WACI (Wild and Crazy Ideas)—forward-looking and innovative ideas that are typically less developed than regular papers.

Technical Panels present the hottest issues of our industry and will cover:

- Technical discussions on system prototyping, embedded software design, mixed signal verification, system-level power challenges, design for manufacturability, emerging applications of EDA technology, and the previously-noted special plenary panel, "How Green is My Silicon Valley".
- Management-focused topics such as costs of scaling, careers in EDA, and the return of the CEO panel.

The program also features six Full-day Tutorials on timely subjects ranging from parallel programming and its application to CAD tools, high-level synthesis, post-silicon validation, functional verification, low-power design in the wireless space, and the future of circuits based on emerging nanodevices.

Panels

See pages 36-53 for details.

System Prototypes: Virtual, Hardware or Hybrid?
Tuesday, July 28, 10:30am - 12:00pm

EDA in Flux—Should I Stay or Should I Go?
Tuesday, July 28, 2:00pm - 4:00pm

Moore's Law: Another Casualty of the Financial Meltdown?
Tuesday, July 28, 4:30pm - 6:00pm

DFM—Band-Aid or Competitive Weapon?
Wednesday, July 29, 9:00am - 11:00am

Oil Fields, Hedge Funds and Drugs
Wednesday, July 29, 2:00pm - 4:00pm

Guess, Solder, Measure, Repeat—How Do I Get My Mixed-Signal Chip Right?
Wednesday, July 29, 4:30pm - 6:00pm

From Milliwatts to Megawatts: The System-Level Power Challenge
Thursday, July 30, 2:00pm - 4:00pm

The Wild West: Conquest of Complex Hardware-Dependent Software Design
Thursday, July 30, 4:30pm - 6:00pm

Special Sessions

See pages 36-53 for details.

Mechanisms for Surviving Uncertainty: Opportunities and Prospects
Tuesday, July 28, 10:30am - 12:00pm

Dawn of the 22nm Design Era—Yes We Can!
Tuesday, July 28, 2:00pm - 4:00pm

Verifying an SOC Monster: Whose Job Is It Anyway?
Tuesday, July 28, 4:30pm - 6:00pm

Emerging Technologies: Blue-Sky Research or CMOS Replacement?
Wednesday, July 29, 9:00am - 11:00am

Computation in the Post-Turing Era
Wednesday, July 29, 2:00pm - 4:00pm

Multicore Computing and EDA
Wednesday, July 29, 4:30pm - 6:00pm

WACI: Wild and Crazy Ideas
Thursday, July 30, 9:00am - 11:00am

The Tool Shows That My Design Is Wrong, But Where Is the Bug?
Thursday, July 30, 9:00am - 11:00am

Technologies for Green Data Centers
Thursday, July 30, 4:30pm - 6:00pm

User Track Highlights

Sponsored by: cadence™

Tuesday, Wednesday, and Thursday

NEW!

The presentations in the all-new User Track focus on problems that design practitioners face every day. The presentations run in parallel with the regular paper sessions. The User Track program includes front-end sessions, back-end sessions, and a poster session.

The front-end sessions have 16 presentations that focus on a number of themes that enhance system-level design productivity. Specific topics include power management modeling and simulation techniques, verification of power management techniques and embedded device drivers, several perspectives on the use of high-level languages, loosely- and approximately-timed switchable models and methodologies for architecture-level prototyping and design space exploration. The speakers include users from Infineon Technologies AG, Cisco Systems, Inc., Texas Instruments, Inc., Xilinx, Inc., STMicroelectronics, Intel Corp., Virtutech, and ClueLogic.

The back-end sessions have 26 presentations addressing the following questions: How do I stitch last week's ECOs back into my design? How do I analyze power supply and substrate noise effectively for large chips? How do I mix transistor- and gate-level timing analyses, and add statistical timing to this? How do I bring more automation to the analog and mixed-signal domain? Can I improve productivity by designing portable libraries and advanced analog verification methodologies? Answers to these questions and many more will be presented by users from STMicroelectronics, Samsung, Qualcomm, Inc., Intel Corp., Fujitsu Labs, IBM Corp., and Sun Microsystems, Inc.

The poster session includes approximately 40 posters on topics that span both front-end and back-end design. The posters will offer an opportunity for personal interaction with EDA tool users from many leading companies. An Ice Cream Social will be held in conjunction with the poster session on Wednesday from 1:30 - 3:00pm on the Concourse Level.

User Track Sessions

See pages 16-18 for details.

1U Robust Design and Test
Tuesday, July 28, 10:30am - 12:00pm - Rm: 132

2U Practical Physical Design
Tuesday, July 28, 2:00 - 4:00pm - Rm: 132

3U Verification: A Front-End Perspective
Tuesday, July 28, 4:30 - 6:00pm - Rm: 132

4U Timing Analysis in the Real World
Wednesday, July 29, 9:00 - 11:00am - Rm: 132

5U Poster Session and Ice Cream Social
Wednesday, July 29, 1:30 - 3:00pm - Concourse Level

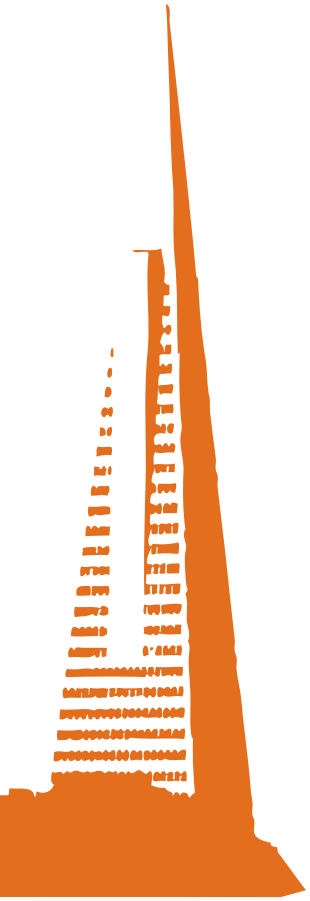
6U Towards Front-End Design Productivity
Wednesday, July 29, 3:00 - 4:00pm - Rm: 132

7U Front-End Development: Embedded Software and Design Exploration
Wednesday, July 29, 4:30 - 6:00pm - Rm: 132

8U Power Analysis and IP Reuse
Thursday, July 30, 9:00 - 11:00am - Rm: 132

9U Front-End Power Planning and Analysis
Thursday, July 30, 2:00 - 4:00pm - Rm: 132

10U Advances in Analog and Mixed-Signal Design
Thursday, July 30, 4:30 - 6:00pm - Rm: 132



Exhibition Highlights

Exhibition

The 46th DAC exhibition is located in the North and South Halls of the Moscone Center.

Visit the DAC exhibition to learn in-depth about new products and services from nearly 200 vendors, spanning all aspects of the electronic design process including EDA tools, IP cores, embedded system and system-level tools, as well as silicon foundry and design services.

Exhibition Hours

Monday, July 27 - Wednesday, July 29 9:00am - 6:00pm
Thursday, July 30 9:00am - 1:00pm

The Best of DAC Exhibits contest! Vote for your favorite vendors, new products, and Pavilion Panel from your laptop or any DACnet terminal, at www.dac.com. When you cast your ballot, you will be entered into a drawing for an iPod Touch!

Exhibitor Forum Attendees are invited to the Exhibitor Forum, in the North Hall in Booth 4359, to hear a series of technical presentations from exhibitors on focused topics. See pages 19-21 for details.

DAC Pavilion The popular DAC Pavilion is located in the South Hall in Booth 1928. This year, the Pavilion will feature 19 presentations on business and technical issues. See pages 22-23 for details.

NEW! **IC Design Central Partner Pavilion,** DAC's new and innovative feature for exhibit floor education, is located in Booth 4500. Attend presentations on how specific exhibitors are solving your design issues with their latest tools and methodologies. See pages 14-15 for details.

Exhibit-Only Pass Register for an exhibits-only pass and receive admission to all days of the exhibition, includes the following:

1. Keynote Panel
2. Tuesday and Wednesday Keynotes
3. Special Plenary Panel
4. IC Design Central Partner Pavilion (19 presentations)
5. User Track Poster Session and Ice Cream Social (38 Poster Presentations)
6. DAC Pavilion (20 Events)
7. Exhibitor Forum (18 Presentations)

Visit these First-Time Participating Companies at DAC:

Achilles Test Systems, Inc. 912
Agnisys Inc. 4064
Altair Engineering 4208
AnSyn 422
APAC IC Layout Consultant, Inc. 4214
Ateeda Limited 4102
BEEcube, Inc. 4307
Cambridge Analog Technologies, Inc. 4301
Chipworks 4203
CST of America, Inc. 3155
Desaut Inc. 1207
DOCEA Power 3143
E-System Design 408
Enterpoint Ltd. 4207
Epoch Microelectronics, Inc. 4213
Fidus Systems Inc. 4204
Innovative Logic Inc. 1306
Logic Perspective Technology Inc. 3257
Mephisto Design Automation 521
Methodics LLC 1924
NextOp Software, Inc. 903
Optiwave Systems Inc. 916
OVM World 3450
R3 Logic Inc. 813
SKILLCAD INC. 3261
Summit Exec, Inc. 3859
Tiempo 4104
Warthman Associates 4205
XJTAG 3954

Design Automation Conference Sponsors

Association for Computing Machinery (ACM)

ACM is an educational and scientific society uniting the world's computing educators, researchers and professionals to inspire dialogue, share resources and address the field's challenges. ACM strengthens the profession's collective voice through strong leadership, promotion of the highest standards, and recognition of technical excellence. ACM supports the professional growth of its members by providing opportunities for life-long learning, career development, and professional networking. For more information, please visit http://www.acm.org.

The ACM Digital Library and Guide to Computing Literature are the definitive online resources for computing professionals. Richly interlinked, they provide access to ACM's collection of publications and bibliographic citations from the universe of published computing literature. http://www.acm.org/dl

Additionally, ACM has 34 Special Interest Groups (SIGs) that focus on different computing disciplines. More than half of all ACM members join one or more of these Special Interest Groups. The SIGs publish newsletters and sponsor important conferences such as SIGGRAPH, OOPSLA, DAC, SC and CHI, giving members opportunities to meet experts in their fields of interest and network with other knowledgeable members http://www.acm.org/sigs. Become an ACM member today and join thousands of other leading professionals, researchers and academics who benefit from all ACM has to offer. Join ACM online at http://www.acm.org, or contact ACM directly by phone: +1-800-342-6626 (US and Canada) or +1-212-626-0500 (Global), by fax: +1-212-944-1318, or by e-mail: acmhelp@acm.org. Hours of operation are from 8:30am - 4:30pm Eastern Time.

ACM/SIGDA

ACM/SIGDA (Special Interest Group on Design Automation) has a tradition of over forty years of supporting conferences and the EDA profession. In addition to sponsoring DAC, SIGDA sponsors ICCAD, DATE, and ASP-DAC, plus approximately 15 smaller symposia and workshops. SIGDA provides a broad array of additional resources to our members, to students and professors, and to the EDA profession in general. SIGDA organizes the Univ. Booth and Ph.D. Forum at DAC and the CADathlon at ICCAD, and funds various scholarships and awards. SIGDA provides its members with full access to SIGDA-sponsored conference proceedings in the ACM Digital Library and the SIGDA E-Newsletter containing information on upcoming conferences and funding opportunities, emailed to SIGDA members regularly. The SIGDA E-Newsletter also includes SIGDA News which highlights the most relevant events in the EDA and semiconductor industry, and the "What is...?" column that brings to the attention of EDA professionals the most recent topics of interest in design automation. SIGDA has recently initiated the creation of Technical Committees in various areas of EDA, ranging from Physical Design and Logic Synthesis, to system-level Design, Low Power Design, Reconfigurable Computing, Testing, Verification, and Emerging Technologies. Attend the 12th Ph.D. Forum/Member Meeting on Tuesday evening to find out how the Technical Committees provide a link between SIGDA activities and various technical areas in EDA. SIGDA also provides strong support for the ACM journal TODAES (Transactions on Design Automation of Electronic Systems). For further information on SIGDA's programs and resources, see http://www.sigda.org. In addition, SIGDA members may also want to consider joining our parent organization, ACM. ACM membership provides access to a variety of ACM products and resources, including discounts on conferences, subscriptions to ACM journals and magazines, and the ACM Digital Library, an invaluable IT resource. For further details, see ACM's home page at http://www.acm.org. As an EDA professional, isn't it time YOU joined SIGDA?

SIGDA/DAC University Booth

This year marks the 22nd University Booth at the Design Automation Conference. The booth is an opportunity for university researchers to display their results and to interact with visitors from industry. Priority is given to presentations that complement the conference technical program. Demos that highlight benchmark results are also encouraged. The Design Contest winners, DAC speakers, and PhD Forum participants are invited to give demonstrations presenting their work at the University Booth. The schedule of presentations is published at the conference and is also available on the SIGDA website at http://www.sigda.org/programs/Ubooth/Ubooth2009/. The organizers thank the Design Automation Conference for its continued support of this project.

EDA Consortium

The EDA Consortium (EDAC) is the international industry association for the providers of tools and services that enable engineers to create the world's electronics products. Its mission is to promote the health of the EDA industry by addressing common industry needs and providing valued services. By publishing the Market Statistics Service (MSS) EDAC enables worldwide tracking of EDA, Semiconductor IP and services revenue. By co-sponsoring the prestigious annual Phil Kaufman Award, the EDA Consortium and the IEEE Council on EDA bring industry-wide recognition to distinguished contributions to EDA. As a co-sponsor of DAC and DATE, the EDA Consortium represents the interests of exhibiting companies. EDAC members influence industry initiatives by participating on committees to address common needs as well as play a positive role in reducing costs for the industry and its customers.

Examples of committee accomplishments include an EDA operating systems roadmap, anti-piracy education, licensing guidelines, and the reduction of governmental export controls. EDAC offers international forums and symposiums which are well attended by industry CEOs, executives, press, and analysts. These events cover topics of interest to emerging and large EDA companies alike. EDA Consortium members receive a 10% discount on DAC booth/suite space. For more information call 408-287-3322 or visit www.edac.org. EDAC is located in San Jose, CA, USA.

46th DAC Proceedings DVD

Additional copies of the 46th DAC Proceedings DVD may be ordered prepaid from:

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IEEE

A non-profit organization, IEEE is the world's leading professional association for the advancement of technology.

IEEE/Council on Electronic Design Automation

The IEEE Council on Electronic Design Automation (CEDA) provides a focal point for EDA activities spread across six IEEE societies (Antennas and Propagation, Circuits and Systems, Computer, Electron Devices, Microwave Theory and Techniques, and Solid State Circuits). The Council sponsors or co-sponsors over a dozen key EDA conferences, including the Design Automation Conference (DAC) and the International Conference on Computer Aided Design (ICCAD), Design Automation and Test in Europe (DATE) and events at Embedded Systems Week (ESWeek). The Council also publishes IEEE Transactions on CAD, as well as the newly launched IEEE Embedded Systems Letters. Since its founding, the Council has expanded its support of emerging areas within EDA such as nanoscale systems, sponsored new initiatives including the Distinguished Speaker Series and is increasing recognition to members of the EDA profession via awards such as the A. Richard Newton and Phil Kaufmann Awards. The Council welcomes new volunteers and local chapters. For more information on CEDA, visit: www.c-eda.org.

IEEE/Circuits and Systems Society

The IEEE Circuits and Systems Society (CASS) is one of the largest societies within IEEE and in the world devoted to the analysis, design, and applications of circuits, networks, and systems. It offers its members an extensive program of publications, meetings and technical and educational activities, encouraging an active exchange of information and ideas. The Society's peer reviewed publication activities include: Trans. on CAS-Part I: Regular Papers; Trans. on CAS-Part II: Express Briefs; and Trans. on CAS for Video Technology. In addition, there are Trans. on CAD; Trans. On VLSI; Trans. on Multimedia; Trans. on Mobile Computing; and Trans. on Biomedical Circuits and Systems which are co-sponsored witth IEEE sister societies. Also available is the CASS Electronic Newsletter. CASS sponsors or co-sponsors a number of international conferences which include the Design Automation Conference (DAC), the Int'l Conference on Computer-Aided Design (ICCAD) and the Int'l Symposium on Circuits and Systems (ISCAS). A worldwide comprehensive program of advanced workshops including a new series on "Emerging Technologies in Circuits and Systems," as well as our continuing education short courses, bring to our worldwide membership the latest developments in cutting-edge technologies of interest to industry and academia alike.

The IEEE CASS has been serving its membership for over 50 years with such member benefits as:

- Discounts on Society publications, conferences and workshops (including co-sponsored publications and conferences)
- The Society Magazine which includes articles on emerging technologies, society news and current events
- Opportunities to network with peers and experts within our 17 focused committee meetings, the local events of over 60 chapters and more than 20 annual conferences/workshops
- Opportunity to read and review papers, write articles and participate in the Society's government
- The CASS Electronic Newsletter
- And all the personal and professional benefits of IEEE CASS/CANDE/CEDA membership

IEEE/Computer Aided Network Design

Computer Aided Network Design (CANDE) is a joint technical committee of the IEEE Circuits and Systems Society and the Council on Electronic Design Automation. CANDE is dedicated to bringing design automation professionals together to further their education, to assist in building relationships, and to sponsor initiatives which grow the CAD/EDA industry.

CANDE sponsors a workshop in the Fall to address emerging technologies and to provide an opportunity for the generation of new ideas. CANDE is the sponsoring technical committee from CASS for both DAC and ICCAD.

For more information, please contact:

IEEE/CASS/CANDE
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Web: www.ieee-cas.org

Management Day

Sponsored by: cadence™

Tuesday, July 28, 10:30am - 6:00pm - Rm: 131

Topic Area: Business

The DAC 2009 Management Day provides managers with timely information to help them make decisions where business and technology intersect. This is a unique opportunity for managers to gain insights from their peers in the industry.

Today's complex SOCs require different types of optimizations and the adoption of emerging solutions to meet stringent design requirements. Optimizing for volume production, low power, and shrinking sizes necessitates accurate trade-off analysis and technical/business decision-making by management. Moreover, moving to new semiconductor technology nodes, such as 28nm or 40nm, can significantly affect the choices of suppliers.

The three sessions in this year's Management Day will discuss these changing needs and present corresponding management decision criteria that allow managers to make the right choices from a pool of alternate options for flows, methodologies and suppliers. The first two sessions will feature presentations by managers representing independent device manufacturers (IDMs), fab-light ASIC providers and fabless companies.

Senior managers of today's most complex nanometer chips — from Intel Corp., Advanced Micro Devices, Inc., STMicroelectronics, Freescale Semiconductor, Inc., and other leading companies — will discuss the latest and emerging solutions, along with their economic impact. The third session will be a panel that will involve the presenters and the audience in an open brainstorming discussion.

This special day provides managers with timely information to help them make decisions where business and technology intersect. This is a unique opportunity for managers to gain insights from their peers in the industry.

Organizer: Yervant Zorian - *Virage Logic Corp.*

Session 1: Trade-Offs and Choices for Emerging SOCs

10:30am - 12:00pm

Session Chair: Nic Mokhoff - *EE Times / TechInsights*
Session Organizer: Yervant Zorian - *Virage Logic Corp.*

Today's emerging SOCs require multiple types of optimizations and the adoption of advanced solutions to meet stringent design requirements. Optimizing for volume production, low power, and shrinking sizes necessitates accurate trade-off analysis and technical/business decision-making by management. This session will feature senior managers of today's most complex nanometer chips.

Delivering the Next Generation High Performance Microprocessor – Challenges and Opportunities

Rani Borkar - *Vice President, Digital Enterprise Group, Intel Corp.*

3-D Stacking: Opportunities and Trends for Consumer SOCs

Philippe Magarshak - *Vice President, Central R&D, STMicroelectronics*

Technology Platform for Next-Generation Networking Products

Don Friedberg - *Director, Network & Storage Products Group, LSI Logic Corp.*

Session 2: Decision Making for Complex SOCs

2:00 - 4:00pm

Session Chair: Ed Sperling - *System Level Design*
Session Organizer: Yervant Zorian - *Virage Logic Corp.*

Moving to new semiconductor technology nodes for complex SOCs can significantly affect the choices of design flow, methodologies and suppliers. The session will cover the challenges of complex SOC design and present corresponding management decision criteria that allow managers to make the right choices from a pool of alternate options. This session features presentations by managers representing independent device manufacturers (IDMs), fab-light ASIC providers, and fabless companies.

A Contrast of the Design /Management Challenges Facing a 5-Month Versus a 15-Month Development Cycle SOC

Alan Nakamoto - *Vice President, Engineering and Founder, PMC-Sierra, Inc.*

Design Challenges in Intense Mobile Multimedia Processors

Pierre Garnier - *Vice President and General Manager, Worldwide Wireless Baseband, Texas Instruments, Inc.*

IP Development and Sourcing Decisions for Complex Wireless Baseband SOC

Christoph Heer - *Senior Director, Infineon Technologies AG*

EDA Challenges in a Design For Zero Defect (ZD) Culture

Ed Nuckolls - *Austin IC R&D, Freescale Semiconductor, Inc.*

Session 3: Panel Discussion: Making Critical Decisions for Emerging SOC Development

4:30 - 5:30pm

Session Chair: Peggy Aycinena - *EDA Confidential*
Session Organizer: Yervant Zorian - *Virage Logic Corp.*

The panel complements the two management presentation sessions (numbers) where the key managers of today's most complex nanometer chips will discuss the emerging solutions and discuss their economic impact. This Management Day panel will provide a unique opportunity for all attending managers to interact directly with the panelists and gain insights from their peers in the industry.

Trade-Off Analysis in Complex SOC Designs

Albert Li - *Director, Global Unichip Corp.*

Panelists:
Rani Borkar - *Vice President, Digital Enterprise Group, Intel Corp.*
Don Friedberg - *Director, Network & Storage Products Group, LSI Logic Corp.*
Pierre Garnier - *Vice President and General Manager, Worldwide Wireless Baseband, Texas Instruments, Inc.*
Christoph Heer - *Vice President Digital IP & Re-Use, Infineon Technologies AG*
Albert Li - *Director, Global Unichip Corp.*
Philippe Magarshak - *Vice President, Central R&D, STMicroelectronics*
Alan Nakamoto - *Vice President, Engineering and Founder, PMC-Sierra, Inc.*
Ed Nuckolls - *Austin IC R&D, Freescale Semiconductor, Inc.*

Reception: 5:30 - 6:00pm

The IC Design Central Partner Pavilion

NEW!

Putting More Design into DAC

The IC Design Central Partner Pavilion brings together vendors supplying products and services that address many of the critical design functions necessary to produce working silicon on time and on budget. Companies from all areas of the design and product development process - EDA, Foundry, IP, Design Services, Assembly/Package, Test, and System Interconnect - must cooperate to offer integrated front-to-back solutions that ensure first-time-successful silicon and predictable time-to-market. Visit the ICDC Partner Pavilion and find design flows and solutions needed to create today's challenging designs.

The ICDC Partner Pavilion is a combination of exhibit booths and 30-minute presentations by each participating vendor. The combination of product displays in the exhibits and technical product presentations in the ICDC Theater offers attendees an in-depth look into flows and methodologies from vendors featuring a variety of products and services for the entire design eco-system.

All presentations take place on the ICDC stage, Booth 4500 in the North Exhibit Hall. See pages 14-15 for details.

IC Design Central Partner Pavilion Presentations

Fidus Systems Inc.: Passive Eye Openers
Monday, July 27, 10:30 - 11:00am

Cambridge Analog Technologies: Ultra-Low Power ADC and Precision PLL
Monday, July 27, 11:00 - 11:30am

Epoch Microelectronics: Modeling and Simulation of an All Digital Phase Locked Loop
Monday, July 27, 11:30am - 12:00pm

Blue Pearl Software: Higher Design Productivity with RTL and Timing Constraint Analysis (1st Showing)
Monday, July 27, 12:30 - 1:00pm

IBM Corp.: Get Your Silicon Design Right the First Time
Monday, July 27, 1:00 - 1:30pm

Cadence Design Systems, Inc./IBM Corp. (1st Showing)
Monday, July 27, 1:30 - 2:00pm

Tiempo: Tiempo IPs and Design Technology: A Breakthrough for Green Semiconductor Devices
Monday, July 27, 2:30 - 3:00pm

Cadence Design Systems, Inc./Virage Logic Corp.: Innovative Power Optimized Memory for Advanced Node SOC Design
Monday, July 27, 3:00 - 3:30pm

APAC IC Layout Consultant, Inc.: Improve your Bottom Line with APAC IC Layout Consultant, Inc.
Monday, July 27, 3:30 - 4:00pm

Warthman Associates: How to Write Maintainable Engineering Specifications
Tuesday, July 28, 10:30 - 11:00am

Chipworks: Reverse Engineering and the Forward Design Flow
Tuesday, July 28, 11:00 - 11:30am

Cadence Design Systems, Inc ./MIPS Technologies: Optimizing Power in Advanced Multicore Systems
Tuesday, July 28, 11:30am - 12:00pm

iNoCs: Networks-On-Chip
Tuesday, July 28, 12:00 - 12:30pm

Blue Pearl Software: Higher Design Productivity with RTL and Timing Constraint Analysis (2nd Showing)
Tuesday, July 28, 12:30 - 1:00pm

Amiq Consulting S.R.L.: DVT Eclipse for Advanced e and SystemVerilog Programming
Tuesday, July 28, 1:00 - 1:30pm

BEEcube, Inc.: Multicore SOC Development on Real-Time Hardware 9 Months Before the Silicon Tapeout
Tuesday, July 28, 1:30 - 2:00pm

Altair Engineering: PBS Grid Works Workload Management 24x7x365 Increases Time to Market
Wednesday, July 29, 2:30 - 3:00pm

Cadence Design Systems, Inc./IBM Corp. (2nd Showing)
Wednesday, July 29, 3:00 - 3:30pm

Enterpoint Ltd.: 101 Ways to Use a Merrick
Wednesday, July 29, 3:30 - 4:00pm

IC Design Central Partner Pavilion - ICDC Stage - Booth #4500

NEW!

Monday, July 27

10:30 - 11:00am

FIDUS SYSTEMS, INC.: PASSIVE EYE OPENERS

Topic Area: Analog/Mixed-Signal/RF Design

In both low speed as well as Giga bits/sec data rate communication systems, the data eye opening is critical. This is most conveniently enhanced at the chip level through pre-emphasis and equalization for high speeds. For low speed operation, no such techniques are available. In this presentation, a study of the use of unconventional terminations, such as inductors and ferrites is examined. It is shown that under certain conditions, a substantial improvement in eye opening is possible for both low and high speed operation. Advantages and limitations of such terminations will be presented.

11:00 - 11:30am

CAMBRIDGE ANALOG TECHNOLOGIES, INC.: ULTRA-LOW POWER ADC AND PRECISION PLL

Topic Area: Analog/Mixed-Signal/RF Design

This talk will focus on CAT's precision analog circuits including ADCs that consume 5x-15x lower power relative to competition, and CAT's all-digital integer and fractional-N PLL for general purpose and ultra-high performance applications below 1ps jitter. Cambridge Analog Technologies, Inc. is a provider of leading edge ultra-low power analog circuits including ADC and PLL catering to SOCs built for a wide array of applications such as wireline, wireless, medical, automotive areas, displays, imaging and embedded control.

11:30am - 12:00pm

EPOCH MICROELECTRONICS, INC.: MODELING AND SIMULATION OF AN ALL DIGITAL PHASE LOCKED LOOP

Topic Area: Analog/Mixed-Signal/RF Design

This talk will describe both a phase domain model and time domain model of an ADPLL. Emphasis will be made on using the models to derive specifications for PLL sub-blocks such as the phase-frequency detector and voltage-controlled oscillator. In addition, the models will be used to derive the specifications for an example fractional-N ADPLL covering 2GHz to 3GHz.

12:30 - 1:00pm

BLUE PEARL SOFTWARE: HIGHER DESIGN PRODUCTIVITY WITH RTL AND TIMING CONSTRAINT ANALYSIS (1ST SHOWING)

Topic Area: Synthesis and FPGA

Blue Pearl Software will present solutions to manage your timing constraints and improve your RTL code, resulting in better QoR through synthesis and P&R for faster timing closure on your complex designs. These design productivity enhancing solutions are available as tools or services to meet customer needs. Come and hear how Cobalt Timing Constraint Generation, Azure Timing Constraint Validation and Indigo RTL Analysis can help you achieve better designs faster.

1:00 - 1:30pm

IBM CORP.: GET YOUR SILICON DESIGN RIGHT THE FIRST TIME

Topic Area: Verification and Test

With any semiconductor device, pre-silicon design verification is critical to the quality, cost, and timeliness of the finished product. This session features a compelling IBM enterprise verification management solution (EVMS) for 24/7 verification that is based on over a decade of in-house experience at IBM. Participants will gain insights on how IBM EVMS / Cadence solution has helped IBM accelerate the pre-silicon verification process while managing growing complexity, enhancing engineering efficiency, and answering the question "are we done with verification?"

1:30 - 2:00pm

CADENCE DESIGN SYSTEMS, INC./IBM CORP. (1ST SHOWING)

Topic Area: General Interest

Please join Cadence and IBM at the DAC IC Design Central Partner Pavilion where they will jointly present details of recent work in their broad and long-standing collaboration to develop innovative technology and design solutions that enable customer success now and into the future. Cadence and IBM – collaborating for customer success.

2:30 - 3:00pm

TIEMPO: TIEMPO IPS AND DESIGN TECHNOLOGY: A BREAKTHROUGH FOR GREEN SEMICONDUCTOR DEVICES

Topic Area: Low-Power Design

TIEMPO develops and markets powerful Core IPs designed in an innovative clock-less and delay-insensitive technology. TIEMPO design technology represents the next breakthrough for ultra-low power and green semiconductor devices as it enables the design of chips that are ultra-low power, ultra-low noise, ultra-low voltage, very robust versus process-voltage-temperature variations and highly secured. TIEMPO IP portfolio includes various microcontroller and crypto-processor cores, and is supported by a design and synthesis flow using standard languages only. For more information, please visit www.tiempo-ic.com.

3:00 - 3:30pm

CADENCE DESIGNS SYSTEMS, INC./VIRAGE LOGIC CORP.: INNOVATIVE POWER OPTIMIZED MEMORY FOR ADVANCED NODE SOC DESIGN

Topic Area: Low-Power Design

Please join Cadence Design Systems and Virage Logic Corporation at the IC Design Central Partner Pavilion to learn about the ease of integration of power optimized memories in multi-media low power SOC applications. Virage Logic Corporation will present new innovative hierarchical low-power memory architecture and IP integration methodology using CPF-based macro modeling that offers excellent control of memory power consumption in demanding mobile applications.

3:30 - 4:00pm

APAC IC LAYOUT CONSULTANT, INC.: IMPROVE YOUR BOTTOM LINE WITH APAC IC LAYOUT CONSULTANT, INC.

Topic Area: General Interest

APAC IC Layout Consultant, Inc. provides quality Analog IC Layout Design Services at very competitive rates. We can help improve your bottom line, help you through a global financial crisis and through an economic recovery.

We have highly competent engineers with experience in processors, chipsets, and Flash memories; we use cutting-edge tools; worked with technology nodes down to 40 nm; familiar with TSMC and Chartered foundry rules.

We protect your work. We deliver. Improve your bottom line with APAC IC.

IC Design Central Partner Pavilion - ICDC Stage - Booth #4500

Tuesday, July 28

10:30 - 11:00am

WARTHMAN ASSOCIATES: HOW TO WRITE MAINTAINABLE ENGINEERING SPECIFICATIONS

Topic Area: General Interest

Engineering specifications often have a life beyond the needs of the design team that writes them. They become a starting point for other documents, including those for new engineering and customer-support employees, patent applications, customer data sheets and reference manuals, and marketing collateral. By creating a clear and well-structured specification, its maintenance and the creation of derivative documents will be easier and faster. This talk covers some basic principles of clear writing and efficient use of editing tools.

11:00 - 11:30am

CHIPWORKS: REVERSE ENGINEERING AND THE FORWARD DESIGN FLOW

Topic Area: New and Emerging Technologies

Using real life examples from Intel's 45nm SRAM macro and Texas Instrument's Chipcon RF device, this session will show a design engineering team how to execute and leverage competitive circuit reverse engineering directly in their own product development workflow.

Chipworks will demonstrate the tools and software used to complete these analyses cost-effectively and without specialized training. We will illustrate how a forward designer can extract schematic data from high magnification images of the microchip layers, and organize the schematics functionally and hierarchically. This data can be analyzed, simulated, and leveraged with a proven track record of getting designs completed faster and with a lower re-spin risk.

11:30am - 12:00pm

CADENCE DESIGN SYSTEMS, INC./MIPS TECHNOLOGIES: OPTIMIZING POWER IN ADVANCED MULTI-CORE SYSTEMS

Topic Area: Low-Power Design

Optimizing power consumption simultaneously with increasing performance demands presents significant design, packaging and cost challenges. Please join Cadence Design Systems and MIPS Technologies at the IC Design Central Partner Pavilion to learn about how Coherent multiprocessing coupled with advanced CPF-based power management capabilities can offer the best performance/power optimization for a given application. This presentation explores advanced power management techniques for state of the art multicore systems using a design flow based upon the Cadence low-power reference flow.

12:00 - 12:30pm

iNoCs: NETWORKS-ON-CHIP

Topic Area: New and Emerging Technologies

Current and future SOCs are composed of a large number of IP blocks and are increasingly hard to integrate, due to performance, timing closure, floorplanning, IP heterogeneity, clocking challenges. iNoCs proposes Network-On-Chips to tackle these issues. A NOC design tool takes high-level communication requirements as an input and outputs NOC RTL, accounting for wirelength and clocking concerns. Existing IP cores can be seamlessly integrated while matching performance and timing constraints. The iNoCs flow saves design effort and optimizes time-to-market.

12:30 - 1:00pm

BLUE PEARL SOFTWARE: HIGHER DESIGN PRODUCTIVITY WITH RTL AND TIMING CONSTRAINT ANALYSIS (2ND SHOWING)

Topic Area: Synthesis and FPGA

Blue Pearl Software will present solutions to manage your timing constraints and improve your RTL code, resulting in better QoR through synthesis and P&R for faster timing closure on your complex designs. These design productivity enhancing solutions are available as tools or services to meet customer needs. Come and hear how Cobalt Timing Constraint Generation, Azure Timing Constraint Validation and Indigo RTL Analysis can help you achieve better designs faster.

Tuesday, July 28

1:00 - 1:30pm

AMIQ CONSULTING S.R.L.: DVT ECLIPSE FOR ADVANCED e AND SYSTEMVERILOG PROGRAMMING

Topic Area: Verification and Test

Today verification engineers use advanced languages like e or SystemVerilog, and spend significant time developing verification environments, in other words programming. In the software industry advanced smart editors (called IDEs - Integrated Development Environments) combine syntax checker, linter, class browser, revision control and other useful tools, and enable faster and better code development, both for beginners and complex maintenance. Verification engineers should use similar tools and improve productivity and quality.

1:30 - 2:00pm

BEEcube, Inc.: MULTICORE SOC DEVELOPMENT ON REAL-TIME HARDWARE 9 MONTHS BEFORE THE SILICON TAPEOUT

Topic Area: System-Level and Embedded

The multicore SOC design challenge is how to provide software developers with a hardware implementation fast enough for executing binary compatible software, while allowing hardware designers to continue optimizing the final silicon implementation. BEEcube's BEE3 system provides such an environment, by integrating HW/SW co-development processes with real-time implementation of full multicore SOCs. This provides a 9-month time advantage in the development. The BEE3 systems have been deployed in many leading companies and universities worldwide, including Microsoft and Sun Microsystems.

Wednesday, July 29

2:30 - 3:00pm

ALTAIR ENGINEERING: PBS GRID WORKS WORKLOAD MANAGEMENT 24x7x365 INCREASES TIME TO MARKET

Topic Area: General Interest

Altair PBS software addresses the complex computing performance demands of EDA chip design. Altair software delivers highly available, scalable grids, cloud and HPC cluster computing.

Altair PBS Software suite consists of PBS web portals to streamline workload, PBS Professional which maximizes performance from multicore architectures to reduction of power via Green Provisioning, PBS Analytics reports hardware and software usage patterns over a specified period of time by generating reports for example: license usage, jobs, users, projects and Altair HiQube Business Intelligence tool which provides you the ability to analyze your overall business from several perspectives.

Altair provides enterprises the ability to maximize ROI on all computing infrastructure assets resulting in a competitive edge.

3:00pm - 3:30pm

CADENCE DESIGN SYSTEMS, INC./IBM CORP. (2ND SHOWING)

Topic Area: General Interest

Please join Cadence and IBM at the DAC IC Design Central Pavilion where they will jointly present details of recent work in their broad and long-standing collaboration to develop innovative technology and design solutions that enable customer success now and into the future. Cadence and IBM – collaborating for customer success.

3:30pm - 4:00pm

ENTERPOINT LTD.: 101 WAYS TO USE A MERRICK

Topic Area: New and Emerging Technologies

A brief introduction to our new Merrick family, future products, and discuss specifically the first release Merrick1 with 101 FPGAs on board. We analyze ways of applying a Merrick platform to the fields of ASIC Development and Parallel Processing Applications and in detail explain some of the features specifically for these applications.

We also examine how cost effective custom versions of the platform can be created quickly for customer specific needs.

Rm: 132

1U ROBUST DESIGN AND TEST

Topic Area: Interconnect and Reliability **Tuesday - July 28, 10:30am - 12:00pm**

Moderators: Jarrod Brooks - *Cypress Semiconductor Corp., Lexington, KY*
Srinivas Nori - *Microsoft Corp., Mountain View, CA*

Automotive parts need to be very robustly designed for Electromagnetic Interference (EMI). Designers at STMicroelectronics will describe their approach to reduce EMI. Wherein image sensors need to be signed off taking into account IR drop and voltage derating. Aptina Imaging Corp. will describe their approach to designing a robust sensor. Samsung will present how, through various biasing techniques, their ASICs and SOCs are made more robust. Power usage in test mode is becoming a real problem for low-power devices and if not moderated carefully can lead to permanent damage of the device. STMicroelectronics describes their answer to this problem.

1U.1 Electromagnetic Interference Reduction on an Automotive Microcontroller
Patrice Joubert Doriol, **Davide Pandini,** Cristiano Forzan, Mario Rotigni, Giovanni Graziosi - *STMicroelectronics, Agrate Brianza, Italy*
Yamarita Villavicencio - *Politecnico di Torino, Torino, Italy*

1U.2S Power Integrity Sign-Off Flow Using CoolTime and PrimeTime-SI -- Flow and Validation
Hang Li - *Aptina Imaging Corp., San Jose, CA*

1U.3S Improving Parametric Yield in DSM ASIC/SOC Design
Jung Yun Choi, Bong Hyun Lee, Kyung-Tae Do, Hyung-Ock Kim, Hyo-Sig Won, Kyu-Myung Choi - *Samsung, Yongin City, Republic of Korea*

1U.4 Low-Power Test Methodology
Swapnil Bahl, Akhil Garg - *STMicroelectronics, Greater Noida, India*
Roberto Mattiuzzo, Saverio Graniello, Davide Appello - *STMicroelectronics, Agrate Brianza, Italy*
Matthieu Sautier - *STMicroelectronics, Crolles, France*

Rm: 132

2U PRACTICAL PHYSICAL DESIGN

Topic Area: Physical Design **Tuesday - July 28, 2:00 - 4:00pm**

Moderators: Guntram Wolski - *Cisco Systems, Inc.,*
Sorin Dobre - *Qualcomm, Inc., San Diego, CA*

How do you apply ECOs late in the design process? Register arrays occupy more than half of all transistors of modern designs. Are there ways to automate these design register arrays? How do you distribute clocks on large ASICs? In this session, come and find out how Intel Corp. attacks these problems. DSPs often require more than the standard ASIC methodologies offer. Qualcomm, Inc. will describe how they build their semi-custom methodology. Finally, STMicroelectronics engineers describe how they use IP-XACT standard from Spirit to enable IP reuse.

2U.1 Automated Pseudo-Flat Design Methodology for Register Arrays
Raj R. Varada, Ragadeepika Kshatri, Andrew G. Spix - *Intel Corp., Santa Clara, CA*

2U.2 Qualcomm DSP Semi-Custom Design Flow: Leveraging Place and Route Tools in Custom Circuit Design
Nadeem Eleyan, Masud Kamal, Baker Mohammad, Paul Bassett - *Qualcomm, Inc., Austin, TX*
Ken Lin - *Qualcomm, Inc., Cardiff by the Sea, CA*

2U.3S Auto ECO Flow Development for Functional ECO Using Efficient Error Rectification Method Based on Conformal
Andal Jayalakshmi - *Intel Corp., Penang, Malaysia*

2U.4S Monte Carlo Techniques for Physical Synthesis Design Convergence Exploration
Andrew G. Spix, **Raj R. Varada** - *Intel Corp., Santa Clara, CA*

2U.5S Tortoise: Chip Integration Solution
Giorgio Mastrorocco, Alvaro Ferrera - *STMicroelectronics, Agrate Brianza, Italy*
Bhawna Chopra, **Mukesh Chopra** - *STMicroelectronics, Greater Noida, India*

2U.6S ASIC Clock Distribution Design Challenges
Siong Kiong Teng - *Intel Corp., Penang, Malaysia*

Rm: 132

3U VERIFICATION: A FRONT-END PERSPECTIVE

Topic Area: Verification and Test **Tuesday - July 28, 4:30 - 6:00pm**

Moderator: Alicia Strang - *Marvell Semiconductor, Inc., Aliso Viejo, CA*

This session highlights advances in verifying various aspects when designing complex systems. The first paper explores using interactive 2-D projections to improve the understanding of multi-dimensional cross coverage results. The second paper initiates a novel direction in using abstract executable models to verify power management protocols. The third paper describes an improved environment for embedded device driver verification including constrained random testing of the software-hardware interface.

3U.1 Interactive 2-D Projection Cross Coverage Viewer for Coverage Hole Analysis
Keisuke Shimizu - *ClueLogic, Sunnyvale, CA*
Tomohisa Iida - *Verifore, Inc., Kanagawa, Japan*

3U.2 Verification of Power Management Protocols Through Abstract Functional Modeling
Vivekananda Vedula - *Intel Corp., Bangalore, India*
Gila Kamhi, Tali Levy, Muhammad K. Mhameed, Eli Singerman, Yael Zbar - *Intel Corp., Haifa, Israel*
Niranjan M. M, Raj Bahadur S. Rajput, Vivekananda Vedula - *Intel Corp., Bangalore, India*
Harish M. Rawlani - *Ipflex, Inc., Bangalore, India*

3U.3 Design Flow for Embedded System Device Driver Development and Verification
Jason Andrews - *Cadence Design Systems, Inc.,Arden Hills, MN*
Ross Dickson - *Virtutech, San Jose, CA*
Jakob Engblom - *Virtutech, Stockholm, Sweden*

Rm: 132

4U TIMING ANALYSIS IN THE REAL WORLD

Topic Area: Physical Design **Wednesday - July 29, 9:00 - 11:00am**

Moderator: Tom Dillinger - *Advanced Micro Devices, Inc., Sunnyvale, CA*

How do you mix gate-level and transistor-level timing analysis? How is statistical timing applied in practice to processor designs? How does one effectively merge timing constraints from multiple domains, model network variation, and account for single-event upsets? All of these questions will be answered in this session by users who found ways to deal with these.

4U.1 Design of a Single-Event Effect Fault Tolerant Microprocessor for Space Using Commercial EDA Tools
Roland Weigand - *European Space Agency, Noordwijk, The Netherlands*
Jean Edelin - *Atmel Corp., Nantes, France*

4U.2 SSTA and Its Application to SPARC 64™ Processor Design
Noriyuki Ito, Hiroaki Komatsu, Hiroyuki Sugiyama, Katsumi Iguchi, Naomi Bizen, Yuji Yoshida - *Fujitsu, Kawasaki, Japan*

4U.4S Unifying Transistor- and Gate-Level Timing Through the Use of Abstraction
Frank Borkam - *IBM Corp., San Mateo, CA*
Alex Rubin - *IBM Corp., Santa Clara, CA*
Uwe Fassnacht - *IBM Corp., Mountain View, CA*

4U.3S A Hierarchical Transistor and Gate-Level Statistical Timing Flow for Microprocessor Designs
Debjit Sinha, Adil Bhanji, Kerim Kalafala, Natesan Venkateswaran, Sachin Gupta - *IBM Corp., Hopewell Jct., NY*
Chandu Visweswariah, Gary Ditlow - *IBM Corp., Yorktown Hts., NY*

4U.5S The Automatic Generation of Merged-Mode Design Constraints
Subrangshu K. Das, Aishwarya Singh - *Texas Instruments, Inc., Bangalore, India*
Ajay J. Daga, Vikas Sachdeva - *FishTail Design Automation, Lake Oswego, OR*

4U.6S Modeling Clock Network Variation in Timing Verification
Tong Xiao, An-Jui Shey, Jiyang Cheng, Rob Mains, Georgios K. Konstadinidis, George Chen - *Sun Microsystems, Inc., Santa Clara, CA*

Concourse Level

5U POSTER SESSION AND ICE CREAM SOCIAL

Topic Area: General Interest

Wednesday - July 29, 1:30 - 3:00pm

The poster session includes approximately 40 posters on topics that span both front-end and back-end design.
The posters will offer an opportunity for personal interaction with EDA tool users from many leading companies.

USER TRACK FRONT-END

3-D Visualization of Integrated Circuits in the Electric™ VLSI Design System
Steven Rubin, Gilda Garreton - *Sun Microsystems, Inc., Menlo Park, CA*

Automatic Generation, Execution and Performance Monitoring of a Family of Multiprocessors on Large Scale Emulator
Xinyu Li, Omar Hammami - *NSTA, Paris, France*
Ludovic Larzul - *EVE, Palaiseau, France*

C-Based Hardware Design Using AutoPilot™ Synthesizing MPEG-4 Decoder onto Xilinx FPGA
Jason Cong - *Univ. of California, Los Angeles, CA*
Zhiru Zhang - *AutoESL Design Technologies, Inc., Los Angeles, CA*
Yi Zou - *Univ. of California, Los Angeles, CA*

C-Based High-Level Synthesis of a Signal Processing Unit Using Mentor Graphics Catapult C
Axel Braun, Tobias Oppold, Joachim Gerlach, - *Univ. of Tübingen, Tuebingen, Germany*
Holger Janssen - *Robert Bosch GmbH, Hildesheim, Germany*
Wolfgang Rosenstiel - *Univ. of Tübingen, Tuebingen, Germany*

Design and Verification Challenges of ODC-Based Clock Gating
Chaiyasit Manovit, Sridhar Narayanan, Sridhar Subramanian - *PwrLite, Inc., Santa Clara, CA*

Effective Debugging Chip-Multiprocessor Design in Acceleration and Emulation
Yunji Chen - *Chinese Academy, Beijing, China*

Enabling IP Quality Closure at STMicroelectronics with VIP Lane
Olivier Florent - *STMicroelectronics, Grenoble, France*
Stéphane Bonniol - *Satin IP Technologies, Montpellier, France*

Formal Verification Based Automated Approaches to System-On-Chip DFT Logic Verification
Subir Roy, Rubin Parekhji - *Texas Instruments, Inc., Bangalore, India*

Interactive Code Optimization for Dynamically Reconfigurable Architecture
Kenji Funaoka, Mayuko Koezuka, Akira Kuroda, Hidenori Matsuzaki, Takashi Yoshikawa, Shigehiro Asano - *Toshiba Corp., Kanagawa, Japan*

Power Gated Design Optimization and Analysis with Silicon Correlation Results
Lee Kee Yong, Fern Nee Tan, Sze Geat Pang - *Intel Corp., Penang, Malaysia*

SystemC: A Complete Digital System Modeling Language: A Case Study
Reni John - *Rambus, Inc., Los Altos, CA*

Transforming Simulators into Implementations
Nikhil Patil, Derek Chiou - *Univ. of Texas, Austin, TX*

Using Algorithmic Test Generation in a Constrained Random Test Environment
Håkan Askdal - *EAB (Ericsson AB), Kista, Sweden*

Visualizing Debugging Using Transaction Explorer in SOC System Verification
Alicia Strang, Robert Carden IV - *Marvell Semiconductor, Inc., Aliso Viejo, CA*

USER TRACK BACK-END

A Generic Clock Domain Crossing Verification Flow
Tayeb Bouguerba - *Advanced Micro Devices, Inc., Markham, ON, Canada*

Roger Sabbagh - *Mentor Graphics Corp., Ottawa, Ontario, Canada*

A Simple Design Rule Check for DP Decomposition
Chih-Hsien Tang, Kuen-Yu Tsai - *National Taiwan Univ., Taipei, Taiwan*

Algorithm for Analyzing Timing Hot-Spots
Bhargav Joshi - *Einfochips, Inc., Ahmedabad, India*

An On-Chip Variation Monitor Methodology Using Cell-Based P&R Flow
Yu-Ting Hung, Yu-Wen Tsai - *Faraday Technology Corp., Hsinchu, Taiwan*

Application and Extraction of IC Package Electrical Models for Support of Multi-Domain Power and Signal Integrity Analysis
Om Mandhana, Jon Burnett - *Freescale Semiconductor, Inc., Austin, TX*
Sam Chitwood, Brad Brim - *Sigrity, Inc., Santa Clara, CA*

Applications of Platform Explorer, Integrator and Verifier in SOC Designs
Byeong Min, Kwang-Hyun Cho, Jaebeom Kim, Chi-Ho Cha, Junhyung Um, Euibong Jung, Sik Kim, Kyu-Myung Choi - *Samsung, Yongin City, Republic of Korea*

Assertion Based Formal Verification in SOC Level
Jentil Jose, Varun Nair - *Wipro Technologies, Cochin, India*

Attacking Constraint Complexity in Verification IP Reuse
Ben Chen, Srinath Atluri, Harish Krishnamoorthy - *Cisco Systems, Inc., San Jose, CA*
Alex Wakefield, Balamurugan Veluchamy - *Synopsys, Inc., Mountain View, CA*

Automated Assertion Checking in Static Timing with IBM ASICs
Nathan Buck - IBM Corp., *Underhill, VT*
William Rose - *IBM Corp., Research Triangle Park, NC*

Case Study of Diagnosing Compound Hold-Time Violations
Shuo-Fen Kuo, Rei-Lung Chen, Jih-Nung Lee, Chi-Feng Wu - *Realtek Semiconductor Corp., Hsinchu, Taiwan*
Dragon Hsu, Ting-Pu Tai - *Mentor Graphics Corp., Hsinchu, Taiwan*
Yu Huang - *Mentor Graphics Corp., Marlboro, MA*
Wu-Tung Cheng - *Mentor Graphics Corp., Wilsonville, OR*

Design Profiling - Modeling the ASIC Design Process
Tom Guzowski - *IBM Corp., Essex Jct., VT*

Enhanced SDC Support for Relative Timing Designs
Eric Quist , Peter Beerel, - *Univ. of S. California, Los Angeles, CA*
Kenneth Stevens - *Univ. of Utah, Salt Lake City, UT*

Hold Time ECO for Hierarchical Design
Albert Li - *Global Unichip Corp., Hsinchu, Taiwan*
J.J. Hsiao - *Dorado Design Automation, Inc., Hsinchu, Taiwan*

Improving the Automation of the System in Package (SIP) Design Environment via a Standard and Open Data Format
Alain Caron - *IBM, Burlington, VT*

Interconnect Explorer: A High-Level Power Estimation Tool for On-Chip Interconnects
Antoine Courtay, Johann Laurent, Olivier Sentieys, Nathalie Julien - *Univ. de Bretagne, Lorient, France*

Managing Information Silos: Reducing Project Risk through Multi-Metric Tracking
Christopher Kappler, Gregory Goss - *Achilles Test Systems, Inc., Waltham, MA*

Net-List Level Test Logic Insertion: Flow Automation for MBIST and Scan
Chejen Chang, Nikhil Herlekar - *Broadcom Corp., Markham, ON, Canada*

Physical Implementation of Retention Cell Based Design
Alpesh Kothari - *Atoptech, Inc., Santa Clara, CA*

Sequential Clock Gating Optimization in GPU Designs with PowerPro CG
Tayeb Bouguerba - *Advanced Micro Devices, Inc., Markham, ON, Canada*

Soft-Error-Rate Estimation in Sequential Circuits Utilizing a Scan ATPG Tool
Masaki Shimada, Michio Komoda, Yoshiaki Fukui - *Renesas Technology Corp., Tokyo, Japan*
Minoru Ito - *Hitachi, Ltd., Tokyo, Japan*
Kan Takeuchi - *Renesas Technology Corp., Tokyo, Japan*

Solving FPGA Clock-Domain Crossing Problems: A Real-World Success Story
Timothy Paige - *North Pole Engineering, Inc., Minneapolis, MN*
Gordon Braun - *Honeywell International Inc., Minneapolis, MN*
Chris Rockwood - *Mentor Graphics Corp., Milwaukee, WI*

Static Timing Analysis of Single Track Circuits
Prasad Joshi, Peter Beerel - *Univ. of Southern California, Los Angeles, CA*
Jonathan Gainsley, Ivan Sutherland - *Sun Microsystems, Inc., Menlo Park, CA*
Marly Roncken - *Intel Corp., Hillsboro, OR*

Timing Closure in 65-Nanometer ASICs Using Statistical Static Timing Analysis Design Methodology
Llewellyn Marshall, Eric Foreman - *IBM Corp., Essex Jct., VT*

Using STA Information for Enhanced At-Speed ATPG
Colin Renfrew, Ashu Razdan - *Freescale Semiconductor, Inc., Austin, TX*
Bruce Swanson - *Mentor Graphics Corp., Wilsonville, OR*

User Track

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Please view the DAC Schedule for a more detailed display of the dates and times.

6U TOWARD FRONT-END DESIGN PRODUCTIVITY

Rm: 132

Topic Area: System-Level and Embedded **Wednesday - July 29, 3:00 - 4:00pm**

Moderator: Peter Nord - ST-Ericsson, Lund, Sweden

This session focuses on a variety of tools that enhance design productivity. The first paper presents a successful chip/package/PCB codesign flow that has been deployed in more than 30 SIP projects and outlines specific, related challenges to vendors. The second paper describes the use of an FPGA resources estimation tool to allow quick design analysis. The final paper describes a methodology to empower front-end designers to prototype and evaluate the design at the architecture level.

6U.1 Unified Chip/Package/Board Codesign Flow for Laminate, Leadframe, and Wafer-Level Packages in a Distributed Design Environment

Thomas Brandtner, Luca Della Ricca - *Infineon Technologies AG, Villach, Austria*
Markus Pistauer - *CISC Semiconductor Design+Consulting GmbH, Klagenfurt, Austria*
Janez Jaklic - *Cadence Design Systems, Inc., Feldkirchen, Germany*

6U.2S Fast FPGA Resource Estimation

Paul Schumacher - *Xilinx, Inc., Longmont, CO*
Pradip Jha - *Xilinx, Inc., San Jose, CA*

6U.3S Assessing Design Feasibility Early with Atrenta's 1Team®-Implement SOC

Thierry T. Sejourne - *STMicroelectronics, Grenoble, France*
Paolo Petroni - *Atrenta, Inc., Meylan, France*

7U FRONT-END DEVELOPMENT: EMBEDDED SOFTWARE AND DESIGN EXPLORATION

Rm: 132

Topic Area: System-Level and Embedded **Wednesday - July 29, 4:30 - 6:00pm**

Moderator: Tor Jeremiassen - *Texas Instruments, Inc., Houston, TX*

The first paper explores the productive application of use cases to the development of embedded software. The second paper outlines steps to extract parallelism from the AVS video decoding application, mapping it to a heterogeneous dual-core to enable real-time video decoding. The third paper links several design and verification components to enhance design space exploration. The fourth paper examines the utility of HLS from several angles. The last paper proposes a light-weight switching infrastructure that allows for loosely-timed and approximately-timed switchable models.

7U.1S Applying Use Cases to Microcontroller Code Development

Chris R. Gilbert - *Cypress Semiconductor Corp., Colorado Springs, CO*

7U.2S Mapping the AVS Video Decoder on a Heterogeneous Dual-Core SIMD Processor

Nikolaos Bellas, Ioannis Katsavounidis, Maria Koziri, Dimitrios Zacharis - *Univ. of Thessaly, Volos, Greece*

7U.3S An "Algorithm to Silicon" ESL Design Methodology

Nitin Chawla, Harvinder Singh - *STMicroelectronics, Greater Noida, India*
Pascal Urard - *STMicroelectronics, Crolles, France*

7U.4S Necessary but Not Sufficient: Lessons and Experiences with High-Level Synthesis Tools

Soujanna Sarkar, Shashank Dabral, Raj S. Mitra - *Texas Instruments, Inc., Bangalore, India*
Praveen Tiwari - *Interra Systems, Inc. Bangalore, India*

7U.5 Switching Mechanism in Mixed TLM-2.0 LT/AT System

Zhu Zhou, Dharmin Parikh, Atul Kwatra - *Intel Corp., Chandler, AZ*
Pradnyesh Gudadhe - *Arizona State Univ., Tempe, AZ*

8U POWER ANALYSIS AND IP REUSE

Rm: 132

Topic Area: Low-Power Design **Thursday - July 30, 9:00 - 11:00am**

Moderators: Kyu-Myung Choi - *Samsung, Yongin City, Gyeonggi-Do, Republic of Korea*
Kaijian Shi - *Synopsys, Inc., Dallas, TX*

Accurate power supply and substrate noise analysis remains a challenge. Practitioners from Qualcomm, Inc., IBM Corp., Samsung and STARC will show how they attacked the problem. IP blocks need to be designed to be used in many different environments. Texas Instruments, Inc. shows how to analyze blocks for reuse in multiple metal stacks. Assessing a design feasibility early in the process can avoid many problems later. Intel Corp. shows their approach.

8U.1 Dynamic Power Analysis for Custom Macros Using ESP-CV

Stephen Bijansky, Bassam Mohd, Baker Mohammad - *Qualcomm, Inc., Austin, TX*

8U.2 Power Supply and Substrate Noise Analysis; Reference Tool Experience with Silicon Validation

Yoji Bando, Makoto Nagata - *Kobe Univ., Kobe, Japan*
Daisuke Kosaka - *The ARTEC Corp., Kobe, Japan*
Goichi Yokomizo, Kunihiko Tsuboi- *STARC, Yokohama, Japan*
Ying Shiun Li, Shen Lin - *Apache Design Solutions, Inc., San Jose, CA*

8U.3S Modeling and Design Challenges for Multicore Power Supply Noise Analysis

Ben Mashak, Bill Hovis - *IBM Corp., Rochester, MN*
Howard Chen - *IBM Corp., Yorktown Hts., NY*

8U.4S Dynamic Power Noise Analysis Method for Memory Designs

Chanseok Hwang - *Samsung, Hwasung, Republic of Korea*

8U.5S Hard IP Reuse in Multiple Metal Systems SOCs

Aish Dubey, Dhanabal G - *Texas Instruments, Inc., Bangalore, India*
Anurag Gupta- *Freescale Semiconductor, Inc., Noida, India*

8U.6S Apache Redhawk di/dt Mitigation Method in Power Delivery Design and Analysis

Julius Delino, **Thao N. Pham**, Farag Fattouh - *Intel Corp., Folsom, CA*

9U FRONT-END POWER PLANNING AND ANALYSIS

Rm: 132

Topic Area: System-Level and Embedded **Thursday - July 30, 2:00 - 4:00pm**

Moderator: Gilda Garreton - *Sun Microsystems, Inc., Menlo Park, CA*

The first paper presents the experiences of using an automated flow to pre-characterize the power consumption of a set of basic components starting from their behavioral description in C, down to their power estimation at the gate netlist level. The second paper describes the use of a power noise analysis tool to analyze system power integrity. The third paper describes tool use to integrate complex multi-power/voltage domain design. The fourth paper presents a flexible, high-level power management modeling and simulation framework for power architects. The fifth paper outlines an exploratory and refinement-based power planning system.

9U.1 Power Library Pre-Characterization Automation

Benjamin Carrion Schafer, Kazutoshi Wakabayashi - *NEC Corp., Kawasaki, Japan*
Lokesh Kumar - *NEC HCL ST, Noia, India*

9U.2S Chip - Package - PC Board Codesign: Applying a Chip Power Model in System Power Integrity Analysis

Rick Brooks, Jane Lim, Udupi Harisharan - *Cisco Systems, Inc., San Jose, CA*

9U.3S New SOC Integration Strategies for Multi-Million Gate, Multi-Power/Voltage Domain Designs

Sarveswara Tammali - *Texas Instruments, Inc., Bangalore, India*
David R. Matt - *Texas Instruments, Inc., Missouri City, TX*
Bernard Murphy - *Atrenta, Inc., San Jose, CA*

9U.4 PETRA: A Framework for System-Level Dynamic Thermal and Power Management Exploration

Yoni Aizik, Muhammad K. Mhameed - *Intel Corp., Haifa, Israel*

9U.5 ALPES: Architectural-Level Power Planning and Estimation

Francis Maquin, Roberto Guizzetti - *STMicroelectronics, Crolles, France*
Jean-Claude Longchambon- *ST-NXP Wireless, Grenoble, France*
Ashley Crawford- *ST-Ericsson, Fleet, United Kingdom*

10U ADVANCES IN ANALOG AND MIXED-SIGNAL DESIGN

Rm: 132

Topic Area: Analog/Mixed-Signal/RF Design **Thursday - July 30, 4:30 - 6:00pm**

Moderators: Sorin Dobre - *Qualcomm, Inc., San Diego, CA*
Raj R. Varada - *Intel Corp., Santa Clara, CA*

Reuse of analog designs is becoming as important as in digital design. A team from Stanford Univ., Rambus, Inc. and Netlogic describes their way to tackle this problem. A group from Cadence and Taiwanese universities will described their approach to integrate MEMs in mixed-signal designs. A team from NXP Semiconductors and Magwel NV tackled the problem of analyzing substrate noise and presents results on a 90nm technology. Complex circuits often need an integrated approach to physical and electrical verification. A team from SySDSoft, Inc. and Mentor Graphics Corp. describes how to do this on their designs.

10U.1 A Schematic Symbol Library for Collaborative Analog Circuit Development Across Multiple Process Technologies

Jaeha Kim, Metha Jeeradit - *Stanford Univ., Stanford, CA*
Aida Varzaghani- *NetLogic Microsystems, Inc., Mountain View, CA*
Ingrid Huang- *Rambus, Inc., Los Altos, CA*

10U.2 A Mixed-Signal/MEMS CMOS Codesign Flow with MEMS-IP Publishing/Integration

Che-Sheng Chen, Kuei-Ann Wen - *National Chaio Tung Univ., Hsinchu, Taiwan*
Long-Sheng Fan - *National Taiwan Univ., Hsinchu, Taiwan*

10U.3S Substrate Noise Isolation Characterization in 90nm CMOS Technology

Sergei Kapora - *NXP Semiconductors, Eindhoven, The Netherlands*
Peter Meuris, Wim Schoenmaker - *Magwel NV, Leuven, Belgium*

10U.4S An Integrated Physical-Electrical Design Verification Flow

Hazem M. Hegazy - *Mentor Graphics Corp., Cairo, Egypt*
Emad Hegazi - *SySDSoft, Inc., Cairo, Egypt*

S - denotes a short paper | Orange titles signify a best paper candidate

Exhibitor Forum - Booth #4359

Monday, July 27

10:15am - 12:15pm

ARCHITECTURAL EXPLORATION: SYSTEM-LEVEL DESIGN AND EMBEDDED SOLUTIONS

Topic Area: System-Level and Embedded

CoWare, Inc.

Addressing the Design Challenges of ARM-Based LTE Mobile Phone Designs Using System Virtualization

Software availability becomes an increasingly important factor in product differentiation. Virtualization offers a methodology to develop software in the context of the actual design without the need for physical hardware. CoWare, Inc. will demonstrate how its unique Electronic System Virtualization solution addresses the design challenges that hardware and software engineers working on LTE mobile phone designs are facing. CoWare's IP model partners, ARM, Ltd. and Carbon Design Systems, Inc. will explain how their respective modeling technology plays a vital role in modeling ARM, Ltd.'s IP within this solution.

Speakers: **Tom De Schutter** - *CoWare, Inc., San Jose, CA*
Joachim Krech - *ARM Ltd., Aachen, Germany*
Bill Neifert - *Carbon Design Systems, Inc., Acton, MA*

Lynguent, Inc.

System-Level Design with an IME and an Analog IC Simulator

The composition and analysis of a Sigma-Delta Data Converter model using the ModLyng-IME, the Simulink Emulation Toolkit, and the Spectre circuit simulator is discussed. Composition of both the model under test, and the testbench from a library of effects is described. Exporting the model and testbench from the ModLyng-IME through CdsLynk into the Virtuoso IC design environment is explored in the context of SOC architectural design, functional verification, and model reuse.

Speaker: **Jim Holmes** - *Lynguent, Inc., Fayetteville, AR*

CoFluent Design

Early Architecture Exploration of Multicore HW/SW Systems

Architecting parallel real-time applications for multicore-based systems presents important design challenges. CoFluent Studio addresses many of these challenges by allowing for early architecture exploration of HW/SW systems, and providing performance and power estimations from graphics and ANSI C/C++. This system-level approach — based on graphical modeling and SystemC automatic generation and simulation techniques — provides a unique ability to secure system architect in their design trade-off decisions before committing to implementation details (no embedded software code, no hardware IPs required).

Speaker: **Laurent Isenegger** - *CoFluent Design, San Jose, CA*

2:00 - 4:00pm

CHIP MODELING AND ESTIMATION: PREVENTING DESIGN FAILURE THROUGH POWER ANALYSIS FOR IP AND CHIP DESIGNS

Topic Area: Verification and Test

Cadence Design Systems, Inc.

InCyte Chip Estimator with Low-Power Integration

Design teams continue to encounter issues where final silicon does not match the initial specification. The results of the mismatch can range from non-optimized designs that cost extra dollars (for example, due to larger die area, or higher power consumption) to missed market windows due to required re-design. Our tutorial will focus on Cadence's InCyte Chip Estimator holistic view of the chip estimation process, leveraging a powerful IP database. Major focus will be on InCyte's newly expanded low-power estimation capabilities.

Speaker: **Kenneth Chang** - *Cadence Design Systems, Inc., San Jose, CA*

Apache Design Solutions, Inc.

De-Risking Your Design from Power Noise Impact

Mitigating the risk of design failure late in the process requires early-stage prototyping to understand the impact of physical implementation choices, such as number of layers, density of the power/ground grids, number and position of the power/ground pads, and de-cap and package selections. Apache's products including RedHawk, CPM, PsiWinder, and Sentinel provide prototyping features enabling designers to test different implementation choices without any physical data (before floorplanning) and prevent power noise issues from early in the project to final sign-off.

Speaker: **Jerome Toublanc** - *Apache Design Solutions, Inc., Sophia-Antipolis, France*

Mentor Graphics Corp.

Vista: An Architectural Power Solution Creating TLM 2.0 Power Models Based on Gate-Level Physical Power Characterization

Vista offers a unique technology with which IP providers and semiconductors can automatically and accurately model power at TLM (transaction-level modeling) abstractions based on the physical implementation and technology process of the underlined IP's. Hence, users can automatically create power models for all their legacy RTL blocks and plug them into their new TLM platform. Today, when ESL and TLM 2.0 (SystemC) methodologies deployment is rapidly growing, having accurate power metrics at the TLM is of great value. At the TLM architecture-level, one can run numerous iterations at very high speeds, test architecture trade-offs and get insights into power under functional simulation and real-life software use cases; resulting with substantial power reduction opportunities. Vista uses gate-level simulation scenarios (VCDs) and the physical attributes of the cells (.lib) to accurately characterize the power behavior based on the functional state and data activity. All of the power ingredients are characterized (dynamic, static and clock power) and maintained at the TLM model. The power model is then annotated into TLM 2.0 functional model and provides accurate power data through TLM simulation.

Speaker: **Rami Rachamin** - *Mentor Graphics Corp., Wilsonville, OR*

Exhibitor Forum - Booth #4359

Tuesday, July 28

1:00 - 3:00pm

SYSTEM INTEGRATION: ARCHITECTURAL FLOWS, DDM, AND DRC

Topic Area: System-Level and Embedded

Cadence Design Systems, Inc.

System-Level Design and Chip Architecture Flow for Low-Power ICs

This presentation teaches designers how to make smarter trade-offs at the IP and SOC level to optimize IC power consumption vs. area, clock-speed, and throughput. Designers will learn how new technologies for chip planning, high-level synthesis and dynamic power analysis are used to evaluate critical power, area, and timing aspects of a design, and realize optimum results for different applications.

Speaker: **Steve Svoboda** - *Cadence Design Systems, Inc., San Jose, CA*

ClioSoft, Inc. and Synopsys, Inc.

Effective Data Management for AMS Design Teams

Large and geographically dispersed AMS design teams face the challenge of collaborative design data management (DDM) for semiconductor projects. A proper DDM solution must handle the design, the libraries and collateral data, and seamlessly integrate into the user's design flow. Learn how to improve team productivity through efficient data management while reducing re-spins and meeting schedules. The solution presented uses Synopsys' Custom Designer integrated with ClioSoft's SOS DDM platform, providing a complete OpenAccess solution to maximize team productivity.

Speakers: **Les Spruiell** - *Synopsys, Inc., Mountain View, CA*
Karim Khalfan - *Cliosoft, Inc., Fremont, CA*

Mentor Graphics Corp.

Using Equation-Based DRC to Solve Physical Verification Challenges

Traditional design rules leave die real estate "on the table" to ensure manufacturability. Equation-based DRC allows designers to define rules in terms of arbitrarily complex 3-D functions of layout geometry. This eliminates complicated interpolation tables that result in excessive margins. It also simplifies coding of advanced checks, reduces deck size, and provides quantitative "fix hints" that help in debugging. This presentation explains equation-based DRC with specific examples of how to use it on real problems faced by designers today.

Speaker: **David Abercrombie** - *Mentor Graphics Corp., Wilsonville, OR*

3:00 - 5:00pm

DESIGN FOR X: TEST, POWER, AND DESIGN VALIDATION

Topic Area: Verification and Test

DAFCA, Inc.

Doing More with Less: Accelerating FPGA and ASIC Validation with Synthesizable Programmable Instruments

As modern SOC designs grow in size and complexity there is increasing need for better on-chip visibility of hardware and embedded software. This need is most evident in large FPGAs, ASICs and ASIC prototyping systems. When combined with automated insertion and off-chip analysis software, programmable instrumentation enables the most flexible and cost effective solution. By way of example, we will show how ClearBlueFPGA, Altera Quartus SOPC Builder and NIOS IDE are used to instrument and co-validate on-chip hardware and software.

Speakers: **Phil Simpson** - *Altera Corp., San Jose, CA*
Paul Bradley - *DAFCA, Inc., Framingham, MA*

Sequence Design, Inc.

Designing for Power

Design for Power (DFP) has become an essential component of product development. A power-efficient design methodology will embody several DFP concepts, especially power analysis and optimization during all phases of the design process from system design to tape out. This presentation will focus on power management methods during the early design phases, when the system and the RTL code are being developed. These phases are widely recognized as presenting the greatest opportunities for affecting power consumption.

Speaker: **Jerry Frenkil** - *Sequence Design, Inc., Santa Clara, CA*

Mentor Graphics Corp.

Reduced Test Routing and Pins while Improving Production Test Quality

Embedded compression for scan test has been broadly accepted in industry to reduce test time, enabling additional production test patterns for higher quality test. Scan implementation in modern IC designs can require thousands of top-level test signal routes. Low pin count test with embedded compression can reduce these top-level routes by over an order of magnitude. We will present embedded compression that supports million gate blocks with only three signals per block while reducing the pattern application time.

Speaker: **Ron Press** - *Mentor Graphics Corp., Wilsonville, OR*

1:00 - 3:00pm

TIMING, NOISE AND SIGNAL INTEGRITY ANALYSIS

Topic Area: Physical Design

Apache Design Solutions, Inc.

Power and Substrate Noise Analysis and Design Optimization for High-Performance Analog and Custom Designs

At advanced nodes, power noise and reliability becomes a challenge for analog/custom circuit designers. Apache's Totem power noise integrity platform can analyze circuits such as CAM with 100's of millions of transistors, or DDR with 10's of GHz of frequency, while preserving Spice-level accuracy. Considering substrate noise injection, propagation, and coupling between analog and digital blocks, allows designers to optimize isolation techniques for their noise-sensitive circuits. Also included are Power/signal EM and IP model generation for SOC integration.

Speaker: **Aveek Sarkar** - *Apache Design Solutions, Inc., San Jose, CA*

Real Intent, Inc.

Unleash the Power of Formal Analysis for CDC Verification

People often think of formal verification as equivalence checking or model checking. Formal techniques can be applied to a wide variety of applications. In this presentation, we will look at the application of formal techniques to clock domain crossing (CDC) verification. Critical design errors can be detected by performing formal analysis on the data and control crossings of the design. Examples will be presented to demonstrate the power of formal techniques for CDC verification.

Speaker: **Jin Zhang** - *Real Intent, Inc., Sunnyvale, CA*

CST of America, Inc.

A Hierarchical Approach for Full-System Signal Integrity and EMC Analysis

A methodology for the signal/power integrity and EMC analysis of full systems including PCBs, attached cables, connectors and enclosures is developed. It consists of hierarchical modeling and block decomposition; an example consisting of a link with multilayer PCBs, attached cables, high speed connectors is provided. Different numerical techniques (FIT, FEM, TLM and PEEC) are employed in order to optimize the simulation speed and the memory requirements. A broadband compact model is also developed to study the radiated emissions due to PCBs inside a metallic enclosure.

Speaker: **Antonio Ciccomancini Scogna** - *CST of America, Inc., Framingham, MA*

3:00 - 5:00pm

VERIFICATION AND DEBUG: RTL, TLM AND FORMAL TECHNIQUES

Topic Area: Verification and Test

Synopsys, Inc.

Increasing Verification Efficiency Using Virtualization and Embedded Software - Synopsys Innovator, DesignWare® System-Level Library, VCS

Recent surveys show that software on embedded processors is often used for verification of the surrounding hardware. As a result, the dynamic of hardware verification is changing. Replacing traditional RTL processor models with transaction-level models (TLM) can increase verification efficiency by simply speeding up the simulation. To debug defects in testbenches for verification, TLM models allow early development of verification scenarios. This presentation will explain the principles of software driven verification which is changing the landscape of hardware verification.

Speaker: **Frank Schirrmeister** - *Synopsys, Inc., Mountain View, CA*

Jasper Design Automation, Inc.

Accelerating Design Reuse with Formal Technology: ActiveDesign™ with Behavioral Indexing™

As STMicroelectronics well understands, design reuse is mandated, especially in this technological and economic climate. But how best to debug and leverage internal legacy design, and commercial IP? Jasper Design's ActiveDesign™ with Behavioral Indexing™ helps visualize and explore design behavior using emerging formal-based technology. Behavioral Indexing iteratively extracts, indexes and stores relevant design behaviors in a dynamic, executable database. STMicroelectronics shares their application experience and results, including design debug automation, quality, productivity, and reuse efficiencies. Three applications are discussed: for new and existing IP, and for commercial IP.

Speakers: **Rajeev Ranjan** - *Jasper Design Automation, Inc., Mountain View, CA*
Raffaele Guarrasi - *STMicroelectronics, Grenoble, France*

Avery Design Systems, Inc.

Achieving Higher Quality Verification at Earlier Design Phases Using Native Symbolic Methodologies

Behavior-level symbolic simulation offers designers robust formal strategies for early RTL design analysis. Reachability analysis applied to design RTL and testbenches finds early design bugs, hard-to-verify code, and testbench limitations of branch code blocks, FSMs, assertions, and cover properties. X-state verification finds non-deterministic RTL design behaviors associated reset and software initialization, lower-power design state transitions, and clock domain crossing, and generates design fixes to correct designs. Coverage test generation improves functional and property coverage by generating boundary case tests from existing behavioral testbenches that elude conventional logic simulation random methods.

Speaker: **Chris Browy** - *Avery Design Systems, Inc., Andover, MA*

Pavilion Panels - Booth #1928

Monday, July 27

9:30 - 10:30am

GARY SMITH ON EDA: TRENDS AND WHAT'S HOT AT DAC

Topic Area: General Interest

Chair: Bob Gardner - *EDA Consortium, San Jose, CA*
Organizer: Gary Smith - *Gary Smith EDA, Santa Clara, CA*

EDAC brings you DAC's traditional kick off: Gary Smith reviews EDA's hottest technology trends. How will the dramatic changes in EDA, the semiconductor market and the design community affect you? What are the hot products that are 'must sees?' Find out here!

Speaker: **Gary Smith** - *Gary Smith EDA, Santa Clara, CA*

10:45 - 11:45am

EDA HERITAGE SERIES: DOUG FAIRBAIRN'S INDUSTRY RETROSPECTIVE

Topic Area: Business

Chair: Vic Kulkarni - *Sequence Design, Inc., Santa Clara, CA*
Organizer: Jim Lipman - *Sidense Corp., Livermore, CA*

Visionary entrepreneur Doug Fairbairn, provides a retrospective talk on major shifts in the electronics industry over the last quarter century and how they have shaped the tools and methodologies of today and tomorrow.

Speaker: **Douglas G. Fairbairn** - *Consultant, San Jose, CA*

1:00 - 2:00pm

HOGAN'S HEROES: THE LONG ROAD TO SYSTEM-LEVEL SIGN-OFF

Topic Area: Business

Chair: Jim Hogan - *Tela Innovation, Inc., Campbell, CA*
Organizer: Jim Hogan - *Tela Innovation, Inc., Campbell, CA*

When was the last time you looked under the hood before buying a car? You care about the cost, performance, features and power, but you don't need to understand the engine to drive it. Shouldn't we take the same approach to system design? System-level IP offers predictability, price, performance and power benefits. Will EDA enable this new level of productivity?

Speakers: **Per Enge** - *Stanford Univ., Stanford, CA*
Grant Pierce - *Sonics, Inc., Milpitas, CA*
Steve Leibson - *EDN Magazine, Santa Clara, CA*

2:30 - 3:15pm

IP AT RISK: PROTECTING THE COMPANY JEWELS

Topic Area: Business

Chair: Jonathon T. Kaplan - *Kaplan IP, Vancouver, WA*
Organizer: Rich Goldman - *Synopsys, Inc., Mountain View, CA*

Your company's most valuable assets can walk out the door at any time, crossing the ether with ease. Your IP is at risk 24/7, as are your customers. Naomi Fine, the acknowledged leader in IP protection, discusses the risks involved and the techniques that you can apply to protect yourself and your company. Don't be a victim of IP theft!

Speaker: **Naomi R. Fine** - *Pro-Tec Data, Los Gatos, CA*

3:30 - 4:30pm

A CONVERSATION WITH THE 2009 MARIE R. PISTILLI AWARD WINNER

Topic Area: General Interest

Chair: Peggy Aycinena - *EDA Confidential, San Mateo, CA*
Organizer: Sabina Burns - *Virage Logic Corp., Fremont, CA*

Join **Telle Whitney,** the 2009 Marie R. Pistilli Award Winner, in a one-on-one conversation with EDA Confidential's Peggy Aycinena. As always, the conversation promises to be lively and wide-ranging, with ample opportunity for audience participation in a discussion that spans both gender and generational issues.

5:00 - 6:00pm

DAC/ISSCC STUDENT DESIGN CONTEST AWARDS PRESENTATION

Topic Area: General Interest

Chair: Byunghoo Jung - *Purdue Univ., West Lafayette, IN*
Organizers: Byunghoo Jung - *Purdue Univ., West Lafayette, IN*
Bill Bowhill - *Intel Corp., Hudson, MA*

Presentation of the nine student design award winners, across operational, system-level and conceptual award categories of the Student Design Contest, organized by the Design Automation Conference and the International Solid-State Circuits Conference (ISSCC).

View the nine winners: http://www.dac.com/46th/studcon.html

Tuesday, July 28

10:30 - 11:15am

FIGHTING PIRACY ON THE HIGH SEAS: OFFENSE VS. DEFENSE

Topic Area: Business

Chair: Scott Baeder - *Cadence Design Systems, Inc., Chelmsford, MA*
Organizers: Craig Rawlings - *Certicom Corp., Reston, VA*
Scott Baeder - *Cadence Design Systems, Inc., Chelmsford, MA*

Not all pirates are off the coast of Somalia. Not all anti-piracy techniques are appropriate in all situations. Sometimes hardening IP works best. Other times "business intelligence" can be used to convert pirates' clients into your paying customers. Anti-piracy techniques can be applied to design software, to embedded software, or even to physical chips. Learn what's best to protect your treasure.

Speakers: **Bill Latin** - *Certicom Corp., Mississauga, ON, Canada*
Vic Demarines - *V.i. Labs, Inc., Waltham, MA*

11:30am - 12:15pm

LOW-POWER: CONSUMER ELECTRONICS' CATCH-22

Topic Area: Business

Chair: Paul Dempsy - *EDA Tech Forum, Falls Church, VA*
Organizer: Brenda Westcott - *Virage Logic Corp., Fremont, CA*

Digital mobile devices drive significant semiconductor content. These devices increasingly stress the low-power requirements for longer battery life. However, low-power conflicts with consumer electronics' traditional requirement: low-cost, driving packaging and thermal requirements. The panelists debate where in the design chain trade-offs can be made.

Speakers: **Ana Hunter** - *Samsung, San Jose, CA*
Brani Buric - *Virage Logic Corp., Fremont, CA*
Gary Delp - *LSI Corp., Rochester, MN*

1:00 - 2:00pm

TOWN HALL MEETING: CAN WE AFFORD FOR START-UPS TO WIND DOWN?

Topic Area: Business

Chair: Lucio Lanza - *Lanza Tech Ventures, Palo Alto, CA*
Organizer: Lucio Lanza - *Lanza Tech Ventures, Palo Alto, CA*

The economic crisis has strangled investment for semiconductor start-ups. Lack of industry growth and IPOs, rising design costs, and alternative investment opportunities have all served to starve these engines of innovation. Given the impact of the crisis on the start-up model, this panel will consider the resulting long-term health of the semiconductor industry.

Speakers: **Shishpal Rawat** - *Intel Capital, Santa Clara, CA*
Gunjeet Baweja - *Needham & Company, LLC, Menlo Park, CA*
Sanjay Srivastava - *Denali Software, Inc., Sunnyvale, CA*

2:30 - 3:15pm

WILL INTEROPERABLE PDKS FLY IN A STODGY ANALOG WORLD?

Topic Area: Analog/Mixed-Signal/RF Design

Chair: Mike Santarini - *Xilinx, Inc., San Jose, CA*
Organizer: Jingwen Yuan - *Synopsys, Inc., Mountain View, CA*

Most everyone agrees, standardized PDKs are needed to reduce foundry workload and increase productivity. PDKs are the essential link between designers and foundries defining custom design data interchange. Will the analog world embrace the interoperable PDK? What is the true benefit and cost to the analog designer?

Speakers: **Ed Lechner** - *Synopsys, Inc., Mountain View, CA*
Bill Heiser - *Cadence Design Systems, Inc., San Jose, CA*
Tom Quan - *Taiwan Semiconductor Manufacturing Co., Ltd., San Jose, CA*

3:30 - 4:15pm

EMBEDDED MULTICORE: MULTI-OPPORTUNITIES, MULTI-CHALLENGES

Topic Area: System-Level and Embedded

Chair: Markus Levy - *The Embedded Microprocessor Benchmark Consortium, Sacramento, CA*
Organizer: Leslie Cummings - *Skye Marketing Communications, Portland, OR*

Multicore processors are pervasive throughout desktop applications, regardless of their inherent programmability challenges. Now these processors are emerging in high-performance embedded SOCs, an environment with far greater design constraints, driving optimal programming requirements. This panel addresses the opportunity for success for these advanced devices. Are they the catalyst for change between HW and SW team processes?

Speakers: **Max Domeika** - *Intel Corp., Hillsboro, OR*
John Goodacre - *ARM Ltd., Cambridge, United Kingdom*
Pierre Paulin - *STMicroelectronics, Toronto, ON, Canada*

Pavilion Panels - Booth #1928

Tuesday, July 28

4:30 - 5:15pm

EDA ECOSYSTEM: IN SYNC OR OUT OF TOUCH?

Topic Area: General Interest

Chair: Gabe Moretti - *Gabe on EDA, Venice, FL*
Organizer: Gabe Moretti - *Gabe on EDA, Venice, FL*

Have traditional design tools and methodologies kept pace with the needs of designers? Hear what leading Fabless, IDM and FPGA executives have to tell their EDA, IP, foundry and design services partners about their technology and economic challenges and the need to stay in sync for mutual success.

Speakers: **Moshe Gavrielov** - *Xilinx, Inc., San Jose, CA*
Shrenik Mehta - *Sun Microsystems, Inc., Santa Clara, CA*
Marquette Anderson - *Texas Instruments, Inc., Nice, France*

Wednesday, July 29

10:00 - 10:45am

POWER SCAVENGING: WANT NOT, WASTE NOT

Topic Area: Business

Chair: John Blyler, Editor, Chip Design Magazine
Organizer: Yatin Trivedi - *Synopsys, Inc., Mountain View, CA*

Everyone talks about low-power designs, long battery life and the environmental effects of so much power consumption. However, the consumption of power is an ever-increasing need that must be faced. Are there alternatives to generating "small" amounts of power for low-power gadgets from really unconventional methods? Let the experts tell you where some of the hidden power is available and how they are harnessing it for some of the most complex applications.

Speakers: **Sandeep Kundu** - *Univ. of Massachusetts, Amherst, Amherst, MA*
Steve Grady - *Cymbet Corp., Elk River, MN*
Mark Buccini - *Texas Instruments, Inc., Dallas, TX*

12:30 - 1:30pm

ELECTRONICS GOING GREEN: FUTURE OR FUTILE?

Topic Area: Green Technology

Chair: Carl Guardino - *Silicon Valley Leadership Group, Milpitas, CA*
Organizers: Sabina Burns - *Virage Logic Corp., Fremont, CA*
Tiffany Sparks - *Chartered Semiconductor Manufacturing, Milpitas, CA*

Green is in. Companies promote building energy efficient products, using greener materials and doing their part to recycle. Despite the "go green" rhetoric, the electronics industry still relies heavily on toxic chemicals in manufacturing, and significant power outlays for end products. This panel discusses whether the electronics industry is truly making a difference, and what more can be done.

Speakers: **Lori Duvall** - *Sun Microsystems, Inc., Santa Clara, CA*
Parker Brugge - *Consumer Electronics Association, Washington DC*
Bruce S. Klafter - *Applied Materials, Inc., Santa Clara, CA*

2:00 - 2:45pm

SEEKING THE HOLY GRAIL OF VERIFICATION COVERAGE CLOSURE

Topic Area: Verification and Test

Chair: Brian Bailey - *Consultant, Portland, OR*
Organizer: Gloria Nichols - *Launch Marketing, Half Moon Bay, CA*

The promise of total verification coverage closure is one of EDA's holy grails. A range of technologies provide alternative approaches to meet this evolving and elusive goal. Which solutions will eventually lead to the ultimate verification coverage prize? Leading verification experts debate the best approach. Will random test generation continue to prevail, or is it time for something new?

Speakers: **Jim Sullivan** - *Qualcomm, Inc., Cary, NC*
Jon Michelson - *Cisco Systems, Inc., San Jose, CA*
David Bural - *Texas Instruments, Inc., Dallas, TX*
JL Gray - *Verilab, Inc., Austin, TX*

Wednesday, July 29

3:00 - 3:45pm

THE AMS REVIVAL: BIPOLAR THINKING?

Topic Area: Analog/Mixed-Signal/RF Design

Chair: Dave Maliniak - *EDN Magazine, New York, NY*
Organizers: Jim Lochmiller - *OSCI, Windsor, CA*
Jill Jacobs - *MOD Marketing and Events LLC., San Jose, CA*

Analog and Systems. Is it bipolar thinking? Experts from semiconductor, EDA and ESL debate the essentials of mixed-signal/software codesign and what is needed in ESL to bring AMS on-board. They will discuss bridging the gap between AMS and digital design, improving AMS designer productivity, design methodologies, and AMS features in HDLs and SystemC.

Speakers: **Christoph Grimm** - *Technische Univ. Wien, Vienna, Austria*
Mike Woodward - *The MathWorks, Inc., Natick, MA*
David Smith - *Synopsys, Inc., Hillsboro, OR*

4:00 - 5:00pm

TWEET, BLOG OR NEWS: HOW DO I STAY CURRENT?

Topic Area: Bausiness

Chair: Michael Sanie - *Maestro International, Menlo Park, CA*
Organizers: Sabina Burns - *Virage Logic Corp., Fremont, CA*
Jim Lipman - *Sidense Corp., Livermore, CA*

Traditional print and online publications are quickly becoming less prominent while blogs, portals and social media networks are springing up all around. Experts tell you how to successfully navigate through this new maze to ensure you are getting what you need – both news and in-depth technology – to stay current in an increasingly competitive global market.

Speakers: **Sean Murphy** - *SK Murphy, San Jose, CA*
Ron Wilson - *EDN Magazine, San Jose, CA*
John Busco - *NVIDIA Corp., Santa Clara, CA*

5:15 - 6:00pm

REUSE IN AN ENTERPRISE: MYTH OR REALITY?

Topic Area: Business

Chair: Warren Savage - *IPextreme, Campbell, CA*
Organizers: Gabriele Saucier - *Design and Reuse, Grenoble, France*
David Yoon - *Cisco Systems, Inc., San Jose, CA*

Collaboration and knowledge sharing are critical for many reasons, including design team decentralization and the use of third-party IP. An important facet of this collaboration need is IP reuse at the enterprise level. This panel discusses companies that have tried IP reuse, and analyzes their successes and failures.

Speakers: **David Yoon** - *Cisco Systems, Inc., San Jose, CA*
Gabriele Saucier - *Design and Reuse, Grenoble, France*
Bryan Jones - *Intel Corp., Santa Clara, CA*

Thursday, July 30

10:00 - 10:45am

YOU DON'T KNOW JACK - HIGH SCHOOLERS TELL YOU WHAT'S UP WITH TECHNOLOGY

Topic Area: New and Emerging Technologies

Chair: Kathryn Kranen - *Jasper Design Automation, Inc., Mountain View, CA*
Organizer: Gary Robinson - *Synopsys, Inc., San Rafael, CA*

You think you know what features are cool? You don't, but our high schoolers do. Today's and tomorrow's consumers are high school and college students, and they think very differently from you. You'll be shocked as they tell you how they use your technology in ways you never imagined and put you on the path to the next killer app.

Panelists: **Ritik Malhotra** - *Lynbrook High School, San Jose, CA*
Michael Chang - *Santa Teresa High School, San Jose, CA*
Tony Ho - *Lynbrook High School, San Jose, CA*

Tutorials

Registration Fees:

TUTORIALS	Member, ACM or IEEE	Non-Member	Student
Full-Day Tutorials	$300 (per tutorial)	$400 (per tutorial)	$200 (per tutorial)

Earn Continuing Education Credit towards Professional Certification while attending the 46th DAC Tutorials! http://www.dac.com/46th/tut_credit.html

Rm: 133

TUTORIAL #1: LOW-POWER SOC DESIGN: STATE OF THE ART AND DIRECTIONS

Topic Area: Low-Power Design

Monday - July 27, 8:30am - 4:30pm

Organizer: Pascal Urard - *STMicroelectronics, Crolles, France*

Energy efficiency is the key metric in a new generation of products. Many design techniques co-exist to reduce dynamic power and leakage in large systems-on-chip (SOCs). Deciding which techniques to use early in the design process and how to integrate them in an existing design flow is a major challenge.

This tutorial begins by presenting state of the art techniques to achieve improved energy efficiency, particularly aggressive scaling of the power supply. Advantages and tradeoffs of these techniques are described in detail, setting the stage for the remainder of the tutorial, which focuses on industry case studies.

The second part of the tutorial discusses practical challenges such as early power estimation at architectural level, power verification along the design flow, timing characterization when using dynamic voltage/frequency scaling (DVFS), and power gating with retentive sequential elements.

Finally, designers from two major silicon providers serving the cell phone market will share industrial case studies realized in 45nm technology. The first case study focuses on tradeoffs and verification techniques when implementing power islands, body bias, and power gating. The second case study explains various power reduction techniques used in a typical 45nm SOC, and points out limitations of existing tools that need to be overcome to meet the requirements of next technology node products.

Attendees of this tutorial will walk away with in-depth practical knowledge of modern low-power SOC design flows, both their limitations and capabilities, as well as insight on where tomorrow's power challenges lie.

Speakers: **Kaushik Roy** - *Purdue Univ., West Lafayette, IN*
Michael Keating - *Synopsys, Inc., Mountain View, CA*
Bernard Ramanadin - *ST-Ericsson, Crolles, France*
Matt Severson - *Qualcomm CDMA Technologies, Inc., San Diego, CA*

Continental Breakfast: 7:30am, Rm: 134
Lunch: 11:30am - 1:30pm, Rm: 134

Rm: 132

TUTORIAL #2: HIGH-LEVEL SYNTHESIS FOR ESL DESIGN: FUNDAMENTALS AND CASE STUDIES

Topic Area: System-Level and Embedded

Monday - July 27, 8:30am - 4:30pm

Organizer: Philippe Coussy - *Univ. de Bretagne, Lorient, France*

Actual digital systems need new ESL tools in order to raise the specification abstraction level. High-Level Synthesis (HLS) starts from algorithmic specifications that focus on functionality rather than on the cycle accurate implementation that is used in Register Transfer Level (RTL) specifications. HLS tools thus allow designers to rapidly generate complex RTL hardware architectures that are optimized to various performance, area and power requirements. HLS offers the prospect of improving the productivity and quality of digital systems development. Designing at higher levels of abstraction allows one to better cope with the system design complexity, to verify earlier in the design process, and to increase code reuse.

This tutorial will provide a comprehensive introduction to the use of High-Level Synthesis. Basic definitions, key concepts, typical design flows, and design constraints will be first described. Next, case studies using High-Level Synthesis will be presented. The tutorial will examine the use and impact of High-Level Synthesis on the design process, from conception through implementation. It will provide guidance and insight on how this can be achieved in practice. The aim is for attendees to learn about High-Level Synthesis techniques they can use immediately and to give a view of the direction the industry is taking for the longer term.

Speakers: **Daniel Gajski** - *Univ. of California, Irvine, CA*
Jason Cong - *Univ. of California, Los Angeles, CA*
Nitin Chawla - *STMicroelectronics, Greater Noida, India*
Sumio Morioka - *NEC Corp., Kawasaki, Japan*
Rodric Rabbah - *IBM Corp., Hawthorne, NY*
Scott Mahlke - *Univ. of Michigan, Ann Arbor, MI*

Continental Breakfast: 7:30am, Rm: 134
Lunch: 11:30am - 1:30pm, Rm: 134

Rm: 131

TUTORIAL #3: POST-SILICON VALIDATION AND RUNTIME VERIFICATION: ENSURING CORRECTNESS AFTER FIRST SILICON

Topic Area: Verification and Test

Friday - July 31, 9:00am - 5:00pm

Organizer: Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

Modern processor designs are extremely complex and difficult to validate during development, causing a growing portion of the verification effort to shift to the post-silicon phase, after the first few silicon prototypes become available. While post-silicon validation benefits from extremely high execution performance compared to pre-silicon simulation, significant drawbacks are posed by the limited controllability and observability of internal circuit nodes.

Moreover, even after extensive verification and validation in pre- and post-silicon, today's verification approaches are incapable of completely validating a microprocessor before its release to the public. While the past few decades have witnessed significant efforts to improve verification methodology for hardware systems, these efforts have been far outstripped by the massive complexity of modern digital designs, leading to product releases for which an always smaller fraction of system's states has been verified. The result is that escaped bugs are part of the reality of every processor design.

This tutorial addresses state of the art methods for detecting and correcting bugs after the first few silicon prototypes of a design become available, spanning both i) techniques and methodologies for in-lab post-silicon validation and ii) runtime verification solutions, that is, those deployed directly in silicon monitoring a system's operation at runtime, after it becomes commercially available, and throughout its entire lifespan, detecting and correcting functional errors.

This tutorial is intended for microprocessor architects and designers, verification engineers, and CAD professionals interested in a better understanding of current post-silicon validation technologies. It will also benefit designers and verification experts in providing an overview of runtime verification solutions that have recently been proposed by the research community.

Speakers: **Valeria Bertacco** - *Univ. of Michigan, Ann Arbor, MI*
Rand Gray - *Intel Corp., Hillsboro, OR*
Jai Kumar - *Sun Microsystems, Inc., Santa Clara, CA*
Albert Meixner - *NVIDIA Corp., Santa Clara, CA*
Bart Vermeulen - *NXP Semiconductors, Eindhoven, The Netherlands*

Continental Breakfast: 7:30am, Rm: 134
Lunch: 11:30am - 1:30pm, Rm: 134

Tutorials

Registration Fees:

TUTORIALS	Member, ACM or IEEE	Non-Member	Student
Full-Day Tutorials	$300 (per tutorial)	$400 (per tutorial)	$200 (per tutorial)

Rm: 130

TUTORIAL #4: CAD: UTILIZING THE STATE OF THE ART, AND BEYOND, IN PARALLEL PROGRAMMING

Topic Area: Synthesis and FPGA

Friday - July 31, 9:00am - 5:00pm

Organizer: Kurt Keutzer - *Univ. of California, Berkeley, CA*

With mainstream computers offering multicore processors and General-Purpose Graphics Processing Units (GPGPUs) offering manycore processors, economical parallelism is now coming to your desktop. All performance hungry applications will benefit by harnessing the power of these processors. This day long tutorial will first introduce attendees to the state of the art in parallel programming: a number of the most commonly used languages will be introduced including pThreads, OpenMP, Thread-Building Blocks, and MPI. This will be followed by an overview of the state of the art in applying these technologies to CAD.

Given the magnitude of the market at stake, the state of the art in parallel programming is rapidly changing. The second half of the tutorial will outline developments that are more at the frontier of parallel programming and will particularly discuss the challenges of fine grained processors. In particular, new programming languages that support more fine-grained manycore parallelism such as CUDA and OpenCL will be described. This part of the tutorial will also describe a new generation of fine-grained processors and a disciplined approach to architecting fine-grained parallel software that runs on them. Finally, the tutorial will end with a demonstration of how fine-grained parallelism can be applied to computer-aided design.

Speakers: **Kurt Keutzer** - *Univ. of California, Berkeley, CA*
Tim Mattson - *Intel Corp., DuPont, WA*
Tom Spyrou - *Cadence Design Systems, Inc., San Jose, CA*
Michael Wrinn - *Intel Corp., Hillsboro, OR*

Continental Breakfast: 7:30am, Rm: 134
Lunch: 11:30am - 1:30pm, Rm: 134

Rm: 132

TUTORIAL #5: FROM NANODEVICES TO NANOSYSTEMS: PROMISES AND CHALLENGES OF IC DESIGN WITH NANOMATERIALS

Topic Area: New and Emerging Technologies

Friday - July 31, 9:00am - 5:00pm

Organizers: André DeHon - *Univ. of Pennsylvania, Philadelphia, PA*
Deming Chen - *Univ. of Illinois, Urbana-Champaign, Urbana, IL*

Nanomaterials, for example, those formed from chemically synthesized nanoscale building blocks (e.g., CNTs, Graphene, catalyst-grown nanowires) or from atomically engineered spintronic and oxide heterostructures, have the potential to revolutionize microelectronic systems by the introduction of improved device properties, novel device characteristics, or new fabrication techniques.

Speakers: **Yong Chen** - *Univ. of California, Los Angeles, CA*
André DeHon - *Univ. of Pennsylvania, Philadelphia, PA*
Stuart Parkin - *IBM Corp., San Jose, CA*
Subhasish Mitra - *Stanford Univ., Stanford, CA*
Deming Chen - *Univ. of Illinois, Urbana-Champaign, Urbana, IL*

Continental Breakfast: 7:30am, Rm: 134
Lunch: 11:30am - 1:30pm, Rm: 134

However, some important questions can be asked:

1. What are the fundamental principles of building nanodevices with nanomaterials?
2. Why do these nanodevices have the potential to scale beyond the perceived scaling limitations of traditional CMOS?
3. How much impact could these nanodevices have on future system integration, density, and performance?
4. What are the challenges and solutions with respect to circuit/system-level fabrication and CAD?

To answer these questions, this tutorial focuses on the following themes:

Theme 1: Introduction of nanoscale device and component-level modeling and manufacturing.

Theme 2: Presentation of major existing nanosystems design principles and promises.

Theme 3: Identification of key challenges and solutions to bridging the gap between nanodevice research and nanosystem building.

Theme 4: Insights for future nanoscale device/system research.

Rm: 133

TUTORIAL #6: FUNCTIONAL VERIFICATION PLANNING AND MANAGEMENT: NAVIGATING FROM SPECIFICATION TO FUNCTIONAL CLOSURE

Topic Area: Verification and Test

Friday - July 31, 9:00am - 5:00pm

Organizer: Andrew Piziali - *Consultant, Parker, TX*

The increasing complexity of hardware designs, coupled with time-to-market pressures and the high cost of bug escapes, mean that ad-hoc methods for verification planning and execution are no longer adequate.

This tutorial teaches state of the art methods for planning, monitoring and assessing verification progress, each essential for predictable, successful verification. Quantifying the scope of the verification problem, specifying its solution and measuring verification progress against this plan dramatically reduces schedule uncertainty and provides an adaptive framework for accommodating design and schedule changes. This planning process provides the information necessary to predict the state of the verification process for risk analysis and management, preventing late schedule and quality surprises.

Good planning, monitoring and assessment of the verification process begins with a verification plan that captures the features of the design, along with scheduling and resource constraints. It must include a description of the means to measure verification progress, such as coverage, simulation jobs and cycles, failures and bugs. The verification plan must also be executable, making progress metrics visible in the context of the verification plan and serving as a design-specific verification user interface. Finally, the plan must also specify the verification techniques to be applied to solve each verification problem, such as simulation, assertions and formal analysis.This tutorial discusses how to choose design features that are candidates for verification using each of these techniques so that the overall verification labor is minimized while verification completeness is maximized. The tutorial will cover all of these aspects using real-life examples.

Speakers: **Andrew Piziali** - *Consultant, Parker, TX*
Avi Ziv - *IBM Corp., Haifa, Israel*
Janick Bergeron - *Synopsys, Inc., Ottawa, ON, Canada*

Continental Breakfast: 7:30am, Rm: 134
Lunch: 11:30am - 1:30pm, Rm: 134

Rm: 303-305

CEDA: FRONTIERS IN RESEARCH AND EDUCATION IN COMPUTING: A VIEW FROM THE NATIONAL SCIENCE EOUNDATION

Topic Area: New and Emerging Technologies

Tuesday, July 28, 12:00 - 2:00pm

Organizer: Shishpal Rawat - *Intel Corp., Folsom, CA*

Jeannette M. Wing - *Assistant Director of Computer and Information Science and Engineering Directorate, National Science Foundation, Washington D.C. and President's Professor of Computer Science Computer Science Dept., Carnegie Mellon Univ., Pittsburgh, PA*

The NSF Computer and Information Science and Engineering Directorate funds 84% of all academic computer science research in the United States. Dr. Wing will present highlights of CISE's research and education programs, including current interests in cyber-enabled discovery and innovation, cyber-physical systems, data-intensive computing, network science and engineering, socially intelligent computing, trustworthy computing, and future interests in Green IT and computational economics. Dr. Wing will also put NSF's investments in computing within the broader national and international context.

Speaker: **Jeannette M. Wing** - *National Science Foundation, Washington DC*

Lunch is available to the first 200 attendees. There will be additional seating available.

Rm: 134

12TH ANNUAL SIGDA PH.D. FORUM / MEMBER MEETING

Topic Area: General Interest

Tuesday, July 28, 6:00 - 7:30pm

Organizer: Elaheh Bozorgzaheh - *Univ. of California, Irvine, CA*

SIGDA invites you to attend our 12th annual Ph.D. Forum and Member Meeting at DAC 2009. SIGDA members are invited, as are all members of the EDA Community. We will begin with an overview of SIGDA programs including newly created programs, followed by the presentation of this year's ACM/SIGDA Awards. However, the main focus of the meeting will be the Ph.D. Forum. Aimed at strengthening ties between academia and industry, students will present posters and discuss their Ph.D. dissertation research with interested attendees. The Ph.D. Forum gives students feedback on their research, and gives the EDA community a preview of work in progress. Light refreshments will be served.

For more information: http://www.sidga.org/daforum

Rm: 123

MULTIPROCESSOR SYSTEM-ON-CHIP: CURRENT TRENDS AND THE FUTURE

Topic Area: System-Level and Embedded

Sunday - July 26, 8:00am - 5:00pm

Organizers: Juergen Becker - *Univ. Karlsruhe, Karlsruhe, Germany*
Michael Huebner - *Univ. Karlsruhe, Karlsruhe, Germany*

Registration: $150 (Member), $195 (Non-Member)

For the next decade, Moore's Law is still going to bring higher transistor densities allowing billions of transistors to be integrated on a single chip. However, it became obvious that exploiting significant amounts of instruction-level parallelism with deeper pipelines and more aggressive wide-issue superscalar techniques, and using most of the transistor budget for large on-chip caches has come to an dead end. Scaling performance with higher clock frequencies, especially, is getting more and more difficult because of heat dissipation problems and high energy consumption that is too high. The latter is not only a technical problem for mobile systems, but is also becoming a severe problem for computing centers because high energy consumption leads to significant cost factors in the budget. Improving performance can only be achieved by exploiting parallelism on all system levels.

Multicore architectures offer a better performance/Watt ratio than single-core architectures with similar performance. Combining multicore and co-processor technology promise extreme computing power for highly CPU-time-consuming applications. FPGA-based accelerators especially offer the opportunity to speedup an application by implementing their compute-intensive kernels into hardware, but also adapt to the dynamical behavior of an application.

The purpose of this workshop is to evaluate strategies for future system design in MPSOC architectures. Both hardware design and tool-integration into existing development tools will be discussed. Novel trends in MPSOC combined with reconfigurable architectures are a main topic in this workshop. The main emphasis is on architectures, design-flow, tool-development, applications and system design.

Speakers: **Kees Goossens** - *NXP Semiconductors, Eindhoven, The Netherlands*
Rob Aitken - *ARM Ltd., Sunnyvale, CA*
Diana Goehringer - *FOM, Ettlingen, Germany*
Ricardo Reis - *Federal Univ. of Rio Grande do Sul, Porto Alegre, Brazil*
Kurt Keutzer - *Univ. of California, Berkeley, CA*
Kees Vissers - *Xilinx, Inc., San Jose, CA*
Andreas Herkersdorf - *Technische Univ. München, Munich, Germany*
Marcello Coppola - *STMicroelectronics, Grenoble, France*
Dac Pham - *Freescale Semiconductor, Inc., Austin, TX*

Lunch: 12:10pm, Rm: 134

Rm: 132

6TH UML - SOC AT THE 46TH DAC

Topic Area: System-Level and Embedded

Sunday - July 26, 9:00am - 5:00pm

Organizers: John Wolfe - *Mentor Graphics Corp., Tucson, AZ*
Wolfgang Mueller - *Paderborn Univ., Paderborn, Germany*
Yves Vanderperren - *Katholieke Univ. Leuven, Leuven, Belgium*

Registration: $250 (Member), $295 (Non-Member)

The purpose of the 6th UML-SOC workshop is to educate, provide experience, and facilitate the exchange of ideas between the participants. We will provide an introduction to executable UML and its application to electronic system design, with the support of the concrete case study of a typical embedded system. Starting from a high-level natural-language specification, the participants will model the application with UML, execute the resulting models, locate and repair defects, and then verify that the application meets the requirements. Dedicated attention will be given to interactive discussions at regular intervals during the workshop, a feature which will distinguish the event from hands-on tutorials.

No previous experience with UML, programming, or logic design is required. For practical convenience and teaching purposes, the workshop will utilize the BridgePoint® tools from Mentor Graphics Corp. Specifically, BridgePoint Builder will be employed for the construction of UML models, and BridgePoint Verifier will provide the execution and debugging environment for the models.

Speaker: **Cortland Starrett** - *Mentor Graphics Corp., Brookston, IN*

Lunch: 11:30am - 1:30pm, Rm: 134

Rm: 131

MOVING FROM TRADITIONAL TO EQUATION-BASED DRC

Topic Area: DFM and the Manufacturing Interface

Sunday - July 26, 2:00 - 5:30pm

Organizer: Gene Forte - *Mentor Graphics Corp., Wilsonville, OR*

Registration: $80 (Member), $110 (Non-Member)

The number and complexity of design rule checks is growing dramatically due to increasing manufacturing variability at advanced nodes, and increasing sensitivity of manufacturing to a variety of design features. As a result, simple physical verification has evolved into hard-core process simulation and analysis for such issues as lithography and CMP characterization. Unfortunately, the cost and compute intensity of simulation make this approach too expensive and time consuming to use early in the design process. In addition, simulators only exist for a specific set of well-defined process issues.

This workshop demonstrates how a new approach, called equation based DRC (eqDRC), combines the runtime and integration advantages of traditional DRC with multi-dimensional mathematical modeling. This approach opens the door to a wide array of advanced design rule checks and DFM analyses involving complex geometric interactions. We will walk attendees through multiple examples, in production today, of how eqDRC can be used to solve advanced nanometer layout challenges. IBM Corp. and Freescale Semiconductor, Inc. will discuss how they have utilized this functionality to build a variety of solutions in both the DRC and DFM space. The workshop will conclude with an interactive panel discussion on physical verification challenges and the use of eqDRC and other advanced techniques.

Speakers: **Jim Culp** - *IBM Corp., East Fishkill, NY*
Robert Boone - *Freescale Semiconductor, Inc., Austin, TX*
David Abercrombie, John Ferguson - *Mentor Graphics Corp., Wilsonville, OR*

Workshops

Rm: 133

MEETING THE CHALLENGES OF ESD/ERC IN A MIXED-SIGNAL WORLD

Topic Area: Physical Design

Sunday - July 26, 2:00 - 5:30pm

Organizer: Gene Forte - *Mentor Graphics Corp., Wilsonville, OR*

Registration: $80 (Member) $110 (Non-Member)

Designers of advanced ICs increasingly need to perform various electrical checks based on a separate set of electrical design rules (ERC) that are distinct from traditional physical design rules. An important application of ERC is verifying that electrostatic discharge (ESD) protection circuits are in place wherever the device is vulnerable, whether those circuits are included in the schematic and netlist or not. Robust ERC reduces the number of die susceptible to catastrophic electrical failures during final testing, as well as premature failures in the field.

This workshop will demonstrate how to use Programmable Electrical Rule Checking (PERC) technology to automate electrical rule checking and to rapidly find and correct ERC violations in a design. Designers working on submicron, mixed-signal, or low-power devices used in mobile and other leading-edge applications will find this workshop extremely valuable. The workshop will conclude with an interactive panel discussion on ERC challenges and the use of PERC and other advanced techniques.

Speakers: **Scott Service** - *DSP Group, Minneapolis, MN*
Pieter Donck - *Sarnoff Corp., Gistel, Belgium*
Michael Khazhinsky - *Freescale Semiconductor, Inc., Austin, TX*
Hazem Hegazy - *Mentor Graphics Corp., Cairo, Egypt*

Rm: 300

MARKETING OF TECHNOLOGY – THE LAST CRITICAL STEP

Topic Area: Business

Sunday - July 26, 1:30 - 4:30pm

Organizers: Chuck Byers - *Managing Director, Business Practicum, Gilroy, CA*
Michael Sanie - *Managing Director, Maestro International, San Jose, CA*

Registration: $80 (Member) $110 (Non-Member)

"Marketing of Technology – The Last Critical" speaks directly to the technically trained professional charged with formulating the go-to-market strategy and plans for the company's next big product.

The workshop will cover marketing's "4Ps" from a semiconductor perspective and will provide hands-on tools for developing product positioning and message platforms that drive product differentiations product revenue and enhanced product margins and the communications tools needed to communicate the value of innovation to technical markets. Special emphasis will be placed on new Web 2.0 tools to drive marketing success.

Has an afternoon coffee break.

Rm: 124

INTERNATIONAL WORKSHOP ON BIO-DESIGN AUTOMATION

Topic Area: New and Emerging Technologies

Monday - July 27, 8:00am - 6:00pm

Organizers: Douglas Densmore - *Univ. of California, Berkeley, CA*
Marc Riedel - *Univ. of Minnesota, Minneapolis, MN*
Soha Hassoun - *Tufts Univ., Medford, MA*
Ion Mandoiu - *Univ. of Connecticut, Storrs, CT*

Registration: $150 (Member), $195 (Non-Member)

The International Workshop on Bio-Design Automation (IWBDA) will bring together researchers from the synthetic biology and electronic design automation communities. The broad focus will be on concepts, methodologies and software tools for the automated synthesis of novel biological functions. A specific focus will be on the application of computational expertise from electronic circuit design to these areas.

Still in its early stages, the field of synthetic biology has been driven by experimental expertise; much of its success has been attributable to the skill of the researchers in specific domains of biology. There has been a concerted effort to assemble repositories of standardized components. However, creating and integrating synthetic components remains an ad hoc process. The field has now reached a stage where it calls for computer-aided design tools. The electronic design automation (EDA) community has unique expertise to contribute to this endeavor. This workshop offers a forum for cross-disciplinary discussion, with the aim of seeding collaboration between the research communities.

Some specific areas of interest are:

- Design methodologies for synthetic biology
- Standardization of biological components
- Automated assembly techniques
- Computer-aided modeling and abstraction techniques
- Engineering methods inspired by biology

Speakers: **Drew Endy** - *Stanford Univ., Stanford, CA*
Ron Weiss - *Princeton Univ., Princeton, NJ*

Lunch: 12:00 - 1:30pm, Rm: 125

Rm: 123

YOUNG FACULTY WORKSHOP

Topic Area: General Interest

Monday - July 27, 9:00am - 5:00pm

Organizers: Steven P. Levitan - *Univ. of Pittsburgh, Pittsburgh, PA*
Soha Hassoun - *Tufts Univ., Medford, MA*

Registration: $150 (Member), $195 (Non-Member)

The Design Automation Conference will be hosting a workshop for new and soon-to-be faculty in the field of electronic design automation (EDA) at DAC 2009 in San Francisco.

This one day workshop for young faculty and people planning to enter academia (both senior graduate students and researchers from industry) will be on topics of relevance to surviving and succeeding as a faculty member in the current academic/research climate. The workshop will be open for all pre-tenure faculty and senior graduate students in CAD, Electronic Systems Design, and related areas.

The full day workshop will be organized into six sessions, with each session led by one or two senior faculty, researchers, or representatives from funding agencies. Topics covered include establishing a research career, the art of teaching an EDA course, seeking tenure, balancing career and life components, and diversity in academia. Each of these sessions will run one hour with time allocated for Q&A and open discussions. There will be an opportunity during lunch and at the end of the day for representatives of NSF, SRC and industry researchers to meet with the attendees.

Supported by:

Rm: 131

WORKSHOP FOR WOMEN IN DESIGN AUTOMATION (WWINDA): CAREER CROSSROADS - WHO HAS THE MAP?

Topic Area: General Interest

Monday - July 27, 9:00am - 1:45pm

Registration: $75 (Member), $100 (Non-Member)

A time comes in your career when you arrive at a crossroads with a decision to make. Do you continue to climb the technical ladder or do you move over to the management track? There is no right answer, though there are certainly pros and cons to each choice. These choices are even more complex in today's economy – how do you make the right choice for you while navigating the uncertain economic climate? A recent study conducted by the Anita Borg Institute for Women and Technology in conjunction with the Michelle R. Clayman Institute for Gender Research at Stanford University finds that real barriers to advancement do exist for women in technical careers. Who, then, has the map when career crossroads are reached?

Mission Statement

To be a workshop of relevance to women in Electronic Design Automation (EDA), by providing a forum for the exchange of ideas for successful careers in the EDA profession, to address the particular needs of professional women and to provide an opportunity for peer networking.

2009 WWINDA Chair: Karla Reynolds

2009 WWINDA Steering Committee:

Peggy Aycinena - *Editor, EDA Confidential*
Nanette V. Collins - *Publicity Chair, 46th DAC*
Marie R. Pistilli - *Co-Chair, Board of Directors, MP Associates, Inc.*

Keynote Address: **Telle Whitney** - *President and CEO, Anita Borg Institute*

Dr. Whitney will present results of the ABI research that takes an in-depth look into the barriers to retention and advancement of technical women in mid-level career positions. Based on the findings, the study provides solid recommendations to employees in high-tech companies on how to overcome these barriers.

Panel Discussion

Panel Moderator: Mar Hershenson - *Magma Design Automation, Inc.*

Panelists, knowing the realities documented by the ABI study, and drawing on their own career and workplace experiences, will explore what you can do to prepare and overcome obstacles when making important career decisions. Each will address:

- Career barriers they encountered and how they got around them
- How they made the decision on where to take their career path (technical vs. management)
  - Skills required including, technical and interpersonal
  - The need to continuously assess the skills you have and the skills required for the path you want to take

They will offer concrete advice on how to succeed on either path and identify ways to "manage" your career, including:

- What your career means to you
- How to add value to your organization
- How to get recognized
- Ways to influence the corporate culture

Panelists: Catherine Ahlschlager - *Hardware Manager, Sun Microsystems, Inc.*
Francine Bacchini - *Publisher, SCDsource™; Founder, President and CEO, Tech Source Media, Inc.*
Limor Fix - *Associate Director, Intel Research Pittsburgh*
Holly Stump - *Vice President of Marketing, Jasper Design Automation, Inc.*
Jan Willis - *Calibra Consulting*

Rm: 301

VIRTUAL PLATFORM WORKSHOP AT DAC

Topic Area: System-Level and Embedded

Wednesday - July 29, 9:00am - 5:30pm

Organizers: Soha Hassoun - *Tufts Univ., Medford, MA*
Larry Lapides - *Imperas, Inc., Thame, United Kingdom*

Registration: $150 (Member), $195 (Non-Member)

Virtual Platforms (VPs) have emerged as a cornerstone in SOC design validation and in embedded software development. Virtual platforms, a model representation created by assembling component models, enable early software development and lead to fewer silicon re-spins and shorter time-to-market. This workshop outlines challenges in building and utilizing VPs for software development and verification, and showcases solutions from both vendor and user perspectives. The purpose of this workshop is to bring together people interested in this topic to promote VPs, educate users about their potential, and to exchange usage experiences. The intended participants are those interested in various topics associated with VP use and development: IP use, SOC, embedded system, embedded software, and software functional verification.

The workshop begins with a tutorial-like state of the art overview on critical issues facing VP developers and users. The morning session then continues with detailed presentations on building VPs: exploring timing mechanisms in TLM (Transaction-Level Modeling), integration of RTL Models into Virtual Platforms for complex multicore systems, and platform composition and refinement. Speakers are from Qualcomm, Inc., Carbon Design Systems, Inc., and EVE.

The lunch time panel session brings several industry experts together to discuss issues facing virtual platform designers and users such as software reuse, status of VP standards, and how and when VPs will achieve broader acceptance. The panelists are from GreenSocs, Open Virtual Platforms, and Cadence Design Systems, Inc.

The afternoon session brings six industry experts to discuss tools and experiences in: software functional verification, architectural exploration on VPs, combining TLM-2.0 code with legacy virtual platforms, and system verification. The speakers are from CoWare, Inc., Intel Corp., Posedge Software, Imperas, Inc., and Synopsys, Inc.

Lunch Panel: 12:00 - 2:00pm, Rm: 302

Colocated Events at DAC

San Francisco Marriott

THE INTERNATIONAL CONFERENCE ON MICROELECTRONIC SYSTEMS EDUCATION

Topic Area: System-Level and Embedded

Saturday, July 25 - Monday, July 27, 8:00am - 5:00pm

Organizer: Don Bouldin - *Univ. of Tennessee, Knoxville, TN*

(MSE) is dedicated to furthering undergraduate and graduate education in designing and building innovative microelectronic systems. This conference provides an excellent opportunity for educators and industry to work together to ensure continued excellence in the field of microelectronic systems.

For more information: http://www.mseconference.org

Program Overview

Saturday, July 25, all day - Tutorials and workshops conducted by corporate patrons of MSE09.

Sunday, July 26, all day - Invited speakers, contributed papers, two poster sessions and buffet meals for lunch and dinner.

Monday, July 27, morning - additional invited speakers and contributed papers.

Monday, July 27, afternoon - demonstrations at the DAC University Booth.

Rm: 304

DESIGN AUTOMATION SUMMER SCHOOL 2009

Topic Area: General Interest

Saturday, July 25 - Sunday, July 26, 8:00am - 5:00pm

Organizers: Karam S. Chatha - *Arizona State Univ., Tempe, AZ*
Li Shang - *Univ. of Colorado, Boulder, CO*
Patrick Madden - *State Univ. of New York, Binghamton, NY*
Yuan Xie - *Pennsylvania State Univ., University Park, PA*
Diana Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*
Robert P. Dick - *Univ. of Michigan, Ann Arbor, MI*
Kartik Mohanram - *Rice Univ., Houston, TX*

Supported by:

The Design Automation Summer School will offer graduate students the opportunity to participate in a two day intensive course on selected areas of research and development in design automation. Each topic of instruction in this course will be covered by a distinguished speaker who will define the topic, describe recent accomplishments in considerable detail, and outline upcoming challenges.

Interactive discussions and follow-up activities among the participants will round off an intensive yet comprehensive activity geared towards graduate students in design automation.

For more information, visit the DASS website: http://ziyang.eecs.umich.edu/~dickrp/dass09/

Rm: 306/Lunch: 305

SLIP 2009: INTERNATIONAL WORKSHOP ON SYSTEM-LEVEL INTERCONNECT PREDICTION

Topic Area: Interconnect and Reliability

Sunday, July 26, 8:30am - 6:30pm

Organizer: Chung-Kuan Cheng - *Univ. of California, San Diego, La Jolla, CA*

Registration: $300 (Member), $380 (Non-Member), $250 (Student - ACM or IEEE Member), $300 (Non-Member Student)

The System-Level Interconnect Prediction (SLIP) Workshop focuses on modeling and prediction of the usable properties of optimized interconnect systems and their impact on system performance. Both theory and applications of interconnect prediction techniques are highlighted, with an emphasis on applications to architectural and micro-architectural exploration, physical design, interconnect technology planning and communication networks. In addition to the presentation of state of the art papers in these fields, invited talks and tutorials by leading researchers will aim to encourage dialogue between the architecture, physical design, and interconnect technology communities.

SLIP 2009 will feature special sessions on System-Level Interconnect Prediction for Emerging Technologies, with emphasis on 1) The implications of emerging technologies (e.g., 3-D integration, carbon nanotubes, quantum cellular automata) on system-level interconnect planning and synthesis and; 2) The synergies between estimation and analysis techniques for circuit interconnect systems and other large-scale networks arising in other context such as social web networks and systems biology.

Representative topics include:

1. Interconnect prediction at high-level synthesis
2. Interconnect prediction at logic synthesis or physical layout
3. Interconnect architecture of structural designs or FPGAs
4. Interconnect architecture of multiple cores or Network-On-Chips
5. Interface of chips or packaging
6. Interconnect of 3-D ICs
7. Interconnect of advanced technologies, e.g., electromagnetic / optical waves, carbon nanotubes, nanowires, spin waves, etc.
8. Distributions of powers or clocks
9. Synergies between chip intercommunication networks and networks arising in other contexts like social networks and system biology
10. Other related topics

For more information: http://www.sliponline.org/

Rm: 301

3RD IEEE INTERNATIONAL WORKSHOP ON DESIGN FOR MANUFACTURABILITY AND YIELD (DFM&Y)

Topic Area: DFM and the Manufacturing Interface

Sunday, July 26, 9:00am - 5:00pm

Organizers: Puneet Gupta - *Univ. of California, Los Angeles, CA*
Rob Aitken - *ARM Ltd., Sunnyvale, CA*

Registration: $200 (Member), $250 (Non-Member), $130 (Student - ACM or IEEE Member), $200 (Non-Member Student)

Increased manufacturing challenges in today's nanometer technologies require up to date solutions for yield optimization. Designing an SOC for manufacturability and yield aims at improving the manufacturing process and consequently its yield by enhancing communications across the design manufacturing interface. A wide range of Design for Manufacturability (DFM) and Design for Yield (DFY) methodologies and tools are in use today. Some of these are applied during the back-end design stages, including mask design, while others involve post-design activities, from lithography through wafer sort, packaging, final test and failure analysis. DFM can dramatically impact the business performance of chip manufacturers. It can also significantly affect age-old chip design flows. Using a DFM solution is an investment and thus choosing the most cost effective one(s) requires trade-off analysis. The workshop analyzes the key trends and challenges in DFM&Y, and provides an opportunity to discuss a range of DFM and DFY solutions for SOC designs now and in the future.

For more information: http://vlsicad.ucsd.edu/DFMY/

Rm: 130

LOW-POWER COALITION WORKSHOP: ADVANCES IN LOW-POWER DESIGN THROUGHOUT THE DESIGN FLOW

Topic Area: Low-Power Design

Sunday, July 26, 1:00 - 4:30pm

Organizers: Nick English, Sumit Dasgupta - *Si2, Austin, TX*

Complimentary Registration

The Low-Power Coalition (LPC) of Si2 has defined and published a power-aware reference flow that is recommended to the industry, including the power closure points and information available throughout the flow, from Electronic System Level (ESL) through implementation. This flow will be discussed. To aid in automating many of the steps along the tool chain, a draft power intent data model and associated Application Procedural Interface (API) are being defined that will work seamlessly with the OpenAccess API and information model. We will provide an early view of this data model and API. In addition, enhancements have been made to extend the Common Power Format (CPF), an Si2 standard first released as v1.0 in March 2007 and v1.1 in September 2008.

The current status and future direction of the format will be presented, including progress made since the last Low-power Workshop at DAC 2008; format interoperability goals and plans, and end-user experiences with the technology developed and implemented so far. A panel will discuss "What's Next," focusing on areas in which power flows, models, and formats might be extended to support additional power-aware design approaches, such as adaptive methods, asynchronous methods, etc. A selection of advanced tools to improve power-aware design, developed by EDA companies, will also be presented.

Panelists will be selected from speakers.

Speakers: **Gill Watt** - *Advanced Micro Devices, Inc., Boston, MA*
Qi Wang - *Cadence Design Systems, Inc., San Jose, CA*
Jerry Frenkil - *Sequence Design, Inc., Boston, MA*
David Hathaway - *IBM Corp., Burlington, VT*
Jake Buurma - *Si2, San Jose, CA*
Dale Pollek - *Atrenta, Inc., San Jose, CA*
Anmol Mathur, **Steve Carlson** - *Calypto Design Systems, Inc., San Jose, CA*

Rm: 304/Lunch: 303

2ND IEEE INTERNATIONAL WORKSHOP ON HARDWARE-ORIENTED SECURITY AND TRUST (HOST-2009)

Topic Area: New and Emerging Technologies

Monday, July 27, 7:30am - 6:00pm

Organizers: Jim Plusquellic - *Univ. of New Mexico, Albuquerque, NM*
Mohammad Tehranipoor - *Univ. of Connecticut, Storrs, CT*

Registration: $250 (Member), $320 (Non-Member), $200 (Student - ACM or IEEE Member), $250 (Non-Member Student)

The emergence of a globalized, horizontal semiconductor business model raises a set of concerns involving the security and trust of the information systems on which modern society is increasingly reliant for mission-critical functionality. Hardware-oriented security and trust (HOST) issues span a broad range including threats related to the malicious insertion of Trojan circuits designed e.g., to act as a `kill switch' to disable a chip, to integrated circuit piracy, to attacks designed to extract encryption keys and IP from a chip, to hardware-related malicious disruptions and/or diversions of systems. HOST covers security and trust issues in all types of electronic devices and systems such as ASICs, COTS, FPGAs, microprocessors/DSPs, and embedded systems. The mission of HOST is to provide a forum for the presentation and discussion of research that is of critical significance to the security of, and trust in, modern society's microelectronic-supported infrastructures.

Keynote Speaker: **Paul Kocher** - *President and Chief Scientist, Cryptography Research, Inc., San Francisco, CA*

For more information: http://www.engr.uconn.edu/HOST/

Rm: 301/Lunch: 302

7TH IEEE SYMPOSIUM ON APPLICATION SPECIFIC PROCESSORS (SASP)

Topic Area: System-Level and Embedded

Monday, July 27, 8:30am - 5:00pm - Tuesday, July 28, 11:00am - 5:00pm

Organizers: Cristina Silvano - *Politecnico di Milano, Milano, Italy*
Alex Orailoglu - *Univ. of California, San Diego, La Jolla, CA*

Registration: $420 (Member), $530 (Non-Member), $245 (Student - ACM or IEEE Member), $245 (Non-Member Student)

The market for embedded processors is driven primarily by two factors: cost and volume. This has forced a re-evaluation of the best way to satisfy users' needs for high-performance and low-energy consumption without drastically increasing the complexity of the design process. Domain-specific embedded processors, in markets such as network processing, automotive, and others, have splintered a pre-existing market for general-purpose, low-cost, low-energy processors. Reprogrammable and reconfigurable embedded processors, in contrast, offer a single, fixed-silicon device that could amortize manufacturing costs for low-to-medium volume market segments. SASP explores (micro)architectural design approaches, trade-offs, and compiler technologies, for both domain-specific and customizable embedded processors. The symposium is a forum wherein challenges and solutions will be explored, discussed, and compared.

Major topics include, but are not limited to:

- Domain-specific processors (Network, multimedia, etc.)
- Application-specific hardware accelerators
- Microarchitectural customization techniques
- (Re)configurable architectures (coarse-grained, FPGA, etc.)
- Application-specific processors in System-On-Chip (SOC)
- Application-specific customizations for low-power
- Applications and/or industrial experience
- Compiler technology targeting customizable processors
- Tools, techniques, and algorithms for architectural exploration
- Novel methodologies for hardware/software codesign
- Application specific MPSOC and design automation for NOCs
- Hardware/software for GPUs and other graphics/gaming platforms
- OS and middleware support for application specific processors

For more information: http://www.sasp-conference.org/

San Francisco Marriott

NORTH AMERICAN SYSTEMC USERS GROUP 11TH NASCUG MEETING

Topic Area: System-Level and Embedded

Monday, July 27, 1:30 - 6:00pm

Organizers: David Black - *XtremeEDA, Austin, TX*
Jill Jacobs - *MOD Marketing and Events LLC., San Jose, CA*

Sponsored by the Open SystemC Initiative

1:30 - 5:00pm: Technical Presentations

5:00pm: Networking Reception - Rm: Golden Gate A1-A2

Electronic system-level methodology has become mainstream. Broad acceptance of OSCI's transaction-level modeling standard, TLM-2.0, by companies worldwide clearly indicates a significant breakthrough for today's system-level design and verification. But changes are coming fast and furious. ESL design and modeling is expanding across multiple domains. How do we keep up with the challenges demanded by a diverse range of technology sectors?

Join us at the 11th North American SystemC Users Group (NASCUG) Meeting as innovative and influential industry leaders discuss these critical issues, as well as their real-world experiences in designing and modeling with SystemC.

Topics include:

- Transaction-Level modeling / OSCI TLM-2.0
- AMS Extensions Using SystemC
- Virtual Platform Design
- Architectural modeling
- Hardware/software codesign
- Verification techniques using SystemC and more!

For further information and to register:

www.nascug.org/

www.systemc.org/

Thanks to our Global Sponsors:

Rm: 130

DESIGN FOR MANUFACTURABILITY WORKSHOP - DFM CHALLENGES AT SUB-45NM DESIGN

Monday, July 27, 1:00 - 3:00pm

Organizers: Jake Buurma, Sumit Dasgupta - *Si2, Austin, TX*

Complimentary Registration

We have entered an era when Chip IP, SOC Design, manufacturing, and test are being done by different companies. The subject of Design for Manufacturability is rushing to the forefront of the list of challenges to the Semiconductor and EDA industries. This workshop will address the current situation in the DFM arena and describe tangible and specific progress in a number of design areas targeted at 45nm and below. This workshop will present interface standards being developed between chip design and manufacturing flows as well as a clear lexicon that defines most, if not all, manufacturing technology parameters which have here-to-fore been loosely described and have been often confused among foundries, EDA vendors, and end customers. This includes establishing a DFM Terminology and a roadmap for developing interface standards.

The workshop will also educate the audience on a high-level language that the Design for Manufacturability Coalition (DFMC) at Si2 has defined and published. The language called iCheck describes a comprehensive set of DFM parameters for Design Rule Checks, Critical Area Analysis, Lithography and Chemical Mechanical Planarization. Silicon foundries use iCheck to define the exact conditions required for a DFM hotspot check without having to describe how to perform the check. This workshop is not intended to continue to admire the problems of Design for Manufacturability, but to show that real progress is being made. As part of the workshop, selected vendors will present their products aimed at helping designers produce higher yielding integrated circuits and systems. Panelists will be selected from speakers.

Speakers: **Jim Culp** - *IBM Corp., East Fishkill, NY*
Greg Hackney - *Mentor Graphics Corp., Wilsonville, OR*
Qi De Qian - *IC Scope Research, Santa Clara, CA*
Mike Smayling - *Tela Innovations, Inc., San Jose, CA*
Vivek Singh - *Intel Corp., Hillsboro, OR*

Rm: 304

NASA/ESA CONFERENCE ON ADAPTIVE HARDWARE AND SYSTEMS (AHS 2009)

Topic Area: New and Emerging Technologies

Wednesday, July 29 - Saturday, August 1, 8:00am - 5:30pm

Organizers: Martin Suess, David Merodio - *European Space Agency, Noordwijk, The Netherlands*
Didier Keymeulen - *Jet Propulsion Laboratory, Pasadena, CA*
Tetsuya Higuchi - *National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan*
Steve Trimberger - *Xilinx, Inc., San Jose, CA*
Tughrul Arslan, Ahmet Erdogan - *Univ. of Edinburgh, Edinburgh, United Kingdom*
Umeshkumar Patel - *Goddard Space Flight Center, Greenbelt, MD*

Registration: $870 (Full Conference), $690 (Student)

The purpose of this conference is to bring together leading researchers from the adaptive hardware and systems community to exchange experiences and share new ideas in the field. The conference expands the topics addressed by the precursor series of NASA/DoD Conference on Evolvable Hardware, held between 1999 and 2005. With a broader scope (including a variety of hardware and system adaptation methods) and targeting more industry participation, the NASA/ESA series started with the AHS 2006 conference held in Istanbul, Turkey, the AHS 2007 conference held in Edinburgh, UK, and the AHS 2008 conference held in Noordwijk, The Netherlands.

Adaptation reflects the capability of a system to maintain or improve its performance in the context of internal or external changes, such as uncertainties and variations during fabrication, faults and degradations, modifications in the operational environment, incidental or intentional interference, different users and preferences, modifications of standards and requirements, trade-offs between performance and resources.

Adaptation at hardware levels increases the system capabilities beyond what is possible with software-only solutions, and a large number of adaptation features employing both analog and digital adjustments are becoming increasingly present in the most elementary system components. Algorithms, techniques, and their implementation in hardware are developed over a diverse variety of applications, such as adaptive communications (adapting to changing environment and interferences), reconfigurable systems on a chip and portable wireless devices (adapting to power limitations) or survivable spacecraft (adapting to extreme environments and mission unknowns). This meeting will provide a forum for discussion on the generic techniques of adaptive hardware and systems, with a focus on communications and space applications, and a view to its expansion and exploitation in other applications such as consumer, medical, defense and security.

For more information: http://www.see.ed.ac.uk/~ahs2009/

Rm: 301

IEEE/ACM SYMPOSIUM ON NANOSCALE ARCHITECTURES

Topic Area: New and Emerging Technologies

Thursday, July 30, 8:00am - 6:00pm - Friday, July 31, 8:00am - 5:00pm

Organizers: Shamik Das - *The MITRE Corp., McLean, VA*
Ramesh Karri - *New York Univ., Brooklyn, NY*

Registration: $300 (Member), $380 (Non-Member), $220 (Student)

Moore's law based scaling is rapidly approaching a "brick wall" as we enter the nanoelectronic regime. Novel silicon and non-silicon nanoelectronic devices are being developed to explicitly address this problem. Similarly, while defect and fault-tolerance techniques are designed under the assumption that a system is composed largely of correctly functioning units, this is no longer true in emerging nanoelectronics. In addition, nanoelectronics offers massive parallelism on a scale significantly beyond anything we have seen before, yet very few commercial massively parallel applications are envisioned. Also, while current computer aided design tools and methodologies can barely manage billion-transistor chips, how can trillion-device chips that nanoelectronics promises be designed?

The NANOARCH symposium is a forum for the presentation and discussion of novel architectures and design methodologies for future nanoscale implementations. The meeting has been held annually since 2005, and the 2009 Symposium seeks to build on the successes of prior editions.

The areas addressed by the symposium include massively parallel and biologically-inspired architectures, defect and fault-tolerant architectures, case studies on defect, fault and yield models, experimental reliability evaluation, validation frameworks, and design and simulation tools and emerging computational models.

The symposium's topics of interest include:

- Architectures for nanoelectronic digital and mixed-signal circuits and systems
- Computational paradigms and programming models for nanoscale architectures
- Modeling and simulation of nanoelectronic devices, circuits, and system architecture
- Simulation of complex systems with nanoscale computing architectures
- Implementing microarchitecture concepts using nanoarchitecture building blocks
- Defect and fault tolerant nanoelectronic device, circuit, and system-level architectures
- Manufacture testing of nanoelectronic architectures
- Computer-aided design tools and methodologies for nanoelectronic architecture

For more information: http://www.nanoarch.org/

Tuesday, July 28, 8:30 - 10:15am

Opening Remarks -
Andrew B. Kahng -
46th DAC General Chair

Keynote Address -
Overcoming the New Design Complexity Barrier: Alignment of Technology and Business Models

Fu-Chieh Hsu -
Vice President, Design and Technology Platform, Taiwan Semiconductor Manufacturing Company Ltd., Hsinchu, Taiwan

Marie R. Pistilli Women in EDA Achievement Award
Telle Whitney – *President and CEO, Anita Borg Institute for Women and Technology, Palo Alto, CA*

For her significant contributions in helping women advance in the field of EDA technology.

P.O. Pistilli Undergraduate Scholarships for Advancement in Computer Science and Electrical Engineering

The objective of the P.O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering, and Computer Science from under-represented groups (women, African American, Hispanic, Native American, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship and SIGDA continues to administer the program for DAC. DAC normally funds two or more $4000 scholarships, renewable up to five years, to graduating high school seniors.

The 2009 recipient is:

Cesar A. Torres, Jr.

Attending Stanford University, majoring in Computer Science.

For more information about the P.O. Pistilli scholarship, contact Andrew B. Kahng, Univ. of California, San Diego, CSE & ECE Depts., Mailcode #0404, 9500 Gilman Dr., La Jolla, CA 92093-0404.

Email: abk@cs.ucsd.edu

A. Richard Newton Graduate Scholarships

The DAC Executive Committee has chosen to name our existing DAC Graduate Scholarships after the late Professor A. Richard Newton. We feel that supporting young faculty and graduate research is an appropriate way to honor his vision and carry out some of his goals. Each year the Design Automation Conference sponsors several $24,000 scholarships to support graduate research and study in Design Automation (DA), with emphasis in "design and test automation of electronic and computer systems". Each scholarship is awarded directly to a University for the Faculty Investigator to expend in direct support of one or more DA graduate students. The criteria for granting such a scholarship expanded in 1996 to include financial need. The criteria are: the academic credentials of the student(s); the quality and applicability of the proposed research; the impact of the award on the DA program at the institution; and financial need. Preference is given to institutions that are trying to establish new DA research programs.

Advisor: **Shiyan Hu** – *Michigan Technological Univ., Houghton, MA*

Student: **Chen Liao** – *Michigan Technological Univ., Houghton, MA*

Project: High Performance Placement and Routing Techniques for Digital Microfluidic Biochip Design

ACM/IEEE A. Richard Newton Technical Impact Award in Electronic Design Automation

For seminal contributions to multilevel logic optimization impacting research, education and industrial practice.

Robert K. Brayton - *Univ. of California, Berkeley, CA*

Richard Rudell - *Los Gatos, CA*

Alberto Sangiovanni-Vincentelli - *Univ. of California and PARADES Berkeley, CA*

2008 Phil Kaufman Award for Distinguished Contributions to EDA

Sponsored by the EDA Consortium and IEEE Council on EDA

Aart J. de Geus – *Chairman, CEO and Co-Founder of Synopsys, Inc., Mountain View, CA*

Aart de Geus is the recipient of the prestigious 2008 Phil Kaufman Award for his significant impact on EDA and IC design through productizing advanced techniques beginning with logic optimization and synthesis.

2009 IEEE Emanuel R. Piore Award
David J. DeWitt - *Microsoft Corp., Madison, WI*

For fundamental contributions to the architecture, algorithms, and implementation of innovative database systems.

IEEE Transactions on Computer-Aided Design 2009 Donald O. Pederson Best Paper Award

Hristo Nikolov, Todor Stefanov, Ed F. Deprettere – *Leiden Univ., Leiden, The Netherlands*

For the paper entitled, **Systematic and Automated Multiprocessor System Design, Programming, and Implementation**. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 27, no. 3, pp. 542-555, March 2008.

IEEE Circuits and Systems Society 2009 Industrial Pioneer Award
Paul E. Jacobs – *Qualcomm CDMA Technologies, San Diego, CA*

Paul Jacobs' vision of wireless data services has been pioneering and transformational in the worldwide cellular industry. At Qualcomm, starting from the development of the first Palm OS® based Smartphone, and now in his capacity as CEO, he has grown company revenues to over $10B through this vision.

IEEE Circuits and Systems Society 2009 Vitold Belevitch Award
Ronald A. Rohrer – *SystemIC, Bend, OR*

For advancing circuit theory to solve practical circuit design problems with everlasting impact on the global electronic industry.

IEEE Circuits and Systems Society 2009 VLSI Transactions Best Paper Award

Nagarajan Ranganathan, Justin E. Harlow III, Mahalingam Venkataraman – *Univ. of S. Florida, Tampa, FL*

For the paper entitled, **A Fuzzy Optimization Approach for Variation Aware Power Minimization During Gate Sizing**.

IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 16, no. 8, pp. 975-984, August 2008.

Awards

2009 IEEE Fellow

Steven Nowick – *Columbia Univ., New York, NY*

For contributions to asynchronous and mixed-timing integrated circuits and systems.

Joel Phillips – *Cadence Research Labs, Berkeley, CA*

For contributions to numerical techniques in the design of high-frequency and radio frequency systems.

ACM Fellow

Jason (Jingsheng) Cong – *Univ. of California, Los Angeles, CA*

For contributions to electronic design automation.

Jonathan S. Rose – *Univ. of Toronto, Toronto, ON, Canada*

For contributions to the architecture and computer-aided design of field-programmable gate arrays (FPGAs).

Rob A. Rutenbar – *Carnegie Mellon Univ., Pittsburgh, PA*

For contributions to computer-aided design tools for mixed-signal integrated circuits.

SIGDA Distinguished Service Award

Nikil Dutt – *Univ. of California, Irvine, CA*

For contributions to ACM's Special Interest Group on Design Automation during the past fifteen years as a SIGDA officer, coordinator of the University Booth in its early years, and most recently, as Editor-in-Chief of the ACM Transactions on Design Automation of Electronic Systems.

ACM Outstanding PhD Dissertation Award in EDA

Student: **Kai-Hui Chang** – *Univ. of Michigan, Ann Arbor, MI*

Advisors: **Igor Markov, Valeria Bertacco** – Univ. of Michigan, Ann Arbor, MI

For the dissertation: Functional Design Error Diagnosis, Correction and Layout Repair of Digital Circuits.

SIGDA Outstanding New Faculty Award

Yu (Kevin) Cao – *Arizona State Univ., Tempe, AZ*

For a junior faculty member early in his/her academic career who demonstrates outstanding potential as an educator and/or researcher in the field of electronic design automation.

ACM Transactions on Design Automation of Electronic Systems (TODAES) 2009 Best Paper Award

Sivaram Gopalakrishnan, Priyank Kalla – *Univ. of Utah, Salt Lake City, UT*

Optimization of Polynomial Datapaths Using Finite Ring Algebra.

ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 12, Issue 4 (September 2007).

46th DAC Best Paper Candidates

Seven papers were nominated by the Technical Program Committee as DAC Best Paper Candidates. Final decisions will be made after the papers are presented at the conference. The awards for the best paper will be presented at 12:00pm on Thursday, July 30, in Gateway Ballroom, prior to the Special Plenary Panel.

10.3 Generating Test Programs to Cover Pipeline Interactions
Thanh Nga Dang – *National Univ. of Singapore, Singapore*
Abhik Roychoudhury – *National Univ. of Singapore, Singapore*
Tulika Mitra – *National Univ. of Singapore, Singapore*
Prabhat Mishra – *Univ. of Florida, Gainesville, FL*

12.1 GPU Friendly Fast Poisson Solver for Structured Power Grid Network Analysis
Jin Shi – *Tsinghua Univ., Beijing, China*
Yici Cai – *Tsinghua Univ., Beijing, China*
Wenting Hou – *Synopsys, Inc., Beijing, China*
Liwei Ma – *Synopsys, Inc., Beijing, China*
Sheldon X.-D. Tan – *Univ. of California, Riverside, CA*
Pei-Hsin Ho – *Synopsys, Inc., Hillsboro, OR*
Xiaoyi Wang – *Tsinghua Univ., Beijing, China*

15.1 An Efficient Approach for System-Level Timing Simulation of Compiler-Optimized Embedded Software
Zhonglei Wang – *Technische Univ. München, Munich, Germany*
Andreas Herkersdorf – *Technische Univ. München, Munich, Germany*

18.2 A Computing Origami: Folding Streams in FPGAs
Andrei Hagiescu – *National Univ. of Singapore, Singapore*
Weng-Fai Wong – *National Univ. of Singapore, Singapore*
David Bacon – *IBM Corp., Hawthorne, NY*
Rodric Rabbah – *IBM Corp., Hawthorne, NY*

22.1 Statistical Multi-Layer Process Space Coverage for At-Speed Test
Jinjun Xiong – *IBM Corp., Yorktown Hts., NY*
Yiyu Shi – *Univ. of California, Los Angeles, CA*
Vladimir Zolotov – *IBM Corp., Yorktown Hts., NY*
Chandu Visweswariah – *IBM Corp., Yorktown Hts., NY*

23.2 A Robust and Efficient Harmonic Balance (HB) Using Direct Solution of HB Jacobian
Amit Mehrotra – *Berkeley Design Automation, Santa Clara, CA*
Abhishek Somani – *Berkeley Design Automation, Bangalore, India*

24.3 New Spare Cell Design for IR Drop Minimization in Engineering Change Order
Hsien-Te Chen – *National Tsing-Hua Univ., Hsinchu, Taiwan*
Chieh-Chun Chang – *National Tsing-Hua Univ., Hsinchu, Taiwan*
TingTing Hwang – *National Tsing-Hua Univ., Hsinchu, Taiwan*

2009 DAC/ISSCC Student Design Contest Winners

The Student Design Contest promotes excellence in the design of electronic systems by providing a competition for graduate and undergraduate students at universities and colleges. It is co-organized by DAC and ISSCC. This year we received over 60 submissions in three categories: operational systems, operational chips and conceptual designs based on simulation. Nine award winners were selected. The Student Design Contest is co-sponsored by DAC, industry sponsors and ISSCC.

Awards will be presented at the DAC Pavilion on the exhibit floor, Booth 1928, Monday, July 27 from 5:00 – 6:00pm. The ceremony will include a brief overview of presentations from each winning project team.

Smart Memories Polymorphic Chip Multiprocessor
Ofer Shacham, Zain Asgar, Han Chen, Amin Firoozshahian, Rehan Hameed, Christos Kozyrakis, Wajahat Qadeer, Stephen Richardson, Alexandre Solomatnikov, Don Stark, Megan Wachs, Mark Horowitz – *Stanford Univ., Stanford, CA*

Large-Scale SRAM Variability Characterization Chip in 45nm CMOS
Zheng Guo, Andrew Carlson, Liang-Teck Pang, Kenneth Duong, Tsu-Jae King Liu, Borivoje Nikolic - *Univ. of California, Berkeley, CA*

A 600MS/s 30mW 0.13µm CMOS ADC Array Achieving over 60dB SFDR with Adaptive Digital Equalization
Wenbo Liu, Yun Chiu – *Univ. of Illinois, Urbana-Champaign, Urbana, IL*

A 212MPixels/s 4096x2160p Multiview Video Encoder Chip for 3-D/Quad HDTV Applications
Li-Fu Ding, Wei-Yin Chen, Pei-Kuei Tsung, Tzu-Der Chuang, Pai-Heng Hsiao, Yu-Han Chen, Shao-Yi Chien, Liang-Gee Chen – *National Taiwan Univ., Taipei, Taiwan*

A Fully-Automated Process Characterization Macro for Gate Dielectric Breakdown
John Keane, Shrinivas Venkatraman, Chris H. Kim – *Univ. of Minnesota, Minneapolis, MN*
Paulo F. Butzen – *Univ. Estadual do Rio Grande do Sul, Porto Alegre, Brazil*

A Heterogeneous MPSOC with Hardware Supported Dynamic Task Scheduling for Software Defined Radio
Torsten Limberg, Markus Winter, Marcel Bimberg, Reimund Klemm, Marcos Tavares, Holger Eisenreich, Georg Ellguth, Jens-Uwe Schlüßler, Emil Matus, Gerhard Fettweis – *Technische Univ. Dresden, Dresden, Germany*
Hendrik Ahlendorf – *ZMD AG, Dresden, Germany*

An Ultrasensitive CMOS Magnetic Biosensor Array for Point-Of-Care (POC) Microarray Application
Hua Wang, Ali Hajimiri – *California Institute of Technology, Pasadena, CA*

Phoenix: An Ultra-Low-Power Processor for Cubic Millimeter Sensor Systems
Mingoo Seok, Scott Hanson, Yu-Shiang Lin, Zhiyoong Foo, Daeyeon Kim, Yoonmyung Lee, Nurrachman Liu, Dennis Sylvester, David Blaauw – *Univ. of Michigan, Ann Arbor, MI*

A 1.2 V 26 mW Configurable Multiuser Mobile MIMO-OFDM/-OFDMA Baseband Processor
Jung-Mao Lin, Hsin-Yi Yu, Yu-Jen Wu, Hsi-Pin Ma – *National Tsing-Hua Univ., Hsinchu, Taiwan*

Technical Sessions

Tuesday, July 28, 10:30am - 12:00pm

1 PANEL: SYSTEM PROTOTYPES: VIRTUAL, HARDWARE OR HYBRID?

Rm: 102

Topic Area: System-Level and Embedded

Chair: Ron Wilson - *EDN Magazine, San Jose, CA*
Organizers: Eshel Haritan - *CoWare, Inc., San Jose, CA*
Tom Borgstrom - *Synopsys, Inc., Mountain View, CA*

Almost all SOC designs today use hardware prototyping at some point of the development cycle to perform hardware/software validation or test interfaces to real-world stimulus. Recently, virtual prototypes have emerged as a way to run system level tests and perform hardware/software co-simulation before silicon or hardware prototypes are available. Does the emergence of virtual prototyping mean the end for FPGA-based prototypes? Will the hardware prototype continue to live on as an integral part of the SOC design cycle? Will hybrids of virtual and hardware prototypes be the answer? Join our expert panelists in a spirited discussion on the best approach for speeding the verification and validation of complex SOC using system prototypes. Virtual, hardware or hybrid – which will reign supreme?

Speakers: **David Abada** - *Amicus Wireless, Sunnyvale, CA*
Andrew Dauman - *Synopsys, Inc., Sunnyvale, CA*
Ramesh Chandra - *Qualcomm, Inc., San Diego, CA*
Olivier Mielo - *ST-Ericsson, Sophia Antipolis, France*
Chuck Cruse - *LSI Corp., Colorado Springs, CO*
Achim Nohl - *CoWare, Inc., Aachen, Germany*

2 SPECIAL SESSION: MECHANISMS FOR SURVIVING UNCERTAINTY: OPPORTUNITIES AND PROSPECTS

Rm: 133

Topic Area: Interconnect and Reliability

Chair: Subhasish Mitra - *Stanford Univ., Stanford, CA*
Organizers: Nagib Z. Hakim - *Intel Corp., Santa Clara, CA*
Vladimir Zolotov - *IBM Corp., Yorktown Hts., NY*

The focus of this technical session is to provide a perspective on the different approaches to mitigate the effects of uncertainty in semiconductor design. In the last several years, an increasing impact of variations and uncertainty in circuits has been felt. The industry has seen an increase in EDA tools and methodologies to understand, model and simulate these effects. The community has recognized that these issues are here to stay and must be accounted for during product design. The session shifts the emphasis from simulation and analysis to mitigation. It explores approaches to make products tolerant to these effects. The advances in developing resilient designs and various aspects of these solutions are presented by industry and academic leaders. The session will highlight key technologies and the practical experience in the implementation process.

2.1 **Circuit Techniques for Dynamic Variation Tolerance**
Keith Bowman, James Tschanz, Chris Wilkerson, Shih-Lien Lu, Tanay Karnik, Vivek De, Shekhar Borkar - *Intel Corp., Hillsboro, OR*

2.2 **Enabling Adaptability Through Elastic Clocks**
Emre Tuncer - *Elastix Corp., Los Gatos, CA*
Jordi Cortadella - *Univ. Politècnica de Catalunya, Barcelona, Spain*
Luciano Lavagno - *Politecnico di Torino, Torino, Italy*

2.3 **Addressing Design Margins Through Error-Tolerant Circuits**
Shidhartha Das, David Bull, **Krisztián Flautner** - *ARM Ltd., Cambridge, United Kingdom*
David Blaauw - *Univ. of Michigan, Ann Arbor, MI*
Rob Aitken - *ARM Ltd., Sunnyvale, CA*

3 COMBATING NON-IDEALITIES IN STATIC TIMING ANALYSIS

Rm: 123

Topic Area: Interconnect and Reliability

Chair: Puneet Gupta - *Univ. of California, Los Angeles, CA*

Static timing analysis has been studied for a long time, however there are still non-idealities that have not been addressed properly. Papers in this session tackle these non-idealities for improving accuracy. The first paper addresses aggressor-victim alignment for crosstalk analysis with current-source driver model. The second paper improves waveform propagation from interconnect end to gate input. The third paper gives a method that considers both false-path and multiple-input switching.

3.1 **Worst-Case Aggressor-Victim Alignment with Current-Source Driver Models**
Ravikishore Gandikota, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*
Li Ding, Peivand Tehrani - *Synopsys, Inc., Mountain View, CA*

3.2 **A Moment-Based Effective Characterization Waveform for Static Timing Analysis**
David D. Ling, **Chandu Visweswariah**, Peter Feldmann - *IBM Corp., Yorktown Hts., NY*
Soroush Abbaspour - *IBM Corp., Hopewell Jct., NY*

3.3 **A False-Path Aware Formal Static Timing Analyzer Considering Simultaneous Input Transitions**
Shihheng Tsai, Chung-Yang (Ric) Huang - *National Taiwan Univ., Taipei, Taiwan*

Rm: 130

4 HIGH-PERFORMANCE PLATFORMS: ADVANCES IN SYSTEM-LEVEL EXPLORATION AND OPTIMIZATION

Topic Area: System-Level and Embedded

Chair: Greg Stitt - *Univ. of Florida, Gainesville, FL*

Multicore and instruction-set-extended platforms enable high performance, but involve the challenging tasks of design space exploration and optimization. The first paper uses a modified data cache and compiler to provide data to custom instruction-set-extended datapaths for high performance and low-power. The remaining papers deal with multicore platforms. The second paper merges formal application models with SystemC platform models to enable rapid system exploration. The third uses integer linear programming to explore and obtain timing analyses of automotive applications mapped to distributed electronic control units. The last paper maximizes multicore performance subject to power and thermal constraints and process variations.

4.1 Way Stealing: Cache-Assisted Automatic Instruction Set Extensions
Theo Kluter, Philip Brisk, Paolo Ienne - *Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland*
Edoardo Charbon - *Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland and Delft Univ. of Technology, Delft, The Netherlands*

4.2 SysCOLA: A Framework for Co-Development of Automotive Software and System Platform
Zhonglei Wang, Wolfgang Haberl, Andreas Herkersdorf - *Technische Univ. München, Munich, Germany*
Martin Wechs - *BMW Forschung und Technik GmbH, Munich, Germany*

4.3S Designing Heterogeneous ECU Networks via Compact Architecture Encoding and Hybrid Timing Analysis
Michael Glaß, Martin Lukasiewycz, Jürgen Teich - *Friedrich-Alexander-Univ. Erlangen-Nürnberg, Erlangen, Germany*
Unmesh D. Bordoloi - *Verimag Labs, Gieres, France*
Samarjit Chakraborty - *Technische Univ. München, Munich, Germany*

4.4S Optimizing Throughput of Power and Thermal-Constrained Multicore Processors Using DVFS and Per-Core Power-Gating
Jungseob Lee, **Nam Sung Kim** - *Univ. of Wisconsin, Madison, WI*

Rm: 125

5 NOVEL DESIGN AND VERIFICATION METHODOLOGIES

Topic Area: Physical Design

Chair: Yu (Kevin) Cao - *Arizona State Univ., Tempe, AZ*

The papers in this session span the entire design flow. The first paper presents a 3-D implementation of a real-world design and compares its performance to the usual 2-D implementation. The second paper presents a power-efficient yield optimization methodology for robust cache design. The final two papers present methods for improving design reliability: one uses lithography-friendly routing and redundant via insertion, while the second uses model-based design rule checks taking into account manufacturing variability.

5.1 Design Automation for a 3DIC FFT Processor for Synthetic Aperture Radar: A Case Study
Thorlindur R. Thorolfsson, Kiran Gonsalves, Paul D. Franzon - *North Carolina State Univ., Raleigh, NC*

5.2 Selective Wordline Voltage Boosting for Caches to Manage Yield under Process Variations
Yan Pan - *Northwestern Univ., Evanston, IL*
Joonho Kong, Sung Woo Chung - *Korea Univ., Seoul, Republic of Korea*
Serkan Ozdemir, Gokhan Memik - *Northwestern Univ., Evanston, IL*

5.3S Double Patterning Lithography Friendly Detailed Routing with Redundant via Consideration
Kun Yuan, Katrina Lu, David Z. Pan - *Univ. of Texas, Austin, TX*

5.4S Use of Lithography Simulation for the Calibration of Equation-Based Design Rule Checks
David Abercrombie, Fedor G. Pikus, Cosmin Cazan - *Mentor Graphics Corp., Wilsonville, OR*

Rm: 124

6 DESIGN AND OPTIMIZATION OF NANOCIRCUITS

Topic Area: New and Emerging Technologies

Chair: Paul Franzon - *North Carolina State Univ., Raleigh, NC*

This session explores how to fabricate and assemble nanoscale devices into optimized logic circuits and memory. The first paper describes how to build logic gates from carbon nanotubes in the face of variation. The second paper shows how to fabricate and optimize decoders to bridge between lithographic-scale wires and sublithographic nanowires that are formed by conformal deposition. The third paper develops logic synthesis techniques for threshold gate circuits based on NDRs. The final paper illustrates how spin-torque transfer MRAM density can be optimized via codesign of error-correcting codes and transistor sizing.

6.1 Carbon Nanotube Circuits in the Presence of Carbon Nanotube Density Variations
Jie Zhang, Nishant Patil, Subhasish Mitra, Arash Hazeghi - *Stanford Univ., Stanford, CA*

6.2 Decoding Nanowire Arrays Fabricated with the Multi-Spacer Patterning Technique
Haykel Ben Jamaa, Yusuf Leblebici, Giovanni De Micheli - *Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland*

6.3S Boolean Logic Function Synthesis for Generalized Threshold Gate Circuits
Marek A. Bawiec, Maciej Nikodem - *Politechnika Wrocławska, Wroclaw, Poland*

6.4S Improving STT MRAM Storage Density Through Smaller-Than-Worst-Case Transistor Sizing
Wei Xu, Tong Zhang - *Rensselaer Polytechnic Institute, Troy, NY*
Yiran Chen - *Seagate Technology, Shakopee, MN*
Xiaobin Wang - *Seagate Technology, Minneapolis, MN*

Rm: 102

7 PANEL: EDA IN FLUX – SHOULD I STAY OR SHOULD I GO?

Topic Area: General Interest

Chair: Tina Jones - *Cadence Design Systems, Inc., San Jose, CA*
Organizers: Andreas Kuehlmann - *Cadence Design Systems, Inc., Berkeley, CA*
Eshel Haritan - *CoWare, Inc., San Jose, CA*

"A crisis is a terrible thing to waste". Quotes like this are often heard by experts in the industry and academia, but what does this mean to me? How should I change my professional interests? How should I evolve my career? How is EDA going to evolve? This panel represents multiple points of views on these questions. Four experts will review the current job situation in EDA and provide a historical perspective for previous recessions. The panel will further discuss views on new directions for the electronics market, how EDA should evolve, and options for career development during the slow down of the industry.

Speakers: **John Epperheimer** - *Workpath Group, LLC, San Jose, CA*
Jan Rabaey - *Univ. of California, Berkeley, CA*
Rahul Razdan - *Univ. of Florida, Gainesville, FL*
Naveen Gupta - *Yahoo!, Inc., Sunnyvale, CA*

Rm: 133

8 SPECIAL SESSION: DAWN OF THE 22NM DESIGN ERA - YES WE CAN!

Topic Area: DFM and the Manufacturing Interface

Chair: Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*
Organizer: Ruchir Puri - *IBM Corp., Yorktown Hts., NY*

45nm CMOS designs are in full production in the semiconductor industry and 32nm design rules and infrastructure is already in place for designs starting later this year. It will not be long before the beat of 22nm will be upon us. This session proposes to cover unique aspects of 22nm CMOS designs and issues that EDA industry must address for this imminent transition. Talks in this session will focus on 22nm CMOS design issues; circuit process interactions that will be crucial for success of 22nm; a discussion on regular layouts and trade-offs; and the discipline and risk management to succeed with 22nm designs. We will explore ideas and opinions on how to reduce the time and investment necessary to drive the use of 22nm CMOS technology for future products and systems. The semiconductor industry is facing serious challenges towards further scaling: creativity and innovation will be required in process, device and circuit design. Some of the burning questions that will be answered in this session include: we can make it (22nm technology), but can we design with it? What is the truth on methodology and tool support for 22nm design and verification? Can we accelerate adoption of this technology? Is a regular layout methodology the solution to the trouble for 32nm and below? Some have argued that so-called restrictive design approaches limit designers' creativity, forcing them to design within constraints established to ensure higher yield. Are the constraints imposed by process variability's impact on yield already beginning to trump designers' creativity?

8.1 Design Perspectives on 22nm CMOS and Beyond
Shekhar Borkar - *Intel Corp., Hillsboro, OR*

8.2 Creating an Affordable 22nm Node Using Design-Lithography Co-Optimization
Andrzej Strojwas, Tejas Jhaveri, Vyacheslav Rovner, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

8.3 Device/Circuit Interactions at 22nm Technology Node
Kaushik Roy, Jaydeep P. Kulkarni, Sumeet Kumar Gupta - *Purdue Univ., West Lafayette, IN*

8.4 Beyond Innovation: Dealing with the Risks and Complexity of Processor Design in 22nm
Carl Anderson - *IBM Corp., Austin, TX*

Rm: 123

9 STATISTICAL METHODS IN STATIC TIMING ANALYSIS

Topic Area: Interconnect and Reliability

Chair: Matthew Guthaus - *Univ. of California, Santa Cruz, CA*

Statistical methods have become an important technique for modeling variability of circuit timing. This session discusses several interesting applications of statistical methodology. The first paper constructs a model of spatial variation on the basis of across wafer variability. The second paper applies Gaussian mixture models for expressing non-Gaussian variations in statistical timing. The third paper analyzes stochastic jitter in digital timing recovery circuits using Markov chain models. The fourth paper develops statistical ordering of correlated timing quantities for path ranking. The last paper proposes a practical technique for analyzing spatial variability in timing analysis.

9.1 Physically Justifiable Die-Level Modeling of Spatial Variation in View of Systematic Across Wafer Variability
Lerong Cheng, Puneet Gupta, Lei He - *Univ. of California, Los Angeles, CA*
Costas J. Spanos, Kun Qian - *Univ. of California, Berkeley, CA*

9.2 A Gaussian Mixture Model for Statistical Timing Analysis
Shingo Takahashi - *NEC Corp., Tokyo, Japan*
Yuki Yoshida, Shuji Tsukiyama - *Chuo Univ., Tokyo, Japan*

9.3 A Stochastic Jitter Model for Analyzing Digital Timing-Recovery Circuits
James Burnham - *High-Q Design, Sunnyvale, CA*
Chih-Kong Ken Yang - *Univ. of California, Los Angeles, CA*
Haitham Hindi - *Palo Alto Research Center, Inc., Palo Alto, CA*

9.4S Statistical Ordering of Correlated Timing Quantities and its Application for Path Ranking
Jinjun Xiong, Chandu Visweswariah, Vladimir Zolotov - *IBM Corp., Yorktown Hts., NY*

9.5S A Parametric Approach for Handling Local Variation Effects in Timing Analysis
Ayhan Mutlu, Jiayong Le, Ruben Molina, Mustafa Celik - *Extreme DA Corp., Santa Clara, CA*

Rm: 130

10 PROFILING,TEST AND DEBUG OF EMBEDDED SYSTEMS

Topic Area: System-Level and Embedded

Chair: Tony Givargis - *Univ. of California, Irvine, CA*

This session presents novel ideas in performance profiling, test program generation, and application debugging in the realm of embedded systems. The first two papers present hardware enhancements to processor architectures that enable runtime application profiling. The third paper in the session presents an approach for on-the-fly test program generation based on a formal model of the processor pipeline. Finally, the last paper presents architectural innovations for multicore processors that enable program debugging and race condition detection.

10.1 Non-Intrusive Dynamic Application Profiling for Multi-Tasked Applications
Karthik Shankar, Roman Lysecky - *Univ. of Arizona, Tucson, AZ*

10.2 A Trace-Capable Instruction Cache for Cost Efficient Real-Time Program Trace Compression in SOC
Chun-Hung Lai, Fu-Ching Yang, Chung-Fu Kao, Ing-Jer Huang - *National Sun Yat-sen Univ., Kaohsiung, Taiwan*

10.3 Generating Test Programs to Cover Pipeline Interactions
Thanh Nga Dang, **Abhik Roychoudhury**, Tulika Mitra - *National Univ. of Singapore, Singapore*
Prabhat Mishra - *Univ. of Florida, Gainesville, FL*

10.4 NUDA: A Non-Uniform Debugging Architecture and Non-Intrusive Race Detection for Many-Core
Chi-Neng Wen, Shu-Hsuan Chou, Tien-Fu Chen - *National Chung Cheng Univ., Chia-Yi, Taiwan*
Alan Peisheng Su - *Global Unichip Corp., Hsinchu, Taiwan*

Rm: 125

11 LOW-POWER DESIGN AND ANALYSIS TECHNIQUES

Topic Area: Low-Power Design

Chair: Stephen Kosonocky - *Advanced Micro Devices, Inc., Fort Collins, CO*

This session presents papers that address a spectrum of techniques in low-power analysis and design. The first paper addresses smart sampling techniques for chip leakage analysis with process variations. The second paper discusses infeasible clock-gating functions and is followed by a talk on low-power gated bus synthesis for communication on SOCs. And the final paper addresses an efficient and non-intrusive extension for activity based analysis of SystemC models.

11.1 Efficient Smart Sampling-Based Full-Chip Leakage Analysis for Intra-Die Variation Considering State Dependence
Vineeth Veetil, Dennis Sylvester, David Blaauw - *Univ. of Michigan, Ann Arbor, MI*
Saumil Shah, Steffen Rochel - *Blaze DFM, Inc., Sunnyvale, CA*

11.2 Resurrecting Infeasible Clock-Gating Functions
Eli Arbel, Cindy Eisner, Oleg Rokhlenko - *IBM Corp., Haifa, Israel*

11.3 Low-Power Gated Bus Synthesis Using Shortest-Path Steiner Graph for System-On-Chip Communications
Renshen Wang, Chung-Kuan Cheng - *Univ. of California, San Diego, La Jolla, CA*
Nan-Chi Chou, Bill Salefski - *Mentor Graphics Corp., San Jose, CA*

11.4 ActivaSC: A Highly Effcient and Non-Intrusive Extension for Activity-Based Analysis of SystemC Models
Cedric Walravens, Yves Vanderperren, Wim Dehaene - *Katholieke Univ. Leuven, Leuven, Belgium*

Rm: 124

12 DESIGN INTEGRITY CHALLENGES

Topic Area: Interconnect and Reliability

Chair: Chandra Kashyap - *Intel Corp., Hillsboro, OR*

Power delivery robustness, fault tolerance and process variational impact challenge modern design approaches and are addressed in this session. The first paper addresses a novel way to create a closed form solution out of power grid equations. The second paper enhances vectorless power grid verification with an approximate matrix inverse. The third paper formally proves the robustness of a digital circuit. The final paper addresses variational impact on clock skew using wire sizing.

12.1 GPU Friendly Fast Poisson Solver for Structured Power Grid Network Analysis
Jin Shi, Yici Cai, Xiaoyi Wang - *Tsinghua Univ., Beijing, China*
Wenting Hou, Liwei Ma - *Synopsys, Inc., Beijing, China*
Sheldon X.-D. Tan - *Univ. of California, Riverside, CA*
Pei-Hsin Ho - *Synopsys, Inc., Hillsboro, OR*

12.2 Fast Vectorless Power Grid Verification Using an Approximate Inverse Technique
Nahi H. Abdul Ghani, Farid N. Najm - *Univ. of Toronto, Toronto, ON, Canada*

12.3 Computing Bounds for Fault Tolerance Using Formal Techniques
Goerschwin Fey, Andre Suelflow, Rolf Drechsler - *Univ. of Bremen, Bremen, Germany*

12.4 Clock Skew Optimization via Wire-Sizing for Timing Sign-Off Covering All Process Corners
Sari Onaissi, Khaled R. Heloue, Farid N. Najm - *Univ. of Toronto, Toronto, ON, Canada*

Technical Sessions

Tuesday, July 28, 4:30 - 6:00pm

Rm: 102

13 PANEL: MOORE'S LAW: ANOTHER CASUALTY OF THE FINANCIAL MELTDOWN?

Topic Area: Business

Chair: William H. Joyner, Jr. - *Semiconductor Research Corp. and IBM Corp., Durham, NC*
Organizers: Jason Cong - *Univ. of California, Los Angeles, CA*
Nagaraj NS - *Texas Instruments, Inc., Dallas, TX*
Ruchir Puri - *IBM Corp., East Fishkill, NY*

Given the exponential increase of fabrication costs, the global recession and credit crunch, one may ask if Moore's Law is financially viable beyond 22nm node. Can we justify the return-of-investment (ROI) for continuous scaling beyond 22nm? Shall we consider other alternatives for integration, such as silicon-in-a-package (SiP) or 3-D integrations?

Speakers: **Riko Radojcic** - *Qualcomm, Inc., San Diego, CA*
Hans Stork - *Applied Materials, Inc., Santa Clara, CA*
Jeff Burns - *IBM Corp., Yorktown Hts., NY*
Peter Rickert - *Texas Instruments, Inc., Dallas, TX*
Moshe Gavrielov - *Xilinx, Inc., San Jose, CA*

Rm: 133

14 SPECIAL SESSION: VERIFYING AN SOC MONSTER: WHOSE JOB IS IT ANYWAY?

Topic Area: Verification and Test

Chair: Badri Gopalan - *Synopsys, Inc., Sunnyvale, CA*
Organizer: Raj S. Mitra - *Texas Instruments, Inc., Bangalore, India*

With the growing complexity of SOCs, verification is no longer a verification team's job alone. This task now spans across different teams – architecture design, IP design, SOC integration, and software teams – and often requires integrated effort across the teams. This session brings together different aspects of cross-team coordination of this complex task. The first paper describes the problem and its different dimensions, and stresses the importance of verification planning, especially for integrating multiple domains (e.g., mixed-signal) and technologies (e.g., emulation). The second paper focuses on reuse between IP and SOC teams, and what it really means to package pieces of internal design into reusable IP, specifically for internal consumption. The third paper looks at ways to architect for verification, and to restructure and streamline the traditional verification flow so that a significant part of the verification is done prior to the start of RTL. The final paper describes the role of verification within the complete product development life cycle, from architecture to design to post-silicon, and how it cycles back and feeds into the architecture for the next generation.

14.1 **Holistic Verification: Myth or Magic Bullet?**
Pradip A. Thaker - *Analog Devices, Inc., Bangalore, India*

14.2 **Verification Problems in Reusing Internal Design Components**
Warren Stapleton - *Advanced Micro Devices, Inc., Austin, TX*
Paul Tobin- *Advanced Micro Devices, Inc., Boxborough, MA*

14.3 **Exploiting "Architecture for Verification" to Streamline the Verification Process**
David Whipp - *NVIDIA Corp., San Jose, CA*

14.4 **The Role of the Verification Team Throughout the ASIC Development Life Cycle**
Eric Chesters - *Cisco Systems, Inc., San Jose, CA*

Rm: 123

15 TIMING SIMULATION: OPTIMIZED EMBEDDED SOFTWARE AND MPSOCs

Topic Area: System-Level and Embedded

Chair: Luciano Lavagno - *Politecnico di Torino, Torino, Italy*

This session presents the state of the art of timing simulation for embedded systems. The first paper shows a method to provide accurate timing analysis for optimized software with no sacrifices of the simulation speed. The second paper describes timing simulation of multicores that considers interaction with DRAMS. The third paper presents a fast workload simulation method for cycle-count analysis of MPSOCs.

15.1 **An Efficient Approach for System-Level Timing Simulation of Compiler-Optimized Embedded Software**
Zhonglei Wang, Andreas Herkersdorf - *Technische Univ. München, Munich, Germany*

15.2 **MPTLsim: A Simulator for X86 Multicore Processors**
Hui Zeng, Matt Yourst, **Kanad Ghose**, Dmitry Ponomarev - *State Univ. of New York, Binghamton, NY*

15.3 **Trace-Driven Workload Simulation Method for Multiprocessor System-On-Chips**
Tsuyoshi Isshiki, Dongju Li, Hiroaki Kunieda - *Tokyo Institute of Technology, Tokyo, Japan*
Toshio Isomura, Kazuo Satou - *Toyota Motor Corp., Toyota, Japan*

S - denotes a short paper | Orange titles signify a best paper candidate

Rm: 130

16 ADVANCES IN EMBEDDED SYSTEM MODELING AND OPTIMIZATION

Topic Area: System-Level and Embedded

Chair: Rajesh Gupta - *Univ. of California, San Diego, La Jolla, CA*

Design modeling and optimization is a critical enabler for future embedded system design. This session showcases four novel techniques. The first paper models the impact of process variation to power analysis sensitivity in security systems. The next two papers discuss design space explorations in customizable processors. They propose techniques to discover the optimal Pareto curves in multi-objective optimization by approximation algorithms and integer linear programming. The final paper introduces a new encoding scheme that optimizes the computation of linear equations in DSP applications.

16.1 Analysis and Mitigation of Process Variation Impacts on Power-Attack Tolerance
Lang Lin, Wayne Burleson - *Univ. of Massachusetts, Amherst, MA*

16.2 Evaluating Design Trade-Offs in Customizable Processors
Unmesh D. Bordoloi - *Verimag Labs, Gieres, France*
Huynh Phung Huynh, Tulika Mitra - *National Univ. of Singapore, Singapore*
Samarjit Chakraborty - *Technische Univ. München, Munich, Germany*

16.3S A Design Flow for Application Specific Heterogeneous Pipelined Multiprocessor Systems
Haris Javaid, Sridevan Parameswaran - *Univ. of New South Wales, Sydney, Australia*

16.4S Xquasher: A Tool for Efficient Computation of Multiple Linear Expressions
Arash Arfaee, Ali U. Irturk, Ryan Kastner - *Univ. of California, San Diego, La Jolla, CA*
Nikolay Laptev - *Univ. of California, Los Angeles, CA*
Farzan Fallah - *Envis Corp., Santa Clara, CA*

Rm: 125

17 INTERCONNECT OPTIMIZATION FOR EMERGING TECHNOLOGIES

Topic Area: New and Emerging Technologies

Chair: Jeff Welser - *IBM Corp. and Semiconductor Research Corp., San Jose, CA*

This session deals with several promising emerging technologies, including microfluidic biochips, nanophotonics and quantum circuits. The first paper proposes an interconnect-centric ILP-based design flow for labs-on-chip. The second paper architects a hybrid on-chip network that integrates metal and optical interconnect, and evaluates it in the context of multicore CPUs with distributed caches. The third paper introduces a new BDD-based approach to synthesizing reversible/quantum circuits and achieves greater scalability than previously known techniques.

17.1 ILP-Based Pin-Count Aware Design Methodology for Microfluidic Biochips
Cliff Chiung-Yu Lin, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

17.2 O-Router: An Optical Routing Framework for Low-Power On-Chip Silicon Nano-Photonics Integration
Duo Ding, Yilin Zhang, Haiyu Huang, Ray T. Chen, David Z. Pan - *Univ. of Texas, Austin, TX*

17.3 BDD-Based Synthesis of Reversible Logic for Large Functions
Robert Wille, Rolf Drechsler - *Univ. of Bremen, Bremen, Germany*

Rm: 124

18 DESIGN FLEXIBILITY: BEND IT, SHAPE IT, ANYWAY YOU WANT IT!

Topic Area: Synthesis and FPGA

Chair: Emre Tuncer - *Elastix Corp., Los Gatos, CA*

Flexibility and adaptability are the focus of this session. The first paper presents a flexible interface methodology for easily adding debugging capabilities to HDL interfaces, especially for generating information to be tracked by a process running on a host environment. The second paper looks at "folding" streams onto FPGA co-processors to create efficient design implementations. The session wraps up with two papers centered around Elastic Buffer (EB) techniques for generating circuits with expanded capabilities for handling variation using retiming and speculation.

18.1 Soft Connections: Addressing the Hardware-Design Modularity Problem
Michael Pellauer - *Massachusetts Institute of Technology, Cambridge, MA*
Michael Adler, Joel Emer - *Intel Corp., Hudson, MA*
Derek Chiou - *Univ. of Texas, Austin, TX*

18.2 A Computing Origami: Folding Streams in FPGAs
Andrei Hagiescu, Weng-Fai Wong - *National Univ. of Singapore, Singapore*
David F. Bacon, Rodric Rabbah - *IBM Corp., Hawthorne, NY*

18.3S Retiming and Recycling for Elastic Systems with Early Evaluation
Dmitry E. Bufistov, Jordi Cortadella, Marc Galceran-Oms - *Univ. Politècnica de Catalunya, Barcelona, Spain*
Jorge Júlvez - *Univ. de Zaragoza, Zaragoza, Spain*
Michael Kishinevsky - *Intel Corp., Hillsboro, OR*

18.4S Speculation in Elastic Systems
Marc Galceran-Oms, Jordi Cortadella - *Univ. Politècnica de Catalunya, Barcelona, Spain*
Michael Kishinevsky - *Intel Corp., Hillsboro, OR*

Technical Sessions

Wednesday, July 29, 9:00 - 11:00am

Rm: 131

19 PANEL: DFM - BAND-AID OR COMPETITIVE WEAPON?

Topic Area: DFM and the Manufacturing Interface

Chair: Joe Sawicki - *Mentor Graphics Corp., Wilsonville, OR*
Organizers: Gene Forte - *Mentor Graphics Corp., Wilsonville, OR*
Nagaraj NS - *Texas Instruments, Inc., Dallas, TX*

The external specifications of an IC (functions, clock rate, power consumption) determine the competitiveness of a product. To be successful and profitable in the IC business, designers need to "out-design" their competitors. Usually, Design for Manufacturing (DFM) is discussed as a yield improvement strategy. But what is the value of DFM from a competitive point of view? Can DFM give designers a competitive "lever" by telling them how far they can push a design without creating a manufacturing disaster? Can DFM be used to optimize designs rather than just to identify hot spots?

Items to be discussed include:
- Rules versus modeling: it's not just a methodology debate
- Physical signoff as a spectrum of business goals from avoiding disaster to gaining a competitive advantage
- Whether RDRs help or hinder competitive advantage
- Whether DFM and PV can ensure a parametric yield envelope to aid competition
- Design-to-fab flow as a total quality management process

Speakers: **Mark Redford** - *Cambridge Silicon Radio, Cambridge, United Kingdom*
Kimon Michaels - *PDF Solutions, Inc., San Jose, CA*
Cliff Hou - *Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan*
Yervant Zorian - *Virage Logic Corp., Fremont, CA*
Prasad Subrmaniam - *eSilicon Corp., Murray Hill, NJ*

Rm: 133

20 SPECIAL SESSION: EMERGING TECHNOLOGIES: BLUE-SKY RESEARCH OR CMOS REPLACEMENT?

Topic Area: New and Emerging Technologies

Chair: Kaustav Banerjee - *Univ. of California, Santa Barbara, CA*
Organizer: Igor L. Markov - *Univ. of Michigan, Ann Arbor, MI*

Nanoelectronics has captivated the imagination of many researchers in VLSI and design automation, but few success stories emerged until now. In the meantime, downscaling mass-produced CMOS devices is becoming increasingly difficult and expensive. The spread between what's currently achievable with nanoelectronics and what is hoped for in the near future raises many questions. What is the state of the art in carbon nanotubes and single-electron transistors? Where will nanoelectronics research be heading tomorrow? How competitive will CMOS at the 32nm and 22nm nodes be?

20.1 The Semiconductor Industry's Nanoelectronics Research Initiative: Motivation and Challenges
Jeff Welser - *IBM Corp. and Semiconductor Research Corp., San Jose, CA*

20.2 Single-Electron Devices for Ubiquitous and Secured Computing Applications
Ken Uchida - *Tokyo Institute of Technology, Tokyo, Japan*

20.3 Digital VLSI Logic Technology Using Carbon Nanotube FETs: Frequently Asked Questions
Nishant Patil, Albert Lin, Jie Zhang, **H.-S. Philip Wong**, Subhasish Mitra - *Stanford Univ., Stanford, CA*

20.4 CMOS Scaling Beyond 32nm: Challenges and Opportunities
Kelin J. Kuhn - *Intel Corp., Hillsboro, OR*

Rm: 123

21 ROUTING: FROM CHIP TO PACKAGE

Topic Area: Physical Design

Chair: Tong Gao - *Synopsys, Inc., Mountain View, CA*

This session advances state of the art in routing from chip-level to package/board codesign. The first paper proposes an elegant O(n log n) algorithm for obstacle-avoiding rectilinear Steiner tree construction. The second paper presents GRIP, a scalable ILP based global router. The next three papers deal with PCB and package-board routing. The third paper deals with automatic bus planning for dense PCBs, where manual design could take a couple of months. The fourth paper proposes a new network-flow model for escape routing, and the fifth paper combines flip-chip routing with I/O pad planning for package-board codesign.

21.1 An O(n log n) Path-Based Obstacle-Avoiding Algorithm for Rectilinear Steiner Tree Construction
Chih-Hung Liu, Sy-Yen Kuo, Yao-Hsin Chou - *National Taiwan Univ., Taipai, Taiwan*
Shin-Yi Yuan - *Feng Chia Univ., Taichung, Taiwan*

21.2 GRIP: Scalable 3-D Global Routing using Integer Programming
Tai-Hsuan Wu, **Azadeh Davoodi**, Jeffery T. Linderoth - *Univ. of Wisconsin, Madison, WI*

21.3 Automatic Bus Planner for Dense PCBs
Hui Kong, Tan Yan, Martin D. F. Wong - *Univ. of Illinois, Urbana-Champaign, Urbana, IL*

21.4S A Correct Network-Flow Model for Escape Routing
Tan Yan, Martin D. F. Wong - *Univ. of Illinois, Urbana-Champaign, Urbana, IL*

21.5S Flip-Chip Routing with Unified Area-I/O Pad Assignments for Package-Board Codesign
Jia-Wei Fang, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*
Martin D. F. Wong - *Univ. of Illinois, Urbana-Champaign, Urbana, IL*

S - denotes a short paper | Orange titles signify a best paper candidate

Rm: 130

22 SPEED PATH IDENTIFICATION AND SILICON DEBUG

Topic Area: Verification and Test

Chair: Tom Williams - *Synopsys, Inc., Broomfield, CO*

Identifying the speed paths for at-speed testing is critical for optimizing the pattern count without compromising defect coverage. The first two papers present a multi-layer process space coverage metric for speed path selection and a data mining approach that analyzes a small number of identified speed paths against a large number of non-speed paths. The last two papers address design debugging in silicon by improving real-time observability using new techniques for interconnection fabric and online state dumping.

22.1 Statistical Multi-Layer Process Space Coverage for At-Speed Test
Jinjun Xiong, Vladimir Zolotov, Chandu Visweswariah - *IBM Corp., Yorktown Hts., NY*
Yiyu Shi - *Univ. of California, Los Angeles, CA*

22.2 Speedpath Analysis Based on Hypothesis Pruning and Ranking
Nicholas Callegari, Li-C. Wang - *Univ. of California, Santa Barbara, CA*
Pouria Bastani - *Intel Corp., Hillsboro, OR*

22.3 Interconnection Fabric Design for Tracing Signals in Post-Silicon Validation
Xiao Liu, Qiang Xu - *The Chinese Univ. of Hong Kong, Shatin, Hong Kong*

22.4 Online Cache State Dumping for Processor Debug
Anant Vishnoi, Preeti Ranjan Panda, M. Balakrishnan - *Indian Institute of Technology, New Delhi, India*

Rm: 125

23 ANALOG/RF SIMULATION AND STATISTICAL MODELING

Topic Area: Analog/Mixed-Signal/RF Design

Chair: Jaijeet Roychowdhury - *Univ. of California, Berkeley, CA*

Advances in analog design and modeling are the focus of this session. The first paper in the session adopts the least angle regression technique from statistics to extract a large-scale performance model from a small set of samples. The second paper presents an in-depth analysis of using a direct solver as opposed to preconditioned iterative solvers in harmonic balance analysis. The third paper proposes stochastic, linear AC analysis for mixed-signal systems including bang-bang PLLs leveraging Markov-chain analysis. The fourth paper adopts an explicit telescopic projective numerical integration method for efficient, parallelizable circuit simulations. The last paper proposes an algorithm for efficient worst-case corner extraction based on a convex semi-definite programming formulation.

23.1 Finding Deterministic Solution from Underdetermined Equation: Large-Scale Performance Modeling by Least Angle Regression
Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*

23.2 A Robust and Efficient Harmonic Balance (HB) Using Direct Solution of HB Jacobian
Amit Mehrotra - *Berkeley Design Automation, Santa Clara, CA*
Abhishek Somani - *Berkeley Design Automation, Bangalore, India*

23.3 Stochastic Steady-State and AC Analyses of Mixed-Signal Systems
Jaeha Kim, Mark A. Horowitz - *Stanford Univ., Stanford, CA*
Jihong Ren - *Rambus, Inc., Los Altos, CA*

23.4S Parallelizable Stable Explicit Numerical Integration for Efficient Circuit Simulation
Wei Dong, Peng Li - *Texas A&M Univ., College Station, TX*

23.5S Efficient Design-Specific Worst-Case Corner Extraction for Integrated Circuits
Hong Zhang, Tsung-Hao Chen, Ming-Yuan Ting - *Mentor Graphics Corp., San Jose, CA*
Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*

Rm: 124

24 RECENT ADVANCES IN TIMING, ECO AND LOGIC OPTIMIZATION

Topic Area: Synthesis and FPGA

Chair: Jie-Hong Roland Jiang - *National Taiwan Univ., Taipei, Taiwan*

This session presents recent advances in logic synthesis. The first paper discusses a function-based, timing-driven optimization technique for synthesizing multilevel logic circuits. The second paper presents a SAT-based Boolean matching for large circuits. The third and the fourth papers present new ideas for the engineering change order problem. The third paper presents new spare cell structure for IR drop minimization while the fourth paper presents spare cell selection for reduced routing cost. The final paper uses high-level don't-cares to reduce initialized registers.

24.1 Timing-Driven Optimization Using Lookahead Logic Circuits
Mihir Choudhury, Kartik Mohanram - *Rice Univ., Houston, TX*

24.2 Simulation and SAT-Based Boolean Matching for Large Boolean Networks
Kuo-Hua Wang, Chung-Ming Chan, Jung-Chang Liu - *Fu Jen Catholic Univ., Taipei, Taiwan*

24.3 New Spare Cell Design for IR Drop Minimization in Engineering Change Order
Hsien-Te Chen, Chieh-Chun Chang, TingTing Hwang - *National Tsing-Hua Univ., Hsinchu, Taiwan*

24.4S Matching-Based Minimum-Cost Spare Cell Selection for Design Changes
Iris Hui-Ru Jiang, Liang-Gi Chang, Huang-Bi Hung - *National Chaio Tung Univ., Hsinchu, Taiwan*
Hua-Yu Chang - *Consultant, Taipei, Taiwan*

24.5S Handling Don't-Care Conditions in High-Level Synthesis and Application for Reducing Initialized Registers
Hong-Zu Chou, Sy-Yen Kuo - *National Taiwan Univ., Taipei, Taiwan*
Kai-Hui Chang - *Avery Design Systems, Inc., Andover, MA*

Technical Sessions

Wednesday, July 29, 2:00 - 4:00pm

Rm: 131

25 PANEL: OIL FIELDS, HEDGE FUNDS AND DRUGS

Topic Area: Interconnect and Reliability

Chair: Patrick Groeneveld - *Magma Design Automation, Inc., San Jose, CA*
Organizer: Andreas Kuehlmann - *Cadence Design Systems, Inc., Berkeley, CA*

Statistical analysis is a fundamental method in analysis, design, and optimization of large systems with uncertainties. It is being applied in drug development, analyzing financial markets, search for new oil fields, and many more areas. As the silicon process technology scales to its limits, uncertainty plays an increasing role and has made its way into tools such as yield analysis, statistical time analysis, etc. In this educational panel, we will start with a short tutorial on Monte Carlo methods including their use in EDA.

Three experts from distinct application fields will then follow and discuss their experience in using Monte Carlo methods for solving large-scale problems in their domain. It may come as a surprise to some attendees of DAC to learn how much commonality there is between methods used in EDA and other field that seem far-fetched.

Speakers: **Rob A. Rutenbar** - *Carnegie Mellon Univ., Pittsburgh, PA*
Erik Carlson - *Armored Wolf, LLC, Aliso Viejo, CA*
Jed Pitera - *IBM Corp., San Jose, CA*
Jinsong Chen - *Lawrence Berkeley National Lab, Berkeley, CA*

Rm: 133

26 SPECIAL SESSION: COMPUTATION IN THE POST-TURING ERA

Topic Area: New and Emerging Technologies

Chair: Todd Austin - *Univ. of Michigan, Ann Arbor, MI*
Organizer: Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

Traditional instruction-based computing is running out of steam. This is probably best evidenced by the end of instruction-level parallelism in processor designs and the quick transition to multicore computing, whose performance potential is yet to be realized. One possible future for computing is to turn to alternative computational models as a means to create new computing value and capabilities. For example, neural-inspired architectures have been shown to perform vision and recognition tasks more efficiently and with less power than traditional architectures. Stochastic computation breaks the traditional limits of energy-efficiency and performance through the combination of digital signal processing techniques and algorithmic-level error-tolerance. Human computation incorporates humans in the computation flow to solve very difficult problems in clever ways.

However, the field today is, as a whole, bound to Turing-style computational frameworks; these alternative computational models are a promising approach to achieving added value in tomorrow's computing systems, but they require new thinking in design, tools and even education. This special session will serve to inform and inspire the DAC community about some new ideas in alternative computational models through renowned speakers and lead investigators in these exciting new areas. Their presentations will be followed by an interactive panel discussion.

26.1 Statistical Computing: An Alternative Road to Low Energy
Jan Rabaey - *Univ. of California, Berkeley, CA*

26.2 Human Computation
Luis von Ahn - *Carnegie Mellon Univ., Pittsburgh, PA*

26.3 How to Make Computers That Work Like the Brain
Dileep George - *Numenta, Inc., Menlo Park, CA*

Rm: 123

27 ADVANCES IN PHYSICAL SYNTHESIS

Topic Area: Physical Design

Chair: Martin D. F. Wong - *Univ. of Illinois, Urbana-Champaign, Urbana, IL*

This session focuses on new placement and buffering algorithms. In the first presentation, a provably good approximation algorithm is proposed for buffering. Then, a multilevel analytical placement framework is presented, which predicts and considers spare cell requirements. The third presentation combines floorplanning and placement techniques to handle complexities of large-scale mixed-size placement problems. In the last presentation, a placement algorithm based on virtual platform generation is described for structured ASICs.

27.1 A Fully Polynomial Time Approximation Scheme for Timing Driven Minimum Cost Buffer Insertion
Shiyan Hu - *Michigan Technological Univ., Houghton, MI*
Zhuo Li, Charles J. Alpert - *IBM Corp., Austin, TX*

27.2 Spare-Cell-Aware Multilevel Analytical Placement
Zhe-Wei Jiang, Meng-Kai Hsu, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*
Kai-Yuan Chao - *Intel Corp., Hillsboro, OR*

27.3 Handling Complexities in Modern Large-Scale Mixed-Size Placement
Jackey Z. Yan, Natarajan Viswanathan, Chris Chu - *Iowa State Univ., Ames, IA*

27.4 RegPlace: A High Quality Placement Framework for Structured ASICs
Ashutosh Chakraborty, Anurag Kumar, David Z. Pan - *Univ. of Texas, Austin, TX*

Rm: 130

28 JUMPING THE HIGH-LEVEL VERIFICATION HURDLE

Topic Area: Verification and Test

Chair: Somdipta Basu Roy - *Texas Instruments, Inc., Dallas , TX*

With increasing complexity of designs, the verification problem at lower levels of abstraction gets progressively harder. One way to cope with this problem is to raise the level of abstraction by considering design at higher levels. In this session, new methods and methodologies are presented to more efficiently verify complex designs. The first paper focuses on a novel white-box technique to uncover out-of-order device-under-verification (DUV) behaviors. That proper selection of modeling language and abstraction level can make the same code useful for both formal and simulation-based techniques is the central focus for the second paper. The third paper advances the research in sequential equivalence checking of RTL models versus the system level, while the last paper in the session is dedicated to equivalence checking of programs.

28.1 A Novel Verification Technique to Uncover Out-Of-Order DUV Behaviors
Gabriel Marcilio, **Luiz C. V. Santos** - *Univ. Federal de Santa Catarina, Florianopolis, Brazil*
Sandro Rigo, Bruno Albertini - *Univ. Estadual de Campinas, Campinas, Brazil*

28.2 Shortening the Verification Cycle with Synthesizable Abstract Models
Alon Gluska, Lior Libis - *Intel Corp., Haifa, Israel*

28.3 Non-Cycle-Accurate Sequential Equivalence Checking
Pankaj P. Chauhan, Deepak Goyal, Gagan Hasteer, Anmol Mathur, Nikhil Sharma - *Calypto Design Systems, Inc., Santa Clara, CA*

28.4 Regression Verification
Benny Godlin, **Ofer Strichman** - *Technion - Israel Institute of Technology, Haifa, Israel*

Rm: 125

29 THERMAL OPTIMIZATION

Topic Area: Low-Power Design

Chair: Robert P. Dick - *Univ. of Michigan, Ann Arbor, MI*

This session deals with thermal issues for VLSI circuit and microarchitectural design. The first two papers present temperature estimation under noisy thermal sensors or with limited sensor data. The third paper presents novel techniques for thermal management via architectural adaptation. The last paper presents an online dynamic voltage scaling technique for energy optimization under thermal constraints.

29.1 Accurate Temperature Estimation Using Noisy Thermal Sensors
Yufu Zhang, Ankur Srivastava - *Univ. of Maryland, College Park, MD*

29.2 Spectral Techniques for High-Resolution Thermal Characterization with Limited Sensor Data
Ryan Cochran, Sherief Reda - *Brown Univ., Providence, RI*

29.3 Dynamic Thermal Management via Architectural Adaptation
Ramkumar Jayaseelan, **Tulika Mitra** - *National Univ. of Singapore, Singapore*

29.4 Online Thermal Aware Dynamic Voltage Scaling for Energy Optimization with Frequency/Temperature Dependency Consideration
Min Bao, Petru Eles, Zebo Peng - *Linköping Univ., Linkoping, Sweden*
Alexandru Andrei - *Ericsson, Linkoping, Sweden*

Rm: 124

30 NOVEL TECHNIQUES TO MINIMIZE CIRCUIT FAILURE

Topic Area: Interconnect and Reliability

Chair: Frank Liu - *IBM Corp., Austin, TX*

Circuit failure rate dramatically increases with the scaling of CMOS technology. Efficient and accurate analysis techniques are essential to predict the failure rate and protect the design quality. This session presents four papers that contribute to circuit reliability. The first paper proposes a piecewise modeling solution that accurately predicts SRAM performance variability, with >10K speed-up as compared to traditional approaches. The following two papers present optimization techniques of logic circuits in order to enhance their resilience under soft errors. The third paper further improves circuit testability in reliable design. The final paper concludes this session with a hierarchical framework for statistical aging analysis.

30.1 SRAM Parametric Failure Analysis
Jian Wang - *PDF Solutions, Inc., San Jose, CA*
Soner Yaldiz, Xin Li, Lawrence T. Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*

30.2 Soft Error Optimization of Standard Cell Circuits Based on Gate Sizing and Multi-Objective Genetic Algorithm
Weiguang Sheng, Liyi Xiao, Zhigang Mao - *Harbin Institute of Technology, Harbin, China*

30.3 Improving Testability and Soft-Error Resilience Through Retiming
Smita Krishnaswamy - *IBM Corp., Yorktown Hts., NY*
Igor L. Markov, John P. Hayes - *Univ. of Michigan, Ann Arbor, MI*

30.4 Statistical Reliability Analysis under Process Variation and Aging Effects
Yinghai Lu, Hengliang Zhu, Fan Yang, Xuan Zeng - *Fudan Univ., Shanghai, China*
Li Shang - *Univ. of Colorado, Boulder, CO*
Hai Zhou - *Fudan Univ., Shanghai, China and Northwestern Univ., Evanston, IL*

Rm: 131

31 PANEL: GUESS, SOLDER, MEASURE, REPEAT – HOW DO I GET MY MIXED-SIGNAL CHIP RIGHT?

Topic Area: Analog/Mixed-Signal/RF Design

Chair: Ken Kundert - *Designer's Guide Consulting, Los Altos, CA*
Organizers: Andreas Kuehlmann - *Cadence Design Systems, Inc., Berkeley, CA*
Geoffrey Ying - *Synopsys, Inc., Mountain View, CA*,

Over the past 20 years, EDA has developed a solid digital implementation methodology that combines some restrictions on the design style with a set of comprehensive tools leading to well predictable design flows. The recent increased use of analog components in complex SOC designs triggered a set of verification challenges ranging from simple connectivity problems to complex interferences between analog and digital data blocks. This panel discusses the state of affairs in analog-mixed signal verification and draws a picture of future directions in terms of new approaches and tools.

Speakers: **Georges Gielen** - *Katholieke Univ. Leuven, Leuven, Belgium*
Martin O'Leary - *Cadence Design Systems, Inc., San Jose, CA*
Eric Grimme - *Intel Corp., Hillsboro, OR*
Sandeep Tare - *Texas Instruments, Inc., Dallas, TX*
Warren Wong - *Synopsys, Inc., Mountain View, CA*

Rm: 133

32 SPECIAL SESSION: MULTICORE COMPUTING AND EDA

Topic Area: System-Level and Embedded

Chair: Bill Swartz - *InternetCAD, Dallas, TX*
Organizer: Patrick H. Madden - *Binghamton Univ., Binghamton, NY*

Parallel computing has exploded in the past few years, coming in both multicore versions of conventional processors, and in the form of general purpose variants of graphics processing units. There is considerable interest in ways to harness these resources effectively. Barring the way to broad acceptance are a lack of software tools and training and more importantly, Amdahl's law. This session features three speakers who have extensive experience and a broad perspective. We will explore advances in concurrent programming, learn about clarity in performance claims in parallel computations and explore programming metaphors for parallel computation.

32.1 **The Cilk++ Concurrency Platform**
Charles E. Leiserson - *Massachusetts Institute of Technology, Cambridge, MA*

32.2 **Misleading Performance Claims in Parallel Computations**
David H. Bailey - *Lawrence Berkeley National Lab, Berkeley, CA*

32.3 **Massively Parallel Processing: It's Déjà vu All Over Again**
Steven P. Levitan, Donald M. Chiarulli - *Univ. of Pittsburgh, Pittsburgh, PA*

Rm: 123

33 LAYOUT-BASED VARIABILITY MODELING AND OPTIMIZATION

Topic Area: DFM and the Manufacturing Interface

Chair: Sherief Reda - *Brown Univ., Providence, RI*

The papers in this session discuss modeling and handling of layout-based variability. The first paper is an elegant optimization scheme for CMP dummy fill. The second paper is on modeling lithography-induced variability. The third paper is about analyzing the impact of variability induced by rapid thermal annealin on the layout.

33.1 **Provably Good and Practically Efficient Algorithms for CMP Dummy Fill**
Chunyang Feng, Changhao Yan, Jun Tao, Xuan Zeng - *Fudan Univ., Shanghai, China*
Hai Zhou - *Fudan Univ., Shanghai, China and Northwestern Univ., Evanston, IL*

33.2 **Predicting Variability in Nanoscale Lithography Processes**
Dragoljub Drmanac - *Univ. of California, Santa Barbara, CA*
Frank Liu - *IBM Corp., Austin, TX*
Li-C. Wang - *Univ. of California, Santa Barbara, CA*

33.3 **Variability Analysis under Layout Pattern-Dependent Rapid-Thermal Annealing Process**
Frank Liu - *IBM Corp., Austin, TX*
Yun Ye, Yu (Kevin) Cao - *Arizona State Univ., Tempe, AZ*

Rm: 130

34 ADVANCES IN CORE VERIFICATION TECHNIQUES

Topic Area: Verification and Test

Chair: Gila Kamhi - *Intel Corp., Haifa, Israel*

This session addresses a wide spectrum of verification technology advances. The first paper achieves significant speedup of event-driven simulation with general purpose CPUs. The second paper explores the use of a SAT solver on negation normal form, as opposed to the classical conjunctive normal form. The third paper discusses abstraction refinement-based model checking.

34.1 Event-Driven Gate-Level Simulation with GP-GPUs
Debapriya Chatterjee, Andrew DeOrio, Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

34.2 Efficient SAT Solving for Non-Clausal Formulas Using DPLL, Graphs, and Watched Cuts
Himanshu Jain - *Synopsys, Inc., Hillsboro, OR*
Edmund Clarke - *Carnegie Mellon Univ., Pittsburgh, PA*

34.3 Constraints in One-To-Many Concretization for Abstraction Refinement
Kuntal Nanshi, Fabio Somenzi - *Univ. of Colorado, Boulder, CO*

Rm: 125

35 FUTURE INTERCONNECT TECHNOLOGIES: HOW DO ON-CHIP NETWORKS EVOLVE?

Topic Area: System-Level and Embedded

Chair: Joerg Henkel - *Univ. Karlsruhe, Karlsruhe, Germany*

3-D and optical interconnect technologies are fast becoming a reality. The greatest impact of these technologies will be on Networks-on-Chip; this session examines three differing methods to exploit and adapt to them. The first paper proposes a novel hybrid optical and electrical network. Serial vertical interconnects are explored in the second paper, while the third paper proposes a ring-based interconnect network for 3-D chips and explores its use in multicore processors.

35.1 Spectrum: A Hybrid Nanophotonic-Electric On-Chip Network
Zheng Li, Yihe Sun - *Tsinghua Univ., Beijing, China*
Daniel Fay, Alan Mickelson, **Li Shang**, Manish Vachharajani, Dejan Filipovic, Wounjhang Park - *Univ. of Colorado, Boulder, CO*

35.2 Exploring Serial Vertical Interconnects for 3-D ICs
Sudeep Pasricha - *Colorado State Univ., Fort Collins, CO*

35.3 No Cache-Coherence: A Single-Cycle Ring Interconnection for Multicore L1-NUCA Sharing on 3-D Chips
Shu-Hsuan Chou, Chien-Chih Chen, Chi-Neng Wen, Yi-Chao Chan, Tien-Fu Chen,
Chao-Ching Wang, Jinn-Shyan Wang - *National Chung Cheng Univ., Chia-Yi, Taiwan*

Rm: 124

36 ROBUST ANALOG SYSTEM DESIGN

Topic Area: Analog/Mixed-Signal/RF Design

Chair: Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*

This session hosts a series of papers on constructing robust analog systems. The first paper addresses the placement problem of analog blocks on a chip in order to enhance device matching with respect to thermal effects. The second paper presents an equation-based yield optimization technique that iteratively refines the constraint space due to variabilities. The last paper proposes the adoption of assume-guarantee contracts for a hierarchical, correct-by-construction composition of analog systems.

36.1 Thermal-Driven Analog Placement Considering Device Matching
Po-Hung Lin, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*
Hongbo Zhang, Martin D. F. Wong - *Univ. of Illinois, Urbana-Champaign, Urbana, IL*

36.2 Yield-Driven Iterative Robust Circuit Optimization Algorithm
Yan Li, Vladimir M. Stojanovic - *Massachusetts Institute of Technology, Cambridge, MA*

36.3 Contract-Based System-Level Composition for Analog Circuits
Xuening Sun, Chang-Ching Wu, Pierluigi Nuzzo, Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

Technical Sessions

Thursday, July 30, 9:00 - 11:00am

Rm: 131

37 SPECIAL SESSION: WACI: WILD AND CRAZY IDEAS

Topic Area: New and Emerging Technologies

Chair: Ted Vucurevich - *Slightly Sharp Enterprises, Los Gatos, CA*
Organizer: Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

The WACI tradition continues: this session is packed with wild and crazy ideas intended to stimulate discussion. WACI papers present new ideas that are promising and thought-provoking, but not necessarily fully developed to the point of full papers. The presentations range from physical-level equalizations, to new models of Boolean computation. Also included are learning, neural and human computers and solutions to serve lazy designers. Cyber-physical connectivity will complete this wild and crazy session. We count on you, once again, to ask the wild questions that make the WACIest question will be awarded a prize.

37.1 Serial Reconfigurable Mismatch-Tolerant Clock Distribution
Atanu Chattopadhyay, Zeljko Zilic - *McGill Univ., Montreal, QC, Canada*

37.2 Thermal-Aware Data Flow Analysis
Jose L. Ayala - *Complutense Univ. of Madrid, Madrid, Spain*
Philip Brisk, David Atienza - *Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland*

37.3 Nanoscale Digital Computation Through Percolation
Mustafa Altun, **Marc Riedel**, Claudia Neuhauser - *Univ. of Minnesota, Minneapolis, MN*

37.4 A Learning Digital Computer
Bo Marr, Arindam Basu, Stephen Brink, Paul Hasler - *Georgia Institute of Technology, Atlanta, GA*

37.5 Programmable Neural Processing on a Smartdust
Shimeng Huang, Joseph Oresko, Yuwen Sun, Allen C. Cheng - *Univ. of Pittsburgh, Pittsburgh, PA*

37.6 Human Computing for EDA
Andrew DeOrio, Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

37.7 Synthesizing Hardware from Sketches
Andreas Raabe - *International Computer Science Institute, Berkeley, CA*
Rastislav Bodik - *Univ. of California, Berkeley, CA*

37.8 Endosymbiotic Computing: Enabling Surrogate GUI and Cyber-Physical Connectivity
Pai H. Chou - *Univ. of California, Irvine, CA*

Rm: 133

38 SPECIAL SESSION: THE TOOL SHOWS THAT MY DESIGN IS WRONG, BUT WHERE IS THE BUG?

Topic Area: Verification and Test

Chair: Eli Singerman - *Intel Corp., Haifa, Israel*
Organizer: Rolf Drechsler - *Univ. Bremen, Bremen, Germany*

Today's verification tools have become very powerful by using and combining simulation and formal techniques. For equivalence checking, property checking and assertion-based methods, the tool usually returns a single failure trace. The user then has to locate the bug manually in a time-consuming debugging session. Thus, the major question is: where is the bug?

The session will address this question and discuss the state of the art:

- How to automate bug localization?
- How to handle multiple design errors?
- What are the right assumptions for modeling errors?
- What support do designers get from tools today?
- What is the best abstraction level to model erroneous behavior?
- Are verification and debugging separate tasks, or should they be unified?

This session is organized as six short papers followed by a half-hour interactive discussion with the speakers.

38.1 Debugging from High-Level Down to Gate Level
Masahiro Fujita, Yoshihisa Kojima, Amir Masoud Gharehbaghi - *Univ. of Tokyo and CREST, Japan*
Science and Technology, Tokyo, Japan

38.2 The Day Sherlock Holmes Decided to do EDA
Andreas Veneris - *Univ. of Toronto, Toronto, ON, Canada*
Sean Safarpour - *Vennsa Technologies, Inc., Toronto, ON, Canada*

38.3 Debugging Strategies for Mere Mortals
Valeria Bertacco - *Univ. of Michigan, Ann Arbor, MI*

38.4 MAGENTA: Transaction-Based Statistical Micro-Architectural Root-Cause Analysis
Gila Kamhi, Alexander Novakovsky, Andreas Tiemeyer, Adriana Wolffberg - *Intel Corp., Haifa, Israel*

38.5 Untwist Your Brain: Efficient Debugging and Diagnosis of Complex Assertions
Adriana Maggiore - *OneSpin Solutions, Sunnyvale, CA*
Michael Siegel, Christian Pichler - *OneSpin Solutions, Munich, Germany*

38.6 Beyond Verification: Leveraging Formal for Debugging
Rajeev K. Ranjan, Sebastian Skalberg - *Jasper Design Automation, Inc., Mountain View, CA*
Claudionor Coelho, Jr. - *Jasper Design Automation, Inc., Belo Horizonte, Brazil*

Rm: 123

39 EMBEDDED SYSTEM DESIGN FOR LOW POWER

Topic Area: Low-Power Design

Chair: Emrah Acar - *IBM Corp., Yorktown Hts., NY*

This session presents several new ideas to reduce power consumption in embedded systems. The first paper proposes a power model for OLED display systems which relies on the fact that different colors consume different amounts of power in OLED devices. The second paper shows how reducing the number of 01 and 10 bit-patterns is important to reduce power in error control code. PRAM and DRAM can be nicely combined, taking advantages of both to reduce power of memory systems, as discussed in the third paper. The final paper in the session discusses a power-efficient memory system for MPEG-4 processors which combines 6T- and 8T-SRAM cells, each type used to store different luma bits.

39.1 Power Modeling of Graphical User Interfaces on OLED Displays
Mian Dong, Yung-Seok Kevin Choi, Lin Zhong - *Rice Univ., Houston, TX*

39.2 Energy-Aware Error Control Coding for Flash Memories
Veera Papirla, Chaitali Chakrabarti - *Arizona State Univ., Tempe, AZ*

39.3 PDRAM: A Hybrid PRAM and DRAM Main Memory System
Gaurav Dhiman, Raid Ayoub, **Tajana Rosing** - *Univ. of California, San Diego, La Jolla, CA*

39.4 A Voltage-Scalable and Process Variation Resilient Hybrid SRAM Architecture for MPEG-4 Video Processors
Ik Joon Chang, **Debabrata Mohapatra**, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

S - denotes a short paper | **Orange titles** signify a best paper candidate

Rm: 130

40 HARDWARE AUTHENTICATION, CHARACTERIZATION AND TRUSTED DESIGN

Topic Area: System-Level and Embedded

Chair: Lin Yuan - *Synopsys, Inc., Mountain View, CA*

This session presents emerging design tools and methods for ensuring hardware authentication, characterization and trust. Since microelectronics forms the kernel of industries, businesses, and governments in the modern world, hardware protection and trust is of increasing importance. The first paper employs the on-chip power distribution system for creation of new physically unclonable functions. The second paper proposes a new time-bounded microprocessor authentication. The next paper employs the noninvasive chip characterization for creation of new hardware Trojan detectors. The fourth paper proposes an advanced framework for microprocessor characterization. The last paper discusses new trusted system design methods by constraint manipulation.

40.1 A Physical Unclonable Function Defined Using Power Distribution System Equivalent Resistance Variations
Ryan Helinski, James F. Plusquellic - *Univ. of New Mexico, Albuquerque, NM*
Dhruva Acharyya - *Verigy Ltd., Cupertino, CA*

40.2 Hardware Authentication Leveraging Performance Limits in Detailed Simulations and Emulations
Daniel Y. Deng, G. Edward Suh - *Cornell Univ., Ithaca, NY*
Andrew H. Chan - *Univ. of California, Berkeley, CA*

40.3 Hardware Trojan Horse Detection Using Gate-Level Characterization
Miodrag Potkonjak, **Ani Nahapetian**, Michael Nelson, Tammara Massey - *Univ. of California, Los Angeles, CA*

40.4S Process Variation Characterization of Chip-Level Multiprocessors
Lide Zhang, Russ Joseph - *Northwestern Univ., Evanston, IL*
Lan S. Bai, Robert P. Dick - *Univ. of Michigan, Ann Arbor, MI*
Li Shang - *Univ. of Colorado, Boulder, CO*

40.5S Information Hiding for Trusted System Design
Junjun Gu, Gang Qu - *Univ. of Maryland, College Park, MD*
Qiang Zhou - *Tsinghua Univ., Beijing, China*

Rm: 125

41 TARGETED TEST AND DIAGNOSIS

Topic Area: Verification and Test

Chair: Subhasish Mitra - *Stanford Univ., Stanford, CA*

The importance of targeting the right faults with the appropriate test method is the focus of this session. Advances in improved targeting methods for a range of test topics, such as digital test generator, IC diagnosis, embedded DRAM BIST and RF testing are presented. The first paper develops fault and wear-out models for embedded DRAM BIST. The second develops a method to validate diagnosis techniques through realistic failure model development. The third paper works at bridging the gap between functional and structural tests through better identification of illegal states. Finally, the fourth paper proposes a method for improving the efficiency of RF testing by adaptively changing the set of applied tests.

41.1 On Systematic Illegal State Identification for Pseudo-Functional Testing
Feng Yuan, Qiang Xu - *The Chinese Univ. of Hong Kong, Shatin, Hong Kong*

41.2 Automated Failure Population Creation for Validating Integrated Circuit Diagnosis Methods
Wing Chiu Tam, Osei Poku, R.D. Shawn Blanton - *Carnegie Mellon Univ., Pittsburgh, PA*

41.3 Fault Models and Testing Strategies for Embedded-DRAM Macros
Mango C.-T. Chao, **Hao-Yu Yang,** Ching-Yu Chin - *National Chaio Tung Univ., Hsinchu, Taiwan*
Rei-Fu Huang - *MediaTek, Inc., Hsinchu, Taiwan*
Shih-Chin Lin - *United Microelectronics Corp., Hsinchu, Taiwan*

41.4 Adaptive Test Elimination for Analog/RF Circuits
Ender Yilmaz, Sule Ozev - *Arizona State Univ., Tempe, AZ*

Rm: 124

42 CHALLENGES OF MEMORY-AWARE DESIGN FOR EMBEDDED SYSTEMS

Topic Area: System-Level and Embedded

Chair: Joerg Henkel - *Univ. Karlsruhe, Karlsruhe, Germany*

This session presents new results in designing memory systems for embedded sub-systems related to execution time and space problems. Two papers consider the influence of register allocation techniques on the WCET of programs and the reduction of WCET through proper allocation of scratchpads. Another paper addresses the problem of memory limitations of dynamic binary translators that are frequently used for purposes of power management and virtualization. A heterogeneous code cache is introduced here that exploits a split of a code cache into scratchpad and main memory. Finally, the fourth paper presents a new real-time compression technique used for compression of program execution traces at runtime in hardware.

42.1 WCET-Aware Register Allocation Based on Graph Coloring
Heiko Falk - *Technische Univ. Dortmund, Dortmund, Germany*

42.2 Optimal Static WCET-Aware Scratchpad Allocation
Heiko Falk, Jan C. Kleinsorge - *Technische Univ. Dortmund, Dortmund, Germany*

42.3 A Real-Time Program Trace Compressor Utilizing Double Move-To-Front Method
Vladimir Uzelac, Aleksandar Milenkovic - *Univ. of Alabama, Huntsville, AL*

42.4 Heterogeneous Code Cache: Using Scratchpad and Main Memory in Dynamic Binary Translators
Jose A. Baiocchi, Bruce R. Childers - *Univ. of Pittsburgh, Pittsburgh, PA*

Technical Sessions

Thursday, July 30, 2:00 - 4:00pm

Rm: 131

43 PANEL: FROM MILLIWATTS TO MEGAWATTS: THE SYSTEM-LEVEL POWER CHALLENGE

Topic Area: System-Level and Embedded

Chair: Atul Sharan - *AutoESL Design Technologies, Inc., Cupertino, CA*
Organizer: Ruchir Puri - *IBM Corp., Yorktown Hts., NY*

This panel discusses power optimization at the system level. What are the needs and opportunities? What are examples of successful practices? Can system-level power optimization ever be automated? Will power optimization be the compelling event for a methodology change in system-level design?

Speakers: **John Shen** - *Nokia, Palo Alto, CA*
Bradley McCredie - *IBM Corp., Austin, TX*
Andres Takach - *Mentor Graphics Corp., Wilsonville, OR*
Jason Cong - *Univ. of California, Los Angeles, CA*
Johannes Stahl - *CoWare, Inc., Aachen, Germany*

Rm: 133

44 PARASITIC EXTRACTION IN THE FACE OF PROCESS VARIABILITY

Topic Area: Interconnect and Reliability

Chair: Zhenhai Zhu - *Cadence Design Systems, Inc., Berkeley, CA*

This session covers field solving techniques for extracting parasitic models of on-chip interconnect structures. The first paper discusses a fast direct matrix solution technique for integral equation-based solvers. The remaining papers deal with variability. Paper two describes a technique based on a continuous surface model for rapidly evaluating the effects of random variations on interconnect capacitance. The third paper deals with stochastic variations by using "geometrical moments" and parallel processing. The final paper in the session applies finite element analysis and adjoint sensitivity techniques to the problem of on-chip resistance extraction with geometric variation.

44.1 A Direct Integral-Equation Solver of Linear Complexity for Large-Scale 3-D and Impedance Extraction
Wenwen Chai, Dan Jiao, Cheng-Kok Koh - *Purdue Univ., West Lafayette, IN*

44.2 Variational Capacitance Extraction of On-Chip Interconnects Based on Continuous Surface Model
Wenjian Yu, Chao Hu, Wangyang Zhang - *Tsinghua Univ., Beijing, China*

44.3 PiCAP: A Parallel and Incremental Capacitance Extraction Considering Stochastic Process Variation
Fang Gong, Lei He - *Univ. of California, Los Angeles, CA*
Hao Yu - *Berkeley Design Automation, Santa Clara, CA*

44.4 An Efficient Resistance Sensitivity Extraction Algorithm for Conductors of Arbitrary Shapes
Tarek A. El-Moselhy - *Massachusetts Institute of Technology, Cambridge, MA*
Abe Elfadel - *IBM Corp., Yorktown Hts., NY*
Bill Dewey - *IBM Corp., Hopewell Jct., NY*

Rm: 123

45 SCHEDULING, ALLOCATION AND RELIABILITY

Topic Area: Low-Power Design

Chair: Gus Palau - *Texas Instruments, Inc., Dallas, TX*

This session has a range of selected papers covering some of the extra design challenges in today's power managed systems. The first paper looks at multicore task optimization with temperature sensitive leakage constraints. The next paper also covers adaptive scheduling of tasks, this time with voltage and frequency scaling to manage demand in a limited supply system. The third paper is on reliability management of large peak current induced voltage drops in clock or power gated systems. The final paper covers clock tree sizing and type assignment for power/ground noise minimization. This is important in power managed systems where there may be severe supply limitations.

45.1 Throughput Optimal Task Allocation under Thermal Constraints for Multicore Processors
Vinay Hanumaiah, Sarma Vrudhula, Karam S. Chatha - *Arizona State Univ., Tempe, AZ*
Ravishankar Rao - *Synopsys, Inc., Mountain View, CA*

45.2 An Adaptive Scheduling and Voltage/Frequency Selection Algorithm for Real-Time Energy Harvesting Systems
Shaobo Liu, Qing Wu, Qinru Qiu - *Binghamton Univ., Binghamton, NY*

45.3 Software-Assisted Hardware Reliability: Abstracting Circuit-Level Challenges to the Software Stack
Vijay Janapa Reddi, Meeta S. Gupta, Michael D. Smith, David Brooks, Gu-Yeon Wei - *Harvard Univ., Cambridge, MA*
Simone Campanoni - *Politecnico di Milano, Milano, Italy*

45.4 Simultaneous Clock Buffer Sizing and Polarity Assignment for Power/Ground Noise Minimization
Hochang Jang, **Taewhan Kim** - *Seoul National Univ., Seoul, Republic of Korea*

S - denotes a short paper | Orange titles signify a best paper candidate

Rm: 130

46 NETWORK-ON-CHIP ADVANCES FOR POWER, RELIABILITY AND THE MEMORY BOTTLENECK

Topic Area: System-Level and Embedded

Chair: Joerg Henkel - *Univ. Karlsruhe, Karlsruhe, Germany*

On-chip interconnects have a significant impact on the performance, power, and other characteristics of modern SOCs. This session presents advances in NOCs to improve reliability, memory system performance, and power. The first two papers address the memory bottleneck by enhancing the NOC to be SDRAM-friendly and utilizing transaction processors to enable computing in, or close to, memory. The third paper addresses how the NOC can operate reliably even in the presence of failures within its components. The last two papers focus on reducing power consumption through voltage-frequency islands, along with the limits imposed by technology scaling on such techniques.

46.1 An SDRAM-Aware Router for Networks-On-Chip
Wooyoung Jang, David Z. Pan - *Univ. of Texas, Austin, TX*

46.2 Multiprocessor System-On-Chip Designs with Active Memory Processors for Higher Memory Efficiency
Junhee Yoo, Kiyoung Choi - *Seoul National Univ., Seoul, Republic of Korea*
Sungjoo Yoo - *Pohang Univ. of Science and Technology, Pohang, Republic of Korea*

46.3 Vicis: A Reliable Network for Unreliable Silicon
David Fick, Andrew DeOrio, Jin Hu, Valeria Bertacco, David Blaauw, Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*

46.4S Technology-Driven Limits on DVFS Controllability of Multiple Voltage-Frequency Island Designs: A System-Level Perspective
Siddharth Garg, Diana Marculescu, Radu Marculescu - *Carnegie Mellon Univ., Pittsburgh, PA*
Umit Y. Ogras - *Intel Corp., Hillsboro, OR*

46.5S NOC Topology Synthesis for Supporting Shutdown of Voltage Islands in SOCs
Ciprian Seiculescu, Giovanni De Micheli - *Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland*
Srinivasan Murali - *iNoCs and Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland*
Luca Benini - *Univ. di Bologna, Bologna, Italy*

Rm: 125

47 LEVERAGING PARALLELISM IN FPGAs AND MULTICORE SYSTEMS

Topic Area: Synthesis and FPGA

Chair: Philip Brisk - *Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland*

This session covers a comprehensive array of topics focusing on hardware parallellism using FPGAs and multicore computing. The session starts with a paper presenting a novel two-tier coarse-grain reconfigurable architecture to reduce power and improve performance. The second paper shows how to accelerate a popular EDA algorithm by means of non-deterministic transactional parallel computing on multicore processors. The third paper studies how to estimate switching activity and reduce power on FPGAs during high-level synthesis. The fourth paper presents a practical application accelerating simulation of wireless systems using FPGAs. The session concludes with a presentation showing how FPGAs can be used in hardware accelerated parallel processing in the context of an industry standard bus architecture.

47.1 Hierarchical Reconfigurable Computing Arrays for Efficient CGRA-Based Embedded Systems
Yoonjin Kim, Rabi N. Mahapatra - *Texas A&M Univ., College Station, TX*

47.2 Multicore Parallel Min-Cost Flow Algorithm for CAD Applications
Yinghai Lu, Xuan Zeng - *Fudan Univ., Shanghai, China*
Hai Zhou - *Fudan Univ., Shanghai, China and Northwestern Univ., Evanston, IL*
Li Shang - *Univ. of Colorado, Boulder, CO*

47.3 FPGA-Targeted High-Level Binding Algorithm for Power and Area Reduction with Glitch-Estimation
Scott Cromar, Jaeho Lee, Deming Chen - *Univ. of Illinois, Urbana-Champaign, Urbana, IL*

47.4S FPGA-Based Accelerator for the Verification of Leading-Edge Wireless Systems
Amirhossein Alimohammad, Saeed Fouladi Fard, **Bruce Cockburn** - *Univ. of Alberta, Edmonton, AB, Canada*

47.5S Transmuting Coprocessors: Dynamic Loading of FPGA Coprocessors
Chen Huang, Frank Vahid - *Univ. of California, Riverside, CA*

Rm: 124

48 SPACE AND TIME MANAGEMENT IN EMBEDDED APPLICATIONS

Topic Area: System-Level and Embedded

Chair: Claudio Pinello - *United Technologies, Berkeley, CA*

This session presents new approaches to map data, code and communications in time and space for various embedded applications. The first paper proposes strategies for optimal performance and reliability in the mapping of data onto flash memories. The second paper improves the performance of applications in CMPs by combining data and code mapping. The third paper proposes an efficient method to derive schedules and controllers for embedded multi-mode control applications. In the fourth paper a new context-sensitive timing analysis is presented for more accurate timing prediction of Esterel programs. Multiple task-scheduling policies for communicating over the FlexRay bus to optimize the end-to-end timing metrics are presented in the fifth paper.

48.1 Dynamic Thread and Data Mapping for NOC Based CMPs
Mahmut Kandemir, Sai Prashanth Muralidhara - *Pennsylvania State Univ., University Park, PA*
Ozcan Ozturk - *Bilkent Univ., Ankara, Turkey*

48.2 A Commitment-Based Management Strategy for the Performance and Reliability Enhancement of Flash-Memory Storage Systems
Yuan-Hao Chang, Tei-Wei Kuo - *National Taiwan Univ., Taipei, Taiwan*

48.3 Quality-Driven Synthesis of Embedded Multi-Mode Control Systems
Soheil Samii, Petru Eles, Zebo Peng - *Linköping Univ., Linkoping, Sweden*
Anton Cervin - *Lund Univ., Lund, Sweden*

48.4S Context-Sensitive Timing Analysis of Esterel Programs
Lei Ju, Bach Khoa Huynh, Abhik Roychoudhury - *National Univ. of Singapore, Singapore*
Samarjit Chakraborty - *Technische Univ. München, Munich, Germany*

48.5S Scheduling the FlexRay Bus Using Optimization Techniques
Haibo Zeng, Paolo Giusto - *General Motors Corp., Palo Alto, CA*
Wei Zheng, Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*
Marco Di Natale - *Scuola Superiore Sant'Anna, Pisa, Italy*
Arkadeb Ghosal - *General Motors Corp., Warren, MI*

Rm: 131

49 PANEL: THE WILD WEST: CONQUEST OF COMPLEX HARDWARE-DEPENDENT SOFTWARE DESIGN

Topic Area: System-Level and Embedded

Chair: Wolfgang Rosenstiel - *Univ. of Tübingen, Tuebingen, Germany*
Organizers: Hiroyuki Yagi - *Sony Corp., Atsugi, Japan*
Eshel Haritan - *CoWare, Inc., San Jose, CA*

Embedded software design can be compared to the lawless Wild West. With no clear methodology and no standard multicore platform modeling environment, every company must improvise its own solution.

The problems facing embedded software users are becoming more complex since:

- Hardware platforms become very complicated with many heterogeneous processors, complicated memory structure and interconnect
- Multiple platform configurations and platform migrations drive an explosion of the number of versions that need to be developed/maintained/ported
- Processors are becoming very complicated and hard to program
- Semiconductor vendors cannot justify the investment required to provide a complete Hardware Abstraction Layer (HAL), RTOS, etc.
- It is hard to put together an embedded software development environment (platform model + HAL+ development tools)
- A very high level of speed and efficiency is required in software development

Speakers: **Jakob Engblom** - *Virtutech, Stockholm, Sweden*
Jason Andrews - *Cadence Design Systems, Inc., Arden Hills, MN*
Kees Vissers - *Xilinx, Inc., San Jose, CA*
Marc Serughetti - *CoWare, Inc., San Jose, CA*
Nobu Matsumoto - *Toshiba Corp., Kawasaki, Japan*

Rm: 133

50 SPECIAL SESSION: TECHNOLOGIES FOR GREEN DATA CENTERS

Topic Area: Green Technology

Chair: Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*
Organizer: Ricardo Bianchini - *Rutgers Univ., Piscataway, NJ*

This session will describe state of the art in computing, storage, and networking technologies as well as data center design and operation for different classes of industrial applications. The emphasis will be on (i) building blocks and architecture of future green data centers, and (ii) technical approaches for improving energy efficiency (and thereby, reducing total cost of ownership) of data centers while meeting thermal and power delivery constraints and service level agreements. A broad set of techniques to tackle main energy efficiency challenges will be discussed including: data center-level management algorithms; server chassis and processor-level power management; server placement and power/load balancing; virtualization and server consolidation; data compression and de-duplication; data centers-on-chip and fully disaggregated data center architectures; thermal and HVAC management; and power delivery and distribution issues. The emphasis will be on how our community can help tackle some of the key design and management challenges facing the current and next generation of data centers.

50.1 Internet-In-A-Box: Emulating Data Center Network Architectures Using FPGAs
Randy H. Katz, Jonathan D. Ellithorpe, Zhangxi Tan - *Univ. of California, Berkeley, CA*

50.2 Sustainable Data Centers: Enabled by Supply and Demand Side Management
Prith Banerjee, Chandrakant Patel, Cullen Bash, Parthasarathy Ranganathan - *Hewlett-Packard Co., Palo Alto, CA*

50.3 Green Data Centers and Hot Chips
Dilip D. Kandlur, Tom W. Keller - *IBM Corp., Austin, TX*

Rm: 123

51 HOW TO IMPROVE YOUR MEMORY

Topic Area: System-Level and Embedded

Chair: Peter Marwedel - *Technische Univ. Dortmund, Dortmund, Germany*

The footprint, power consumption, and performance of memories have a fundamental impact on the overall design of digital systems. The first presentation in this session shows how to remove the memory bottlenecks in a digital communications codec. The next talk discusses low-power optimization for instruction caches, while the third talk addresses the compression of instruction words. Finally, the last presentation optimizes performance and durability of flash-memories. The four papers together show the importance of addressing all aspects of memory optimization in future digital design.

51.1 Optimum LDPC Decoder: A Memory Architecture Problem
Erick Amador - *EURECOM, Sophia Antipolis, France*
Renaud Pacalet - *TELECOM ParisTech, Sophia Antipolis, France*
Vincent Rezard - *Infineon Technologies AG, Sophia Antipolis, France*

51.2 A DVS-Based Pipelined Reconfigurable Instruction Memory
Zhiguo Ge - *Intel Corp., Beijing, China*
Tulika Mitra, Weng-Fai Wong - *National Univ. of Singapore, Singapore*

51.3S LICT: Left-Uncompressed Instructions Compression Technique to Improve the Decoding Performance of VLIW Processors
Talal Bonny, Joerg Henkel - *Univ. Karlsruhe, Karlsruhe, Germany*

51.4S Hierarchical Architecture of Flash-Based Storage Systems for High Performance and Durability
Sanghyuk Jung, Yong Ho Song - *Hanyang Univ., Seoul, Republic of Korea*
Jin Hyuk Kim - *Samsung, Seoul, Republic of Korea*

Rm: 130

52 SCHEDULING IN TIME AND SPACE

Topic Area: System-Level and Embedded

Chair: Stavros Tripakis - *Univ. of California, Berkeley, CA*

Scheduling is a key challenge for the parallel architectural platforms used today in embedded systems. The papers in this session describe novel techniques for scheduling concurrent applications on resource-constrained architectural platforms. The first paper allows compaction of the application description while providing conservative bounds on real-time scheduling guarantees. The second paper presents a fast runtime heuristic for selecting a configuration for task execution in a multicore system. The third paper discusses extraction of static behavior from otherwise dynamic applications, enabling lower memory usage. Finally, the last paper characterizes applications to determine their suitability for deployment on heterogeneous multicore processors.

52.1 Reduction Techniques for Synchronous Dataflow Graphs
Marc Geilen - *Technische Univ. Eindhoven, Eindhoven, The Netherlands*

52.2 A Parameterized Compositional Multi-Dimensional Multiple-Choice Knapsack Heuristic for CMP Runtime Management
Hamid Shojaei - *Univ. of Wisconsin, Madison, WI*
Amir Hossein Ghamarian, Twan Basten, Marc Geilen, Sander Stuijk, Rob Hoes - *Technische Univ. Eindhoven, Eindhoven, The Netherlands*

52.3S Mode Grouping for More Effective Generalized Scheduling of Dynamic Dataflow Applications
William L. Plishker, Nimish Sane, Shuvra S. Bhattacharyya - *Univ. of Maryland, College Park, MD*

52.4S Efficient Program Scheduling for Heterogeneous Multicore Processors
Jian Chen, Lizy K. John - *Univ. of Texas, Austin, TX*

Rm: 125

53 HEURISTIC APPROACHES TO HARDWARE OPTIMIZATION

Topic Area: Synthesis and FPGA

Chair: Li Shang - *Univ. of Colorado, Boulder, CO*

Exact solutions for many important circuit optimization problems are computationally infeasible, so high-quality hardware generation often requires heuristic approaches. The first paper applies mathematical partitioning and compensation heuristics to optimize polynomial datapaths. The second paper optimizes register allocation for dual supply voltages. The third paper applies GPU-based parallelization to dramatically accelerate a heuristic algorithm for simultaneous gate sizing and threshold voltage assignment. The final paper explores the trade-off between performance and robustness in embedded microprocessor design using a novel figure of merit.

53.1 Polynomial Datapath Optimization Using Partitioning and Compensation Heuristics
Omid Sarbishei - *Sharif Univ. of Technology, Tehran, Iran*
Bijan Alizadeh - *Univ. of Tokyo and CREST, Japan Science and Technology, Tokyo, Japan*
Masahiro Fujita - *Univ. of Tokyo, Tokyo, Japan*

53.2 Register Allocation for High-Level Synthesis Using Dual Supply Voltages
Insup Shin, Seungwhun Paik, Youngsoo Shin - *KAIST, Daejeon, Republic of Korea*

53.3S GPU-Based Parallelization for Fast Circuit Optimization
Yifang Liu, Jiang Hu - *Texas A&M Univ., College Station, TX*

53.4S Architectural Assessment of Design Techniques to Improve Speed and Robustness in Embedded Microprocessors
Thomas Baumann - *Infineon Technologies. AG, Neubiberg, Germany and Technische Univ. München, Munich, Germany*
Doris Schmitt-Landsiedel - *Technische Univ. München, Munich, Germany*
Christian Pacha - *Infineon Technologies AG, Neubiberg, Germany*

Rm: 124

54 MODEL ORDER REDUCTION TECHNIQUES AND APPLICATIONS

Topic Area: Interconnect and Reliability

Chair: Peng Li - *Texas A&M Univ., College Station, TX*

This session presents advances in model order reduction techniques and an ingenious application to modeling lithography induced variations. The first paper describes an efficient method to optimize the selection of samples in multi-point model order reduction algorithms and the second paper introduces an efficient test for passivity. The final paper is an application of parameterized model order reduction to generate compact lithography mask models.

54.1 ARMS - Automatic Residue-Minimization Based Sampling for Multi-Point Modeling Techniques
Jorge Fernandez Villena - *INESC-ID, Univ. and Técnica de Lisboa, Lisbon, Portugal*
L. Miguel Silveira - *INESC-ID, Univ., Técnica de Lisboa and Cadence Design Systems, Inc., Lisbon, Portugal*

54.2 An Efficient Passivity Test for Descriptor Systems via Canonical Projector Techniques
Ngai Wong - *Univ. of Hong Kong, Hong Kong*

54.3 A Parameterized Mask Model for Lithography Simulation
Zhenhai Zhu - *Cadence Design Systems, Inc., Berkeley, CA*

47th Call for Contributions

47th DESIGN AUTOMATION CONFERENCE®
Anaheim Convention Center, Anaheim, CA - June 14 - 18, 2010
FOR INFORMATION CALL: +1-303-530-4333

With a heritage of excellence for almost half a century, DAC continues to be the premier conference devoted to Electronic Design Automation (EDA) and the application of EDA tools in designing advanced electronic systems. DAC 2010 is seeking papers that deal with tools, algorithms, and design techniques for all aspects of electronic circuit and system design. We invite submissions in the following categories: research papers, User Track papers, "Wild and Crazy Ideas" (WACI) topic papers, suggestions for special sessions, panels, and tutorials, and proposals for workshops and colocated events. Submissions must be made electronically at the DAC website. Detailed guidelines for all categories are available on the DAC website.

RESEARCH PAPERS
DUE BEFORE 5:00pm MT, November 19, 2009

Research paper submissions MUST (1) be in PDF format only, (2) contain an abstract of approximately 60 words clearly stating the significant contribution, impact, and results of the submission, (3) be no more than six pages (including the abstract, figures, tables, and references), double columned, 9-pt or 10-pt font, and (4) MUST NOT identify the author(s) by their name(s) or affiliation(s) anywhere on the manuscript or abstract, with all references to the author(s)'s own previous work or affiliations in the bibliographic citations being in the third person. Preliminary submissions will be at a disadvantage. Format templates are available on the DAC website. Submissions not adhering to these rules will be rejected. DAC will compare each submission against a vast database and any paper with significant similarity to previously published works or with papers that are simultaneously under review with other conferences and symposia, will be rejected. All research papers will be reviewed as finished papers. Authors of accepted papers must sign a copyright release form for their paper. Acceptance notices will be available by logging in to the DAC website after Feb. 25, 2010. Complete author kits will be available on the DAC website by March 19, 2010.

USER TRACK PAPERS - EXTENDED ABSTRACTS
DUE BEFORE 5:00pm MT, November 9, 2009

DAC's User Track addresses the real-life issues facing IC designers, application engineers, and design flow developers. It provides valuable insights and experiences with in-house or commercial EDA tool flows. User Track papers may describe the application of EDA tools to the design of a novel electronic system, or the integration of EDA tools within a design flow or methodology to produce such systems. A User Track paper may be problem-specific in scope (e.g., analyzing substrate coupling during floorplanning) or may address a specific application domain (e.g., designing wireless handsets). Submissions are in the form of an extended abstract. For more details, please see the separate User Track Call for Papers on the DAC website:
http://www.dac.com/47th/UTinfo.html

WILD AND CRAZY IDEAS (WACI) PAPERS
DUE BEFORE 5:00pm MT, November 19, 2009

The "Wild and Crazy Ideas" sessions cover interesting activities on a wide variety of topics that do not fit in the conventional mold. The WACI track features novel (and even preliminary or unproven) technical ideas. The aim of WACI is to promote revolutionary and way-out ideas that inspire discussion among conference attendees, create a buzz, and get people talking. Submissions to the "Wild and Crazy Ideas" track should not exceed two pages, but must otherwise follow the above rules and deadlines for the research papers. Unlike a DAC research paper that explores a specific technology problem and proposes a complete solution to it, with a full table of results, a WACI paper could present less developed but highly innovative ideas related to areas relevant to DAC. All WACI accepted papers will be required to post a two-minute video describing the work as part of the acceptance process.

SPECIAL SESSION SUGGESTIONS
DUE BEFORE 5:00pm MT, November 2, 2009

Special session suggestions must include descriptions of the proposed papers and speakers, and the importance of the special session to the DAC audience. As the term implies, a special session is devoted to a topic of strong contemporary or future interest. The topic must represent an emerging area that does not yet receive sufficient focus from research papers. A submission must list at least three inspiring speakers who address the topic from different angles. DAC reserves the right to restructure all special session suggestions.

PANEL and TUTORIAL SUGGESTIONS
DUE BEFORE 5:00pm MT, November 2, 2009

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure all panel and tutorial suggestions. Please see the website for further details, or call Kevin Lepine, Conference Manager, at +1-303-530-4333.

WORKSHOP SUBMISSIONS
DUE BEFORE 5:00pm MT, January 29, 2010

DAC invites you to organize a workshop on topics related to design, design methodologies, and design automation. DAC provides the financial and organizational support, including attendee registration, rooms at the conference center and audio visual equipment. Please see the website for further details, or call Kevin Lepine, Conference Manager at +1-303-530-4333.

COLOCATED EVENT PROPOSALS
DUE BEFORE 5:00pm MT, January 29, 2010

DAC invites you to colocate your conference, meeting or other special event with DAC. We will provide you with meeting rooms at the conference center at no cost. Your event will be financed and otherwise organized by you. Please see the website for further details, or call Kevin Lepine, Conference Manager, at +1-303-530-4333.

47th Call for Contributions

SUBMISSION CATEGORIES FOR RESEARCH PAPERS

Authors of research papers are required to specify a category from the following list:

1. System-Level Design and Codesign

1.1 System specification, modeling, simulation, verification, and performance analysis
1.2 Scheduling, HW/SW partitioning, HW/SW interface synthesis
1.3 IP and platform-based design, IP protection
1.4 System-On-Chip (SOC) and multiprocessor System-On-Chip (MPSOC)
1.5 Application-specific processor design tools

2. System-Level Communication and Networks-On-Chip

2.1 Modeling and performance analysis
2.2 Communications-based design, communication and network synthesis
2.3 Architectural synthesis, mapping, routing, scheduling
2.4 Optimization for energy, fault-tolerance, reliability
2.5 Interfacing and software issues, beyond-the-die communication
2.6 NOC design methodologies, case studies and prototyping

3. Embedded Hardware Design and Applications

3.1 Case studies of embedded system design
3.2 Flows and methods for specific applications and design domains

4. Embedded Software Tools and Design

4.1 Retargetable compilation
4.2 Memory/cache optimization
4.3 Software for single-/multiprocessor, multicore, GPU systems
4.4 Real-time operating systems
4.5 Verification of embedded software

5. Power Analysis and Low-Power Design

5.1 System-level power design and thermal management
5.2 Embedded low-power approaches: partitioning, scheduling, and resource management
5.3 High-level power estimation and optimization
5.4 Gate-level power analysis and optimization
5.5 Device and circuit techniques for low-power design
5.6 Power-aware and energy-efficient wireless protocols, algorithms and associated design techniques and methodologies

6. Verification

6.1 Functional, transaction-level, RTL, and gate-level modeling and verification of hardware design
6.2 Dynamic simulation, equivalence checking, formal (and semiformal) verification model and property checking
6.3 Emulation and hardware simulators or accelerator engines
6.4 Modeling languages and related formalisms, verification plan development and implementation
6.5 Assertion-based verification, coverage analysis, constrained-random testbench generation
6.6 Verification techniques for software correctness

7. High-Level Synthesis, Logic Synthesis and Circuit Optimization

7.1 Combinational, sequential, and asynchronous logic synthesis
7.2 Library mapping, cell-based design and optimization
7.3 Transistor and gate sizing, resynthesis
7.4 Interactions between logic design and layout or physical synthesis
7.5 High-level, behavioral, algorithmic, and architectural synthesis, "C" to gates tools and methods
7.6 Resource scheduling, allocation, and synthesis

8. Circuit, Interconnect and Manufacturing Simulation and Analysis

8.1 Electrical-level circuit simulation
8.2 Model order reduction methods for linear systems
8.3 Interconnect and substrate modeling and extraction
8.4 High-frequency and electromagnetic simulation of circuits
8.5 Thermal and electrothermal simulation
8.6 Technology CAD and fab automation

9. Timing Analysis

9.1 Process technology characterization, and modeling
9.2 Deterministic static timing analysis and verification
9.3 Statistical performance analysis and optimization

10. Physical Design and Manufacturability

10.1 Floorplanning, partitioning, placement
10.2 Buffer insertion, routing, interconnect planning
10.3 Physical verification and design rule checking
10.4 Automated synthesis of clock networks
10.5 Reticle enhancement, lithography-related design optimizations
10.6 Design for manufacturability, yield, defect tolerance, cost issues, and DFM impact
10.7 Physical design of 3-D integrated circuits
10.8 System-in-package design, package-board codesign
10.9 Design for resilience under manufacturing variations

11. Signal Integrity and Design Reliability

11.1 Signal integrity, capacitive and inductive crosstalk
11.2 Reliability modeling and analysis
11.3 Novel clocking and power delivery schemes
11.4 Power grid robustness analysis and optimization
11.5 Soft errors
11.6 Thermal reliability

12. Analog, Mixed-Signal, and RF

12.1 Analog, mixed-signal, and RF design methodologies
12.2 Automated synthesis
12.3 Analog, mixed-signal, and RF simulation
12.4 High-frequency design and advanced antenna design for wireless design

13. FPGA Design Tools and Applications

13.1 Rapid prototyping
13.2 Logic synthesis and physical design techniques for FPGAs
13.3 Configurable and reconfigurable computing

14. Testing

14.1 Test quality/reliability, current-based test, delay test, low-power test
14.2 Digital fault modeling, automatic test generation, fault simulation
14.3 Digital design for test, test data compression, built-in self test
14.4 Memory test and repair, FPGA testing
14.5 Fault-tolerance and online testing
14.6 Analog/mixed-signal/RF testing, system-in-package (SIP) testing
14.7 Board- and system-level test, system-on-chip (SOC) testing
14.8 Silicon debug and diagnosis, post-silicon design validation

15. New and Emerging Design Technologies (including but not restricted to)

15.1 MEMS, sensors, actuators, imaging devices
15.2 Nanotechnologies, nanowires, nanotubes
15.3 Quantum computing
15.4 Synthetic and systems biology, biologically-based or biologically-inspired systems
15.5 Non-CMOS 3-D design, new transistor structures and devices, design in new or radical process technologies
15.6 Optical devices and communication

ALL SUBMISSIONS MUST BE MADE ELECTRONICALLY AT THE DAC WEBSITE: WWW.DAC.COM.

ACM and IEEE reserve the right to exclude a paper from archival distribution after the conference if the paper is not presented at the conference, or in other exceptional cases.

Additional Meetings

Monday, July 27

Marriott Hotel, Yerba Buena Salon 4-6

SYSTEM PROTOTYPING LUNCHEON - INSIGHTS INTO A NEW METHODOLOGY FOR ACCELERATING SOC DESIGN

Topic Area: New and Emerging Technologies 11:30am - 1:30pm

The Synopsys System Prototyping Luncheon is a forum for members of the electronic design community to get the latest information on solutions and methodologies for accelerating the design and verification of SOC designs.

Intended for IC design and verification engineers and managers, as well as for system architects, this event will discuss how software-based methodologies like IP, high-level synthesis and virtual platforms, when combined with the performance and versatility of hardware-based Rapid Prototyping systems can boost productivity, accelerate schedules, and lead to higher quality designs.

Rm: 200

CEDA PUBS BOARD AND IEEE EMBEDDED SYSTEMS LETTERS (ESL) EDUCATION BOARD MEETING

Topic Area: General Interest 3:00 - 6:00pm

Organizers: Thomas Centrella -
Rajesh Gupta - *Univ. of California, San Diego, La Jolla, CA*

Rm: 206

DESIGN AND TEST EDITORIAL BOARD MEETING

Topic Area: General Interest 4:00 - 6:00pm

Organizer: Ed Zintel - IEEE CS Publications

Marriott Hotel, Yerba Buena Salon 7

SYNOPSYS/SUN UNIVERSITY RECEPTION

Topic Area: New and Emerging Technologies 6:00 - 8:00pm

University professors and students are invited to join Synopsys and Sun Microsystems for an evening reception including drinks and hors d'oeuvres. Prize drawings will be held throughout the evening and the following keynote presentations will be featured.

Verifying a Billion-Gate SOC
Janick Bergeron - *Synopsys Fellow, Synopsys, Inc.*

Design in the Nano-Scale Era: Low-Power, Reliability, and Error Resiliency
Kaushik Roy - *Roscoe H. George Professor of Electrical and Computer Engineering, Purdue Univ.*

Rm: 220/222

SI2 ANNUAL MEMBER/GUEST MEETING

Topic Area: Low-Power Design 6:00 - 8:00pm

The Annual Si2 Member/Guest Meeting is open to both member and non-member companies and individuals who are interested in Si2 activities such as OpenAccess, advanced library modeling systems, DFM and low-power design. A networking opportunity will be held at the beginning and end of the meeting with refreshments and light hors d'oeuvres. Steve Schulz, President and CEO of Si2, will present an outline of Si2's activities and accomplishments of the past year and directions for the year ahead, and will also announce the newly-elected members of Si2's Board.

To register for this event, leave a message at this link:

http://www.si2.org/?page=3

Marriott Hotel, Yerba Buena Salon 4-6

PRIMETIME SPECIAL INTEREST GROUP (SIG) RECEPTION

Topic Area: New and Emerging Technologies 6:00 - 8:00pm

Synopsys invites you to join us for cocktails, hors d'oeuvres and a highly informative session covering the latest timing analysis trends, challenges and solutions. Listen to Synopsys R&D and industry-leading experts discuss best practices and present their views on the hottest timing-related topics. If you are a timing signoff engineer or manager, you won't want to miss this special event.

Tuesday, July 28

Rm: 309

PANEL DISCUSSION: FRONTIERS IN VERIFICATION: COVERAGE, CLOSURE AND BEYOND

Topic Area: Verification and Test 7:30 - 9:00am

Moderator: Scott Sandler - *Vice President of Corporate Marketing, Springsoft, Inc.*

Verification of complex electronic system and IC designs is a constantly and rapidly evolving art. Changes in how designs are constructed at the silicon, circuit, logic, and system levels demand new tools and tactics. The implications for verification are enormous: IP plays an increasing role, standards are essential to ensure interoperability of tools, and issues such as coverage, closure, power, and software are becoming critical. This panel will bring together a group of seasoned verification professionals for a lively conversation on how verification must change in the coming years to keep pace.

Marriott Hotel, Yerba Buena Salon 7

SYNOPSYS, INC. VERIFICATION LUNCHEON

Topic Area: Verification and Test 12:00 - 2:00pm

Synopsys invites you to join us for lunch and a highly informative session covering the latest verification trends, challenges and solutions. Listen to leading industry experts discuss best practices and present their views on the hottest verification topics. Learn about new innovations in verification technology that help improve performance and productivity, such as VCS Multicore and the most recent advancements in VMM. If you are a verification engineer or manager, you won't want to miss this special event.

Rm: 300

ACM/SIGDA LEADERSHIP LUNCHEON

Topic Area: General Interest 12:00 - 2:00pm

Organizer: Patrick Madden - *Binghamton Univ., Binghamton, NY*

Organizers of symposia and workshops sponsored by ACM/SIGDA and any ACM/SIGDA volunteers are invited to a lunch get-together. Please meet at room 300 and we will have lunch at an off-site location.

Marriott Hotel, Yerba Buena Salon 8

IPL ALLIANCE LUNCHEON - THE EDA EARTHQUAKE: INTEROPERABLE PDKs SHAKIN' UP THE ANALOG DESIGN WORLD

Topic Area: Business and Technology 12:00 - 2:00pm

Last year's IPL lunch featured the announcement of TSMC joining the IPL Alliance and collaboration with key alliance members to create the industry's first 65nm interoperable PDK. This year, IPL members will present a foundry qualified and validated interoperable PDK.

Attendees will hear about the challenges, features, and roadmap, and customer experiences using the kit.

Rm: 220

SILICON IP - BEYOND CHIPS TO SYSTEMS. WHAT ARE THE CHALLENGES AND OPPORTUNITIES?

Topic Area: New and Emerging Technologies 3:00 - 5:00pm

It's no secret that critical challenges and opportunities exist in the silicon IP industry: complexity of integration and verification, and the need for IP configurability. Companies integrating IP into an SOC, ASIC or FPGA must be able to verify the IP not just in the chip context, but also in the system context. This panel will look at the work being done to assist customers in 'gluing' together IP. It will also examine a new trend—the emergence of pre-integrated IP subsystems with the potential to raise the level of abstraction, as it were, for the integration problem.

Wednesday, July 29

Marriott Hotel, Yerba Buena Salon 7

SYNOPSYS INTEROPERABILITY BREAKFAST: VMM AND IPL

Topic Area: Verification and Test 7:30 - 9:30am

Dr. Chi-Foon Chan, President and COO of Synopsys, invites you to join other designers and EDA users at this annual insightful event. Hear from your peers and suppliers how VMM is used to improve the quality of verification across the entire design spectrum. Learn how interoperable PDKs bring enhanced productivity to custom designers. See who wins the Tenzing Norgay Interoperability Achievement Award.

Rm: 250/262

MDA'S FORMALIZED AMS DESIGN AND REUSE PLATFORM - DAC BREAKFAST PRESENTATION

Topic Area: Analog/Mixed-Signal/RF Design 8:00 - 9:00am

Free and open to all DAC attendees after registration

(www.mephisto-da.com/dac09) - places are limited!

In the last decade we've seen several efforts in EDA to increase the productivity of analog circuit design.

Both start-ups and big EDA vendors have made some progress but unfortunately we're stll far away from any significant change in analog design efficiency in industrial design teams.

This presentation will provide an overview of what is feasible today from a technological perspective and, equally important, how this technology can be introduced to and embraced by the analog design community.

Finally, an overview is provided of how MDA's M-Design platform can boost AMS design efficiency for both novice and expert designers in a non-intrusive way.

For more information, please visit MDA's booth: #521.

Rm: 303

EDA ROADMAP WORKSHOP

Topic Area: Business 9:00am - 5:00pm

Organizers: Andrew B. Kahng - *Univ. of California, San Diego, La Jolla, CA*
Juan-Antonio Carballo - *IBM Corp., San Francisco , CA*

DAC's EDA Roadmap Workshop is the first forum for deep discussion around roadmapping issues relating to the EDA industry. Top industry, consortia, and academic leaders will huddle to analyze the need and state of the sector's roadmapping efforts, and will craft a blank-sheet view of EDA roadmapping for the next 15 years.

Rm: 114

ACM TODAES EDITORIAL BOARD MEETING

Topic Area: General Interest 11:00am - 1:00pm

Organizer: Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

This is the annual meeting of the Editorial Board of the ACM Transaction on Design Automation of Electronic Systems.

Rm: 102

7TH ANNUAL ESL SYMPOSIUM LUNCHEON

Topic Area: System-Level and Embedded 11:00am - 2:00pm

The 7th Annual ESL Symposium Luncheon will be moderated by Walden C. Rhines, CEO of Mentor Graphics, who will be joined by a panel of industry experts sharing their insight and knowledge. Relevant topics discussed include:

- Present and future challenges in an architecture design and verification process.
- Future architecture requirements, such as multicore platforms, and how they change ESL tool capabilities.
- The role of high-level synthesis in bridging the gap between architectural design and RTL.
- The impact of embedded software in the process of architectural design and verification.

Rm: 114

ACM/SIGDA JOINT TECHNICAL COMMITTEES MEETING

Topic Area: Business 12:15 - 2:00pm

Organizer: Massoud Pedram - *Univ. of Southern California, Los Angeles, CA*

This is the annual meeting of the officers of the ACM SIGDA Technical Committees. Updates from SIGDA's Technical Committees will be presented.

Rm: 114

CANDE MEETING

Topic Area: General Interest 6:00 - 7:00pm

Organizer: David Pan - *Univ. of Texas, Austin, TX*

CANDE is a joint Technical Committee on Design Automation for the IEEE Circuits and Systems Society (CASS) and the Council on Electronic Design Automation (CEDA). It is the sponsoring committee from CASS and CEDA for both ICCAD and DAC. CANDE brings design automation professionals together to build relationships, and to sponsor a workshop and initiatives that improve the CAD/EDA industry.

Please visit the CANDE website for more information: http://www.cande.net

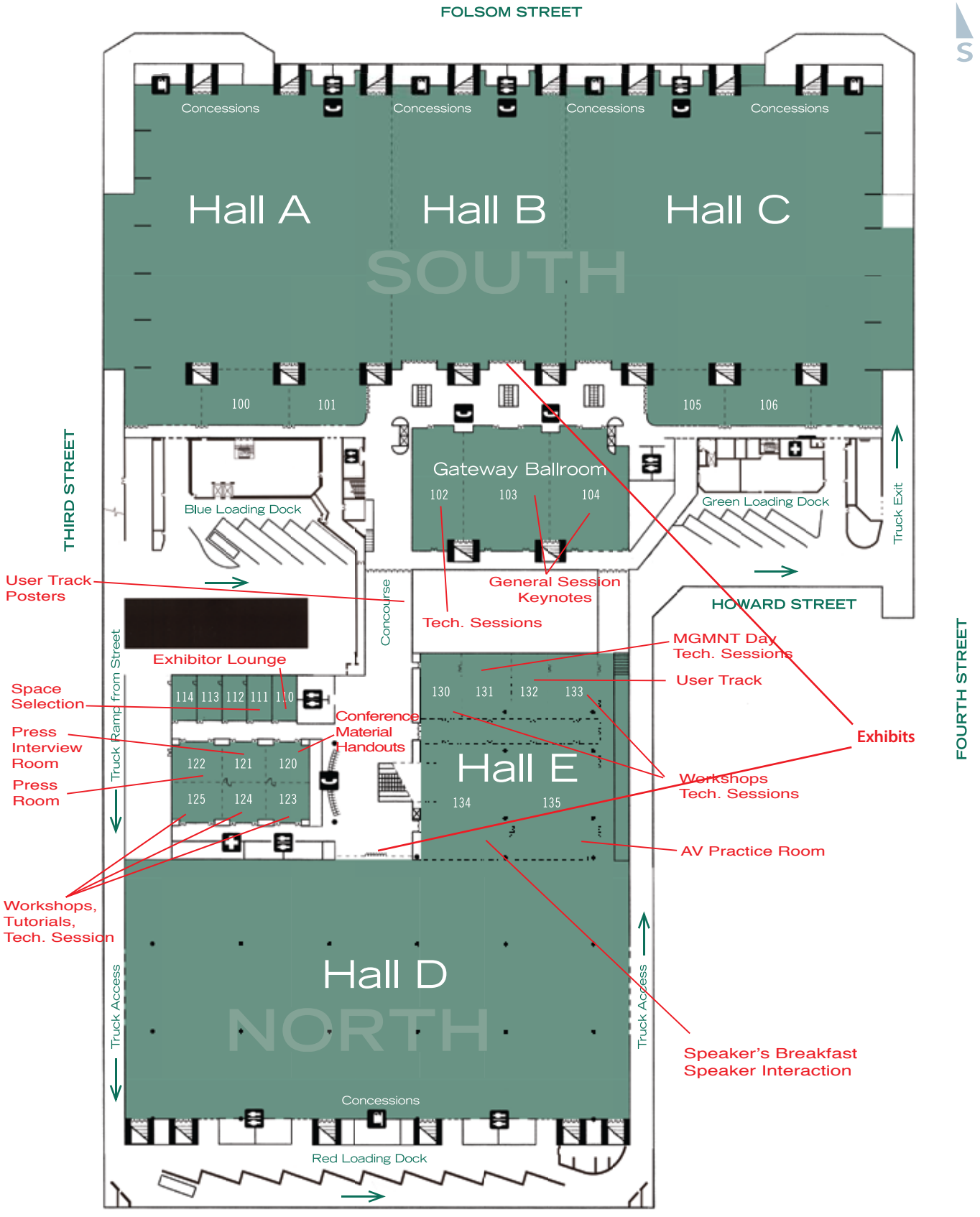
Rm: 124

BIRDS-OF-A-FEATHER (BOF)

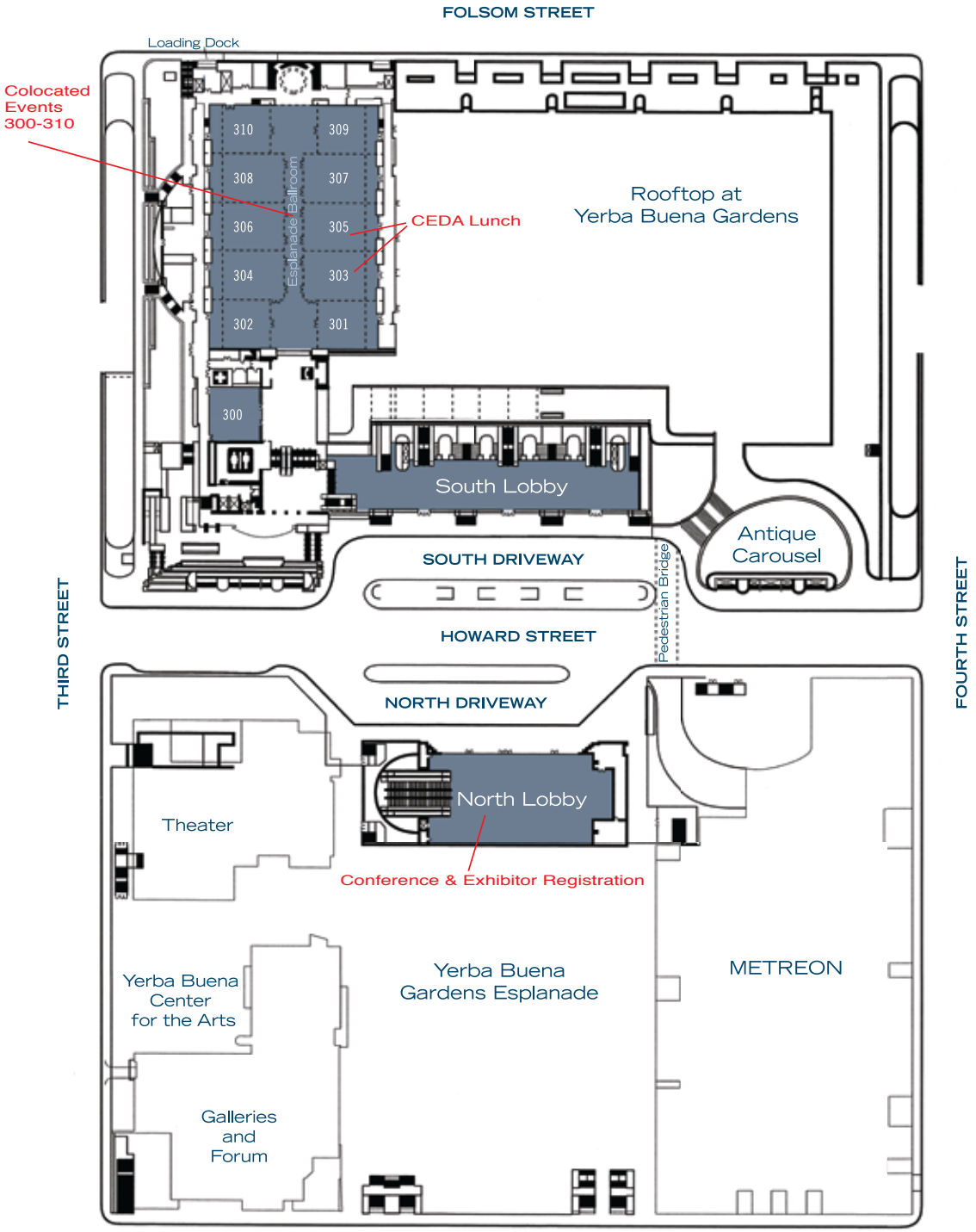
Topic Area: General Interest 6:00 - 7:30pm

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather" (BOF). All BOF meetings are held at the Moscone Center, Wednesday, July 29 / 6:00 - 7:30pm. DAC will facilitate common interest groups meetings to discuss DA related topics. To arrange a BOF meeting, please sign up at the Information Desk located in the North lobby. A meeting room will only be assigned if ten or more people sign up. An LCD projector and screen will be provided. Check DACnet and the Birds-of-a-Feather board at the information desk.

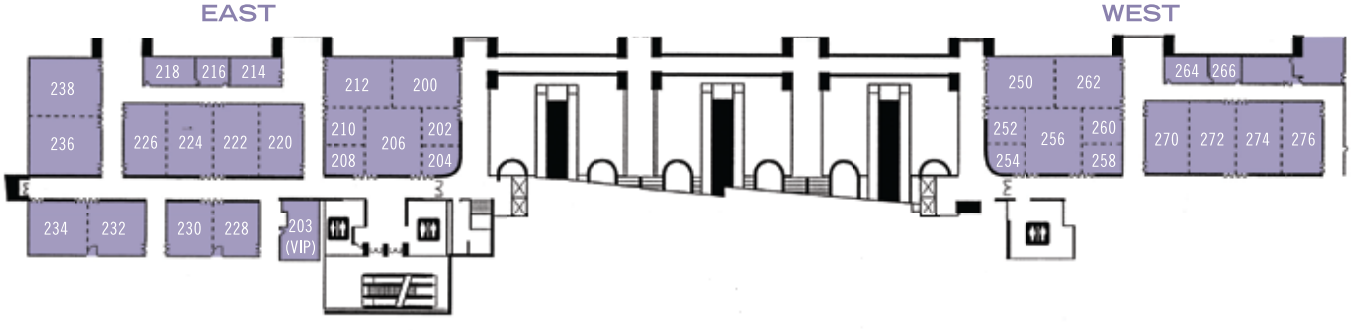
EXHIBIT **LEVEL**



ESPLANADE **LEVEL**



MEZZANINE **LEVEL**



MANAGEMENT DAY

Tuesday, July 28

Sponsored by: cadence™

10:30am - 6:00pm / Rm: 131

For details, see page 12

Where Business and Technology Intersect...

ACM

Knowledge, Collaboration, & Innovation in Computing

Resources for ACM Members

New and Noteworthy

Communications of the ACM

Fully redesigned and redefined, ***Communications*** is the leading print and online magazine for the computing and information technology fields. Industry leaders use *Communications* as a platform to present and debate various technology implications, public-policies, engineering challenges and market trends. Complimented by a new website featuring advanced browse funcitonality, blogs, archives and much more, *Communications* is truly the world's leading source for advanced computing content and resources.

acmqueue Website

acmqueue is now entirely online offering expanded content, increased frequency and more direct engagement with experts. Guided and written by distinguished and widely known practicing professionals, the expanded acmqueue offers features such as: ***planet queue*** blogs by authors who "unlock" important content from the ACM Digital Library and provide commentary; videos; downloadable audio; CTO Roundtable discussions; plus unique Case Studies.

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Additional Resources

ACM Local Chapters
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Distinguished Speaker Luncheon and Lecture

Tuesday, July 28
12:00 - 2:00 PM
Rooms 303-305

"Frontiers in Research and Education in Computing: A View from the National Science Foundation"

Jeannette M. Wing
Assistant Director for
Computer and Information
Science and Engineering
National Science Foundation

President's Professor of Computer Science
Carnegie Mellon University

CEDA
IEEE Council on Electronic Design Automation

http://www.c-eda.org/

Monday CEO Panel: Futures for EDA: The CEO View

Aart de Geus
CEO and Chairman of the Board
Synopsys, Inc.

SYNOPSYS®

Walden C. Rhines
CEO and Chairman of the Board
Mentor Graphics Corp.

Mentor Graphics®

Lip-Bu Tan
President and CEO
Cadence Design Systems, Inc.

cadence™

Monday, July 27, 4:30 - 5:45pm

Gateway Ballroom

46 YEARS

DESIGN AUTOMATION CONFERENCE

Keynote Address

Tuesday, July 28, 8:30 - 10:15am

Gateway Ballroom

Speaker:

Overcoming the New Design Complexity Barrier: Alignment of Technology and Business Models

Fu-Chieh Hsu

Vice President, Design and Technology Platform

Taiwan Semiconductor Manufacturing Company Ltd., Hsinchu, Taiwan

46 YEARS

DESIGN AUTOMATION CONFERENCE

Keynote Address

Wednesday, July 29, 11:15am - 12:15pm

Gateway Ballroom

Speaker:

The End of Denial Architecture and the Rise of Throughput Computing

William J. Dally

Chief Scientist and Senior Vice President of Research, NVIDIA Corp. Santa Clara, CA,Willard R. and Inez Kerr Bell Professor of Engineering Stanford Univ., Stanford, CA


Wednesday Night Party
San Francisco Marriott Hotel
Yerba Buena Ballroom
Wednesday, July 29, 2009

Special Plenary Panel: How Green Is My Silicon Valley

Thursday, July 30, 12:00 - 1:45pm

Gateway Ballroom

Walden C. Rhines

EDA Consortium, Chair, Mentor Graphics Corp., Wilsonville, OR

Panelists:

Ian Wright
CEO, Wrightspeed

Thomas Jacoby
Director, California Clean Energy Fund
Chairman of the Board, Innovations Fuel, Inc.
CEO, Tymphany Corp.

John A. "Skip" Laitner
Director of Economic Analysis
American Council for an Energy Efficient Economy (ACEEE)

46 YEARS

DESIGN AUTOMATION CONFERENCE

Notes

Floorplan will be a fold-out

Schedule will be a fold-out

Exhibitor Listing

Accelicon Technologies, Inc. 4062
autoESL Design Technologies, Inc. 3255
ACE Associated Compiler Experts bv 3648
Achilles Test Systems, Inc. 912
Agnisys Inc. 4064
Altair Engineering 4208
Altos Design Automation 1504
Amiq Consulting S.R.L. 4305
Analog Bits Inc. 811
Analog Rails 3542
AnSyn 422
APAC IC Layout Consultant, Inc. 4214
Apache Design Solutions, Inc. 722
Applied Simulation Technology 3342
Artwork Conversion Software, Inc. 1109
Ateeda Limited 4102
Atoptech 3167
Atrenta Inc. 1528
austriamicrosystems 1417
AutoESL Design Technologies, Inc. 3755
Avery Design Systems, Inc. 1724
Axiom Design Automation 1815
BEEcube, Inc. 4307
Berkeley Design Automation, Inc. 1620
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Bluespec, Inc. 3851
Breker Verification Systems 4051
Cadence Design Systems, Inc. 3751, 4300
Calypto Design Systems 1610
Cambridge Analog Technologies, Inc. 4301
Carbon Design Systems 3359
CAST, Inc. 1421
ChipEstimate.com 1100
ChipVision Design Systems 3555
Chipworks 4203
Ciranova, Inc. 4400
ClioSoft, Inc. 3651
CLK Design Automation, Inc. 3951
CMP 1214
CoFluent Design 3151
Concept Engineering GmbH 918
Coupling Wave Solutions 608
CoWare, Inc. 3665
CST of America, Inc. 3155
DAC Pavilion 1928
DAFCA, Inc. 3855
Dassault Systemes 716
Dataram 1206
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Denali Software, Inc. 1424
Desaut Inc. 1207
Design and Reuse 1006
Dini Group 914
DOCEA Power 3143
Dolphin Integration 1314
Duolog Technologies Ltd. 2028
Dynalith Systems Co., Ltd. 3440
E-System Design 408
EDA Cafe-IB Systems 3445
EDXACT SA 3765
Elsevier 1311
EMA Design Automation, Inc. 3267
Entasys Design, Inc. 3863
Enterpoint Ltd. 4207
Epoch Microelectronics, Inc. 4213
EVE 908
Exhibitor Forum 4359
Extension Media - Chip Design 1408
Extreme DA 1710
Fidus Systems Inc. 4204
FishTail Design Automation, Inc. 3064
Forte Design Systems 1225
FTL Systems, Inc. 1215
GateRocket, Inc. 3550
GiDEL 810
Gradient Design Automation 2024
Helic, Inc. 1824
Hewlett-Packard Co. 1110
IBM Corp. 4311
IC Manage, Inc. 1810
ICDC Partner Pavilion & Stage 4500
IMEC / Europractice 820
Imera Systems, Inc. 3964
Incentia Design Systems, Inc. 808
Infiniscale 3065
Infotech Enterprises Electronic Des. Svc. 711
Innovative Logic Inc. 1306
iNoCs 4303
Instigate 3449
Institution of Engineering and Technology 1308
InternetCAD.com, Inc./Timberwolf Systems 1208
Interra Systems, Inc. 1316
Jasper Design Automation, Inc. 3767
Jspeed Design Automation, Inc. 817
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Legend Design Technology, Inc. 1510
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Magma Design Automation, Inc. 1414
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Nangate 3265
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Nusym Technology, Inc. 622
Oasys Design Systems, Inc. 3061
OneSpin Solutions GmbH 3465
OptEM Engineering Inc. 3351
Optiwave Systems Inc. 916
Orora Design Technologies, Inc. 4151
OVM World 3450
Pextra 1825
Physware, Inc. 1814
PLD Applications (PLDA) 511
POLYTEDA Software Corp. 814
Prentice Hall Prof./Pearson Education 909
Prolific, Inc. 3543
Pulsic Ltd. 815
QThink, Inc. 1216
R3 Logic Inc. 813
Real Intent, Inc. 1728
Reed Business Information 1209
Runtime Design Automation 1117
Sagantec 522
Satin IP Technologies 2124
Seloco, Inc. 1419
Semifore, Inc. 812
Sequence Design, Inc. 3455
Shearwater Group, Inc. (The) 1201
Si2 1400
SIGDA/DAC University Booth 1828
Sigrity, Inc. 708
Silicon Design Solutions 1410
Silicon Frontline Technology 3165
Silicon Image 3243
SKILLCAD INC. 3261
SmartPlay Technologies 520
SoftJin Technologies 3547
Solido Design Automation Inc. 3060
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Target Compiler Technologies NV 3365
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Teklatech 614
Tela Innovations 710
The RTC Group 3355
Tiempo 4104
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True Circuits, Inc. 1101, 3346
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TSMC Open Innovation Forum, Cadence 822
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TSMC Open Innovation Forum, Synopsys 822
TSMC Open Innovation Forum, Tela Innovat. 822
TSMC Open Innovation Forum, Virage Logic 822
TSMC Open Innovation Forum, Wipro 822
TSSI - Test Systems Strategies, Inc. 3540
Tuscany Design Automation, Inc. 3955
Uniquify, Inc. 620
Univa UD 610
Verific Design Automation 3545
Veritools, Inc. 1423
ViASIC Inc. 1522
Warthman Associates 4205
WinterLogic Inc. 3963
XJTAG 3954
XYALIS 1914
Z Circuit Automation, Inc. 1010, 901
Zeland Software, Inc. 1107

Exhibiting Company Descriptions

Accelicon Technologies, Inc.
Booth: 4062

Cupertino, CA

www.accelicon.com

Accelicon Technologies, is the technology leader in device-level modeling and validation. With over 80 customers worldwide, Accelicon has established itself as a clear market leader. Accelicon's products are: MBP, the next-generation device-level model extraction and generation solution, incorporating superior optimization and simulation for 'order of magnitude' performance improvement and unparalleled ease of use, MQA, a rules-driven device-level model validation solution used for model QA and qualification, and PQA automating the analysis of advanced model layout-effects on the design.

ACCIT - New Systems Research
Booth: 3255

Alexandria, Egypt

www.accit-newsystemsresearch.com

ACCIT - New Systems Research is a total solution provider offering products and services in the field of ultra fast Electronic Design Automation (EDA) tools using massively parallel high performance computing platforms. The company's main demo at DAC 2009 is a full precision true analog simulator implemented on massively parallel architectures.

ACE Associated Compiler Experts bv
Booth: 3648

Amsterdam, Netherlands

www.ace.nl

ACE Associated Compiler Experts is one of the world's oldest independent employee-owned IT companies supplying advanced system software products and know-how. With a natural drive to perfection, the compiler experts at ACE are committed to delivering high quality in both products and services. ACE ensures that, the CoSy compiler development system and the SuperTest compiler test and validation suite are recognized for their outstanding quality and support.

Achilles Test Systems, Inc.
Booth: 912

Waltham, MA

www.achillestest.com

Achilles Test Systems products and services enable development teams to correlate results across multiple project data files, cutting debug time in a collaborative development process. Project status is always available and up to date with automatically generated tables and charts to highlight trends from historical data. Every member of a global team just needs a web browser to contribute insights and to access an integrated visualization of seed tracking, test data, and source-code revision history.

Agnisys Inc.
Booth: 4064

Lowell, MA

www.agnisys.us

Agnisys provides innovative tools for design, verification of IPs/SoCs for ASICs/FPGAs.

IDesignSpec is a register management tool that enables you to describe addressable registers in a specification document and generate code from it (RTL, C/C++ headers, OVM/VMM, IP-XACT, SystemRDL, PDF, etc.), thus saving time, promoting reuse and improving quality.

IVerifySpec is a verification management tool that combines requirement capture and traceability with verification planning and simulation result analysis. It's a powerful DO-254 enabling tool to close the loop on open-ended-verification.

Altair Engineering
Booth: 4208

Irvine, CA

www.altair.com

Privately held with more than 1,300 employees, Altair has offices throughout North America, South America, Europe and Asia/Pacific. With a 20-year-plus track record for innovative product design and development, grid computing and analytics technologies, and advanced engineering software, Altair today counts more than 3,500 corporate clients across many vertical industries.

Altos Design Automation
Booth: 1504

San Jose, CA

www.altos-da.com

Altos Design Automation (www.altos-da.com) provides ultra-fast library characterization products for standard cells, I/Os and embedded memories. Altos' "inside view" technology dramatically improves characterization throughput via intelligent use of simulation resources. Liberate supports advanced timing, noise and low power models (CCS, ECSM). Liberate LV enables library validation while Liberate MX automates the creation of embedded memory models. Variety generates variation aware libraries for multiple SSTA tools, including global and local variation. To "improve your view" visit Booth #1504 or email info@altos-da.com

Amiq Consulting S.R.L.
Booth: 4305

Bucharest, Romania

www.amiq.ro

AMIQ develops DVT Eclipse, an IDE for e and SystemVerilog (like Visual C). A unified window combines the smart editor (autocomplete, errors as you type) with class browsing, compliance review, task tracking, 3rd party simulators, revision control and more, which enables efficient code writing, both for beginners and complex maintenance.

AMIQ provides ASIC functional verification services, VIP development and training with significant expertise in e and SystemVerilog, related methodologies (eRM, OVM, VMM) and tools (Sn, IUS, Questa, VCS, vMgr).

Analog Bits Inc.
Booth: 811

Mountain View, CA

www.analogbits.com

Analog Bits, Inc. specializes in designing transistor level IP components fully customized for easy and reliable integration into modern CMOS digital chips.

Products include precision clocking macros such as PLLs, DLLs, programmable interconnect solutions such as multi-protocol SERDES/PMA, programmable I/Os and specialized memories such as high-speed SRAMs, T-CAMs. With billions of IP fabricated in customer silicon from 0.35-um to 32/28-nm processes, Analog Bits is the premier IP supplier with an outstanding heritage of "first time working silicon" at merchant foundries and IDMs.

Analog Rails
Booth: 3542

Chandler, AZ

www.analograils.com

Automatic analog and mixed signal IC complete simulation and design environment. Native on OA.

Schematic, simulation, optimization, parasitic extraction, analog place & route, differential wiring, shields, common centroid structures.

- Manual layout has correct by construction built in DRC & LVS.
- Devices snap and align.
- Digital layout: generates standard cells, placement, routing, timing.
- Always simulate layouts.
- Full hierarchical layouts are created on the fly!
- Cut design cycle to a fraction of the time. Now lightening fast.
- Handles millions of devices.

AnSyn
Booth: 422

Linköping, Sweden

www.ansyn.com

AnSyn provides software and design services for the analog and mixed-signal integrated circuit industry. We offer industrially proven solutions to increase productivity, improve performance, and guarantee high yield in analog design.

Our software products, Analog Dimensions and EqSim, provide a complete platform for optimization-based design of analog and mixed-signal ICs at transistor level. Combining fast performance evaluation and efficient optimization techniques enable optimization-based design of large analog circuits over PVT corners and mismatch conditions.

Apache Design Solutions, Inc.
Booth: 722

San Jose, CA

www.apache-da.com

Apache is a leading provider of global power and noise integrity solutions for Chip-Package-System convergence. Apache's innovative platforms address the unique power and noise challenges of digital, analog/mixed-signal, package/PCB, and SiP designs, while providing an eco-platform that integrates the SoC, custom IP, and System worlds. From early-stage prototyping and optimization through proven silicon sign-off, over 100 customers including 90% of the top semiconductor companies have adopted Apache's products (RedHawk, Totem, and Sentinel) for cost reduction, risk mitigation, and time-to-market improvements.

Applied Simulation Technology
Booth: 3342

San Jose, CA

www.apsimtech.com

Applied Simulation Technology provides IC and PCB design simulation, extraction and modeling solutions for Signal Integrity, Power Integrity and EMI. The software enables engineers to analyze the impact of the layout interconnect and power distribution on system preformance.

Switching noise, delay, crosstalk, impedance and related issues are predicted at the layout stage. Model order reduction technology is used in order to handle large LCR networks associtated with power distribution modeling and simulation.

Solutions range from 2-D to 3-D static and 3-D full wave simulation for support of Gbit designs.

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Exhibiting Company Descriptions

Artwork Conversion Software, Inc.
Booth: 1109

Santa Cruz, CA

www.artwork.com

Artwork provides a wide variety of CAD translators (GDSII, Gerber, DXF, IGES, MEBES), layout viewers (GDSII, OASIS, OA), geometry engines for mask boolean (AND, OR, NOR, XOR) and high resolution rasterizers for mask writers, inspection equipment and direct inkjetting of resists and metal.

Our tools are available on Windows, Linux and Solaris. Many of our tools are available as libraries that can be incorporated into OEM software.

Artwork is celebrating its 20th year in business.

Ateeda Limited
Booth: 4102

Edinburgh, United Kingdom

www.ateeda.com

ATEEDA demonstrates world's first Push Button ANALOG BIST tool at DAC 2009

Following success in volume production of its core EDA analog test tool, OptimATE, ATEEDA launches its analog BIST solution. LinBIST is the world's first EDA tool with genuine pushbutton-BIST. Now the cost-savings associated with BIST are open to all semiconductor companies (IDMs & Fabless alike). Covering a diversity of analog circuits from ADCs & DACs, to regulators and line drivers, ATEEDA's family of tools use smart algorithms, restricted digital gates with minimal analog circuitry to deliver the benefits of BIST.

Atoptech
Booth: 3167

Santa Clara, CA

www.atoptech.com

ATopTech was founded by leading EDA physical design implementation experts to build the next generation of place and route tools focused on designs at 65nm and below. The company's flagship product, Aprisa, is a complete netlist-to-GDSII physical design solution, including floorplanning, placement, clock-free synthesis and optimization, global and detailed routing, and an extremely fast timing engine to handle complex timing challenges such as OCV and MCMM. Aprisa's sign-off accurate timer ensures tight correlation to sign-off timing, eliminating costly iterations in order to close timing.

Atrenta Inc.
Booth: 1528

San Jose, CA

www.atrenta.com

Atrenta is the leading provider of Early Design Closure® solutions that radically improve the efficiency of integrated circuit design. Using Atrenta's comprehensive tool suite for architectural chip assembly and RTL analysis, customers can create robust and correct designs rapidly, preventing expensive and tedious iterations during the implementation phase. With over 150 customers worldwide, including the world's top 10 semiconductor companies, Atrenta provides the most comprehensive solution in the industry for Early Design Closure. Atrenta, Right from the Start!

austriamicrosystems
Booth: 1417

Raleigh, NC

www.austriamicrosystems.com

austriamicrosystems, a leading designer and manufacturer of high performance analog ICs, combines more than 25 years of analog design capabilities and system know-how with its own state of the art manufacturing and test facilities. Operating worldwide, austriamicrosystems is focused on power management, sensors & sensor interfaces, portable audio and car access through its business units Communications, Industry & Medical, Automotive and Full Service Foundry. austriamicrosystems Full Service Foundry is your analog foundry partner focusing on specialty process technologies like RF-CMOS, High-Voltage CMOS and SiGe-BiCMOS.

AutoESL Design Technologies, Inc.
Booth: 3755

Cupertino, CA

www.autoesl.com

AutoESL provides software tools & services that dramatically accelerate the design of systems-on-chip (SoCs). Using state of the art compilation technologies AutoESL's High-Level-Synthesis tools offer the industry's best and only unified language support of C, C++ and SystemC, perform highly effective and efficient optimization of power, performance, and area resulting in reliable and highest-quality implementation-aware RTL. AutoESL addresses both the ASIC and FPGA-based systems markets.

Avery Design Systems, Inc.
Booth: 1724

Andover, MA

www.avery-design.com

Avery Design Systems, Inc. is a leading provider of intelligent functional verification solutions.

Proven VIP for PCI Express, USB, and ATA/SATA speeds testbench development and compliance verification and supports advanced SystemVerilog OVM and VMM implementations and other popular verification environments.

Innovative simulation-centric formal analysis enables more effective early design verification using reachability analysis, supports robust coverage closure and bug hunting methods, and addresses specialized concerns for reset and low power verification.

SimCluster parallel simulation speeds up your RTL and gate-level simulations by 5-10X using simulators you already own.

Axiom Design Automation
Booth: 1815

Milpitas, CA

www.axiom-da.com

Axiom will showcase the industry proven MPSim simulator, a high performance simulation environment for SystemVerilog and OpenVera, with an integrated debugging environment. To help you ride the current recession, Axiom is offering to augment your current verification environment with seamless integration of MPSim in your environment and free peak demand licenses for 3 months.

To further boost verification productivity, Axiom is also offering a new and innovative "Plan Driven Functional Verification Closure Tool" that automatically identifies coverage points and then generates vectors to ensure complete verification closure.

Please come and see us at Booth 1815.

BEEcube, Inc.
Booth: 4307

Fremont, CA

www.beecube.com

The multicore SOC design challenge is how to provide software developers with a hardware implementation fast enough for executing binary compatible software, while allowing hardware designers to continue optimizing the final silicon implementation. BEEcube's BEE3 system provides such an environment, by integrating HW/SW co-development processes with real-time implementation of full multicore SOCs. This provides a 9-month time advantage in the development. The BEE3 systems have been deployed in many leading companies and universities worldwide, including Microsoft and Sun Microsystems.

Berkeley Design Automation, Inc.
Booth: 1620

Santa Clara, CA

www.berkeley-da.com

Berkeley Design Automation, Inc. is the recognized leader in advanced analog, mixed-signal, and RF (AMS/RF) verification. Its Analog FastSPICE unified circuit verification platform combines the accuracy, performance, and capacity needed to verify GHz designs in nanometer-scale silicon. Design teams from top-10 semiconductor companies to leading startups use the AFS Platform to efficiently verify AMS/RF circuits. Founded in 2003, the company has received several industry awards in recognition of its technology leadership and impact on the electronics industry.

Blue Pearl Software
Booth: 4100

Santa Clara, CA

www.bluepearlsoftware.com

Blue Pearl Software offers technology leading tools that help you significantly reduce design time, achieve better RTL code, and mitigate design risk. Indigo RTL Analysis offers the highest capacity, fastest performance and easiest to use linting and functional analysis capabilities. Cobalt Timing Constraint Generation and Azure Timing Constraint Validation allow designers to rapidly specify timing exceptions, and verify that constraints are valid in their design. With Blue Pearl, you will save weeks of work managing constraints and achieve faster timing closure.

Bluespec, Inc.
Booth: 3851

Waltham, MA

www.bluespec.com

Bluespec provides the only general-purpose, high-level synthesis toolset for any use model (models, testbenches, production IP) and design type (datapath, control, interconnect). Models and testbenches can be synthesized along with legacy IP to leverage emulation much earlier in the development cycle. Users get better chips to market sooner by developing software in parallel and validating architectures well before tapeout. Bluespec is the only synthesis tool built on atomic transactions, the only proven technology to manage and simplify large-scale hardware concurrency.

Breker Verification Systems
Booth: 4051

Austin, TX

www.brekersystems.com

Breker's Trek™ Scenario Modeling for Advanced Testbench Automation technology provides functional verification engineers with an automated solution for generating input stimulus, checking output results and measuring scenario coverage.

Trek is tape-out proven and demonstrates a 10X reduction in test-bench development effort with a 2X-3X improvement in overall verification productivity, allowing projects to meet today's aggressive design goals. Architected to run in your current verification environment, this technology also provides powerful graphical visualization and analysis of your design's verification space.

Cadence Design Systems, Inc.
Booth: 3751, 4300

San Jose, CA

www.cadence.com

Cadence enables global electronic-design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use Cadence® software and hardware, methodologies, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More information about the company, its products, and services online.

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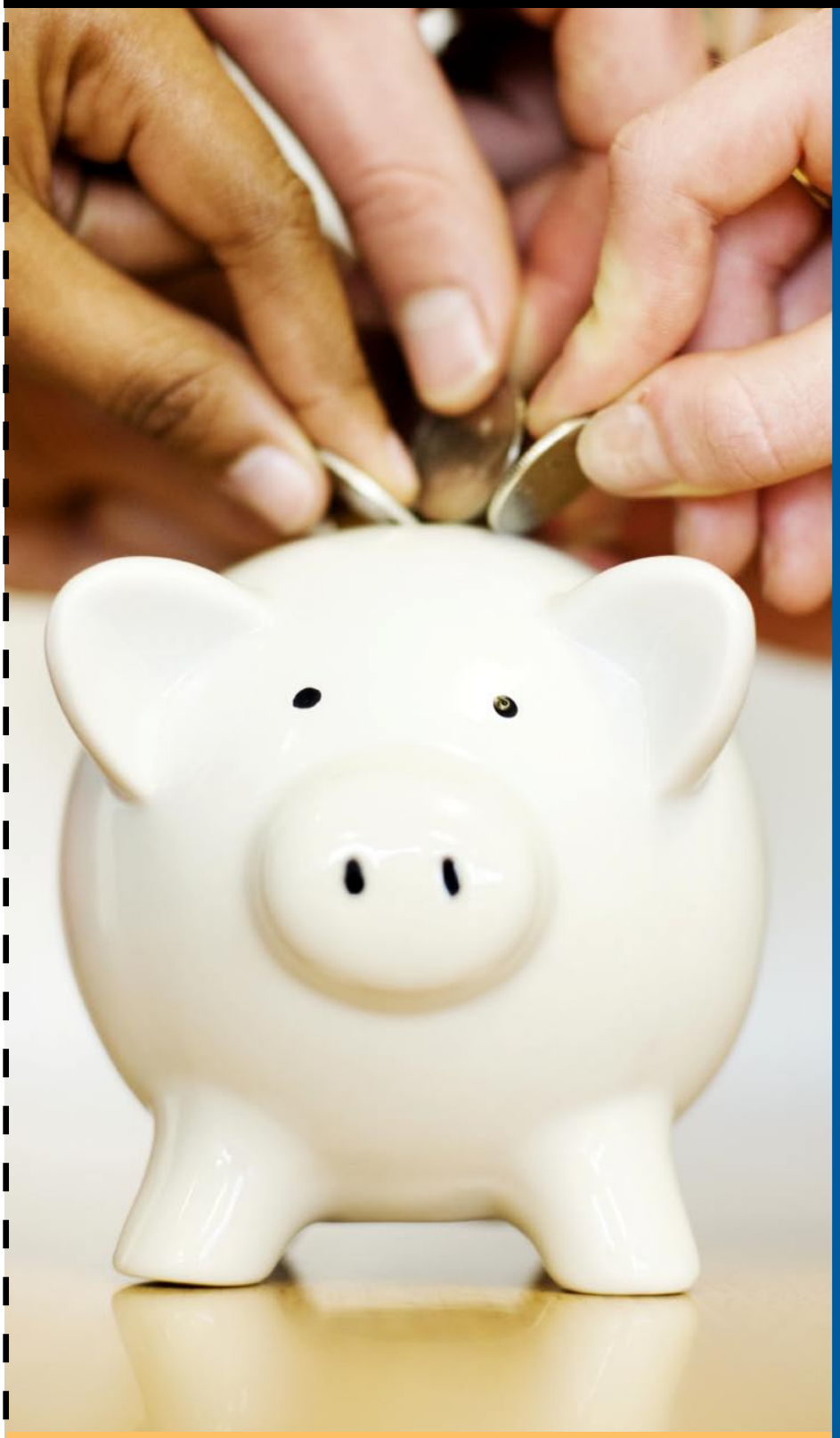

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Exhibiting Company Descriptions

Calypto Design Systems
Booth: 1610

Santa Clara, CA

www.calypto.com

Visit Calypto® Design Systems (booth #1610) to see the latest SLEC® and PowerPro™ products. Calypto empowers SoC designers to develop the highest quality, lowest power electronic systems by applying its patented sequential analysis technology to its industry leading products. PowerPro CG reduces power by up to 60% in RTL designs. Calypto's new PowerPro MG product reduces SoC memory power by introducing Memory Gating logic into the RTL design. Calypto's SLEC product family functionally verifies RTL designs and finds bugs that other tools miss.

Cambridge Analog Technologies, Inc.
Booth: 4301

Bedford, MA

www.cambridgeanalog.com

Cambridge Analog Technologies, Inc. (CAT) is a provider of leading edge ultra-low power analog circuits including ADC and PLL catering to SoCs built for a wide array of applications such as wireline, wireless, medical, automotive areas, displays, imaging and embedded control. CAT's precision ADC consume 5x-15x lower power relative to competition, and CAT's all-digital integer and fractional-N PLL serve both general purpose and ultra-high performance applications below 1ps jitter. CAT offers world-class support for its clients and partners.

Carbon Design Systems
Booth: 3359

Acton, MA

www.carbondesignsystems.com

Carbon Design Systems offers the leading system validation solution for complex system-on-chip (SoC) designs. Our solutions range from model generation and deployment to virtual platform creation, execution, and analysis. Carbon's system models provide 100% implementation accuracy on the critical components required for accurate architectural analysis and pre-silicon hardware/software validation. Solutions are based on industry standards including SystemC TLM2.0.

Carbon's industry-exclusive library of implementation-accurate ARM® processor and peripheral models are at the heart of leading-edge virtual platform designs throughout the world.

CAST, Inc.
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www.cast-inc.com

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ChipEstimate.com
Booth: 1100

San Jose, CA

www.ChipEstimate.com

Over 80,000 chip estimations have been performed by designers, architects and managers worldwide who rely on the ChipEstimate.com chip planning portal. All within one site, users can explore an extensive catalog of semiconductor IP and then download the InCyte Chip Estimator tool to predict the die size, power, leakage, performance and cost of their next chip design. Visit the ChipEstimate.com booth where you can learn about the latest in semiconductor IP from dozens of IP suppliers on the IP Talks! stage. Join us for hands-on demonstrations of IP exploration and chip estimation and learn how to estimate your next chip's size, power and cost -- in just seconds.

ChipVision Design Systems
Booth: 3555

Oldenburg, Germany

www.chipvision.com

ChipVision Design Systems helps semiconductor developers significantly reduce power consumption at the system level. Its award-winning, patented PowerOpt™ solution enables designers to accurately analyze power consumption at the system level and automatically optimize for low power while synthesizing ANSI C++ and SystemC code into Verilog RTL designs, achieving power savings of up to 75 percent compared to RTL designed by hand. The company's solutions are based on open industry standards such as ANSI C++, SystemC, UPF and CPF. For more information, please visit www.chipvision.com.

Chipworks
Booth: 4203

Ottawa, ON, Canada

www.chipworks.com

Chipworks is the recognized leader in reverse engineering and patent infringement analysis of semiconductors and electronic systems. The company's ability to analyze the circuitry and physical composition of these systems makes them a key partner in the success of the world's largest semiconductor and microelectronics companies. Visit our booth to see the fully reverse engineered circuitry of the industry's most innovative devices and get hands-on use of our tools to navigate the both the floor-plan and schematics.

Ciranova, Inc.
Booth: 4400

Santa Clara, CA

www.ciranova.com

Ciranova delivers a quantum productivity advance in custom IC layout for nanometer silicon. Ciranova customers get more complex, higher-performance analog, mixed-signal and RF ICs to market sooner and at lower cost — especially below 90nm. Ciranova PyCells are the mechanism chosen by the IPL Alliance for Interoperable PDK Libraries, and are used by TSMC in their new interoperable PDK. Ciranova Helix device-level placer slashes layout time, lets design teams optimize floorplans, and lets them see parasitics at the beginning of layout.

ClioSoft, Inc.
Booth: 3651

Fremont, CA

www.cliosoft.com

ClioSoft is the design data management solution provider of choice for the electronics design industry. ClioSoft's SOS Design Data Collaboration Platform enables efficient management of design data from concept through tape-out and improves global team productivity. Built to handle the unique demands of designers, the SOS platform gives design teams the freedom and flexibility to choose the way they work, share and collaborate. Custom engineered adaptors seamlessly integrate SOS with leading design flows -- Cadence® Virtuoso® Custom IC, Synopsys® Custom Designer, Mentor ICstudio™ and SpringSoft Laker™. ClioSoft's innovative Universal DM Adaptor technology "future proofs" design management needs by ensuring that data from any flow can be meaningfully managed.

CLK Design Automation, Inc.
Booth: 3951

Littleton, MA

www.clkda.com

CLK Design Automation is the timing synthesis technology leader. CLK's sign-off timing driven clocking and optimization solution delivers performance closure for nanometer IC designs. ClkWorks, the clocking and optimization tool suite, uses sign-off timing to reduce place and route iterations, maximize design performance, minimize power, and enhance yield. Amber, our solution for sign-off timing, SI and power, is the leader in scalable, threaded STA and SSTA. The FX model provides near-Spice accuracy for delay, SI, and process variance.

CMP
Booth: 1214

Grenoble, France

cmp.imag.fr

CMP is a manufacturing broker for ICs and MEMS, for prototyping and low volume production.

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CoFluent Design
Booth: 3151

Le Chesnay, France

www.cofluentdesign.com

CoFluent Design™ provides system-level modeling and simulation tools that enable embedded device and chip designers to imagine and validate new concepts and architectures.

CoFluent Studio™ generates SystemC transactional models from graphics and standard C that describe complex multi-OS, multicore systems in consumer electronics and telecoms.

CoFluent Reader™ enables efficient exchange of executable specifications with all project stakeholders and contractors.

Concept Engineering GmbH
Booth: 918

Freiburg, Germany

www.concept.de

Concept Engineering develops and markets innovative visualization and debugging technology for commercial EDA vendors, in-house CAD tool developers and IC and FPGA designers. Their products include, NIview Widgets - a family of schematic generation engines for EDA tool developers, SpiceVision PRO - a customizable debugger for SPICE and DSPF designs, RTLVision PRO - a graphical debugger for SystemVerilog, Verilog and VHDL designs, GateVision PRO - a customizable debugger for Verilog designs.

SGvision PRO - a mixed-mode debugger.

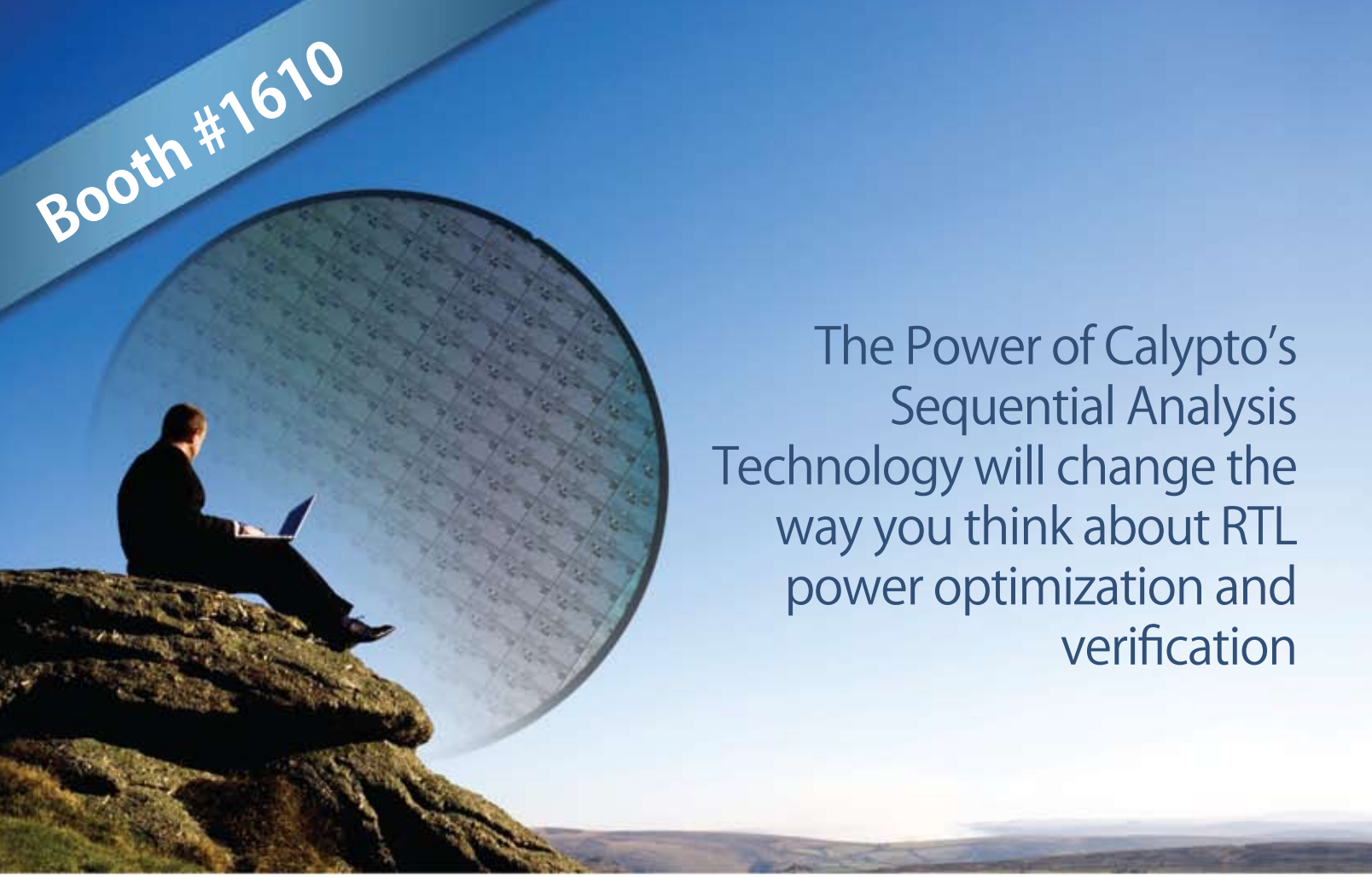
Coupling Wave Solutions
Booth: 608

Austin, TX

www.cwseda.com

Coupling Wave Solutions® (CWS) WaveIntegrity platform targets analysis and resolution of parasitic coupling between digital cores and analog or RF blocks and helps successful integration of Mixed-Signal SOCs and SIPs. WaveIntegrity offers full system noise calculations from initial system-level definitions to layout level. WaveIntegrity automatically analyzes the complete system to predict electrical aggression generated by all components, propagation through a combination of interconnects, silicon substrate and package parasitics and the impact on sensitive analog/RF blocks. The technology predicts noise budgets, supports designs having multiple power domains and integrates seamlessly into any customer flows.

Booth #1610



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PowerPro CG is an automated RTL power optimization solution that dramatically reduces power with no impact on timing or area.

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Exhibiting Company Descriptions

CoWare, Inc.
Booth: 3665

San Jose, CA

www.coware.com

CoWare is the leading global supplier of electronic system virtualization software and services. IP, semiconductor, and electronics companies use CoWare virtualization solutions to design better processor- and software-intensive products faster. CoWare solutions solve the new design challenges associated with platform architecture design, platform verification, application sub-system design, processor design, DSP algorithm design, and software development, and are based on open industry standards including SystemC. These solutions also enable IP and semiconductor companies to implement more effective go-to-market strategies.

CST of America, Inc.
Booth: 3155

Framingham, MA

www.cst.com

CST develops and markets software for the simulation of electromagnetic fields in all frequency bands. Its products allow you to characterize, design and optimize electromagnetic devices before going into the lab or measurement chamber. This can help save substantial costs especially for new or cutting edge products, reduce design risk and improve overall performance and profitability. Customers operate in industries as diverse as Telecommunications, Defense, Automotive, and Medical Equipment, and include market leaders such as IBM, Intel, Mitsubishi, and Siemens.

DAC Pavilion
Booth: 1928

Louisville, CO

www.dac.com

Open to all attendees, the DAC Pavilion brings the technical conference to the exhibit floor with a wide variety of panels and presentations featuring twenty technical, business and strategy discussions. Panels include discussions on Power, Analog, DFM, System-Level Design, IP, Multicore, Synthesis and Verification. In addition, the Pavilion offers sessions on New Media, Green Electronics, a new Community-Directed panel and the popular Gary Smith on EDA and Hogan's Heroes sessions. See pages 22-23, visit DAC.com or stop by booth 1928 for a complete schedule.

DAFCA, Inc.
Booth: 3855

Framingham, MA

www.dafca.com

DAFCA, Inc. is the premier provider of programmable IP, embedded security and software solutions that accelerate ASIC and FPGA validation and debug by providing the unique real-time ability to observe, control and analyze on-chip functional behavior. The on-chip IP also delivers unique anti-tampering and anti-counterfeit solutions protecting assets and profits against theft and unauthorized use. Leading companies around the world rely on DAFCA's solutions to increase development productivity, while also delivering reliable and secure systems to their end users.

Dassault Systemes
Booth: 716

Lowell, MA

www.3ds.com

Dassault Systèmes delivers Product Lifecycle Management (PLM) solutions to the semiconductor, high-tech/electronics, aerospace, automotive, medical device, machinery and consumer product industries. The ENOVIA Synchronicity DesignSync solutions uniquely address a rapidly emerging use for PLM by helping customers connect their electronic design environments directly to the extended enterprise. This enables globally dispersed design teams to collaborate in real time, reducing design and development costs, leveraging design expertise, improving quality and accelerating time to market. Dassault Systèmes is located in Lowell, MA.

Dataram
Booth: 1206

West Windsor, NJ

www.dataram.com

Dataram designs and manufactures reliable, high-capacity and innovative memory solutions for servers from HP, IBM, SUN, Dell, and systems with Intel and AMD processors. Dataram memory is priced up to 50% less than comparable OEM options, is guaranteed 100% compatible, and features a Lifetime Warranty. Dataram offers First-to-Market high capacity upgrades before the OEM introduces an equivalent. Plus long product lifecycles enable memory upgrades for legacy systems you plan to keep running. Visit booth #1206 to learn more about Dataram, or visit www.dataram.com

DATE 2010
Booth: 1115

Edinburgh, United Kingdom

www.date-conference.com

DATE 2010 will take place in the ICC, Dresden, Germany from 8-12 March 2010. DATE is the complete event for the European electronic system design and test community. A world-leading conference and exhibition, DATE unites 2500 professionals with 60 plus exhibiting companies, cutting-edge R&D, industrial designers and technical managers from around the world. As per previous editions the DATE 2010 conference will feature two special days. The technical paper submission deadline is 6 September 2009. Please visit our website for further details.

Denali Software, Inc.
Booth: 1424

Sunnyvale, CA

www.denali.com

Denali Software, Inc., is a world-leading provider of electronic design automation (EDA) software and intellectual property (IP) for system-on-chip (SoC) design and verification. Denali delivers the industry's most trusted solutions for deploying PCI Express, NAND Flash and DDR DRAM subsystems. Developers use Denali's EDA, IP and services to reduce risk and speed time-to-market for electronic system and chip design. Denali is headquartered in Sunnyvale, California and has offices around the world to serve the global electronics industry. More information about Denali, its products and services is available at www.denali.com.

Desaut Inc.
Booth: 1207

Santa Clara, CA

www.desaut.com

Desaut Inc. offers innovative RTL code generation products. MacroRTL 1.0 is released in 12/2008. It can generate sophisticated RTL design objects in concise macro commands. MacroRTL Pro adds a RTL Design LIbrary. Getting into RTL design cannot be easier and coding RTL design cannot be more efficient without using MacroRTL.

Design and Reuse
Booth: 1006

Grenoble, Cedex 1, France

www.design-reuse.com

Design And Reuse (D&R) was founded in 1997 to promote the Intellectual Property (IP) concept in Electronic Systems and became the worldwide leader as a B2B IP web portal: www.design-reuse.com connecting 37.000 users offering and searching for IPs. An unique database collects information about 7000 IPs dedicated to SoC design. D&R, as a software vendor, licenses an Enterprise Platform dedicated to IP packaging, IP Reuse , IP exchange (D&R intranet IP Reuse Station) to major System Design houses.

Dini Group
Booth: 914

La Jolla, CA

www.dinigroup.com

Dini Group will display the world's largest ASIC prototyping platform—the DN7020K10 with 104 million+ ASIC gates. This massive board holds 20 of the largest Altera Stratix-4 FPGAs. Also on display is the DN2002K10PCIE-M featuring new Xilinx Virtex-6 technology. Two 5 million gate SX475T FPGAs on a standard PCIe board provide unmatched speed, flexibility and expanded data flow capability.

Dini Group, founded in 1995, has supplied over 10 billion ASIC gates, they have driven prices below 1/4 Cent/ASIC gate.

DOCEA Power
Booth: 3143

Moirans, France

www.doceapower.com

DOCEA Power develops and commercializes a new generation of methodology and ESL tools for enabling faster and more reliable power and thermal modelling at system level. DOCEA Solution based on the ACEplorer® platform is a consistent approach for executing architecture exploration and optimizing power and thermal behaviour of electronic systems at an early stage of the project.

Founded in 2006 the private company DOCEA Power is based in the Grenoble area, France.

Dolphin Integration
Booth: 1314

Meylan, France

www.dolphin-integration.com

Dolphin Integration provides the best performances of your System-On-Chip thanks to:

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- SMASH All-in-One, for multi-level, multi-domain simulation.

Duolog Technologies Ltd.
Booth: 2028

Dublin, Ireland

www.duolog.com

Duolog provides EDA tools for chip integration. Our Socrates tool suite includes solutions for IP Packaging, Connectivity, Register Management and I/O Layer auto-generation. The Socrates tools all fully support IP-XACT. All tools have a powerful generator framework that auto-generates documentation and code based on user-defined templates. Standard generators include Word, HTML, VHDL, Verilog, C, C++, SystemC and SystemVerilog.

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DASSAULT SYSTEMES

Exhibiting Company Descriptions

EDA Cafe-IB Systems
Booth: 3445

Campbell, CA

www.edacafe.com

Thousands of IC, and system designers visit EDACafé.com to learn about the latest company news and research the latest design tools and services. As the #1 EDA portal it attracts more than 75,000 unique visitors each month and leverages TechJobsCafe.com to bring you targeted job opportunities. EDACafé reaches out to more than 30,000+ EDA professionals with its daily CaféNews. EDACafe will be doing video interviews of industry executives at its DAC booth. Please visit to hear all the conference buzz.

EDXACT SA
Booth: 3765

Voiron, France

www.edxact.com

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EDXACT is the only company providing independent and controlable parasitic management technologies.

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COMANCHE analyses the design interconnections extremly quickly. Its main applications are ESD validation, pre-analysis qualification and design exploration and debugging.

COMANCHE can be used with a GUI or a high performance programmable batch mode for full chip analysis.

EDXACT's tools interoperability is ensured according to partnerships with all major EDA vendors.

Elsevier
Booth: 1311

New York, NY

www.elsevier.com

Since 1984, Morgan Kaufmann has published the finest technical information resources for computer and engineering professionals. Our audience includes the research and development communities, information technology (IS/IT) managers, and students in professional degree programs. We publish in book and digital form in such areas as databases, computer networking, computer systems, human computer interaction, computer graphics, multimedia information and systems, artificial intelligence, and software engineering. Many of our books are considered to be the definitive works in their fields.

EMA Design Automation, Inc.
Booth: 3267

Rochester, NY

www.ema-eda.com

EMA Design Automation offers a full line of EDA products to meet all of your IC and PCB design needs. Featuring products from Cadence® Design Systems, EMA offers Cadence Virtuoso® custom design platform, Cadence Incisive® functional verification platform, Cadence Encounter® Conformal® Equivalence Checker, Cadence design-for-manufacturing (DFM) solutions, Cadence PSpice® analog simulation, and Cadence Allegro® and OrCAD® PCB design technologies. Visit EMA Design Automation in booth 3267.

Entasys Design, Inc.
Booth: 3863

Seoul, Korea

www.entasys.com

Entasys provides an Electronic System Level (ESL) Silicon Virtual Prototyping (SVP) solution to fill the technology gap between ESL and IC implementation designers. Architecture level and Register Transfer Level (RTL) power estimation and floorplanning enable you to predict the design problems of IC implementation and package design interface.

Entasys will demonstrate the flexible IO pad configuration including optimization of the number and the location of power pad and feasibility analysis capability for flip-chip design with power aware ESL design planning solution.

Epoch Microelectronics, Inc.
Booth:4213

Tarrytown, NY

www.epochmicro.com

Epoch Microelectronics, Inc. provides RF, Analog and Mixed signal integrated circuit design services to clients using technologies such as CMOS, SOI BiCMOS, and SiGe BiCMOS in the telecommunications, automotive & consumer electronics, and wireless markets. We work closely with our clients from specification definition stage through final support and integration, carrying out circuit design, layout, evaluation board design, testing and measurement, and debugging.

E-System Design
Booth: 408

Johns Creek, GA

www.e-systemdesign.com

E-System Design is an industry leading provider of EDA software tools for Signal and Power Integrity simulation of IC to package interconnects, highly integrated IC packages, printed circuit boards and systems. E-System Design is focused on supporting the "More than Moore" challenges facing IC package and system designers today and in the future with products that allow the designer to very accurately model system integrity and enable first pass success and fast design closure.

EVE
Booth: 908

San Jose, CA

www.eve-usa.com

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Exhibitor Forum
Booth: 4359

Louisville, CO

www.dac.com

DAC is pleased to announce the continuation of the DAC Exhibitor Forum, providing a theater venue on the exhibit floor for attendees to see focused and practical technical content from exhibitors. This exciting forum features sessions devoted entirely to a specific domain (e.g., verification) where up to three companies will be selected to present per session, followed with a short question and answer period. Visit Booth 4359 for the complete schedule.

Extension Media - Chip Design
Booth: 1408

San Francisco, CA

www.extensionmedia.com

Chip Design covers all of the technical challenges and implementation options engineers face in the development and manufacture of today's complex integrated circuits. Chip Design is the only media network dedicated to the advanced IC Design market. Visit www.chipdesignmag.com to stay informed about the latest developments in chip modeling, architecture, design, test and manufacture, from EDA tools to digital and analog hardware issues. Also, be sure and visit www.http://eecatalog.com/ for valuable information about all of Extension Media's outstanding technology resources.

Extreme DA
Booth: 1710

Santa Clara, CA

www.extreme-da.com

"Come discover the 'No Compromise' timing analysis platform from Extreme DA that delivers design closure. GoldTime gives you a breakthrough in speed and capacity, with sign-off accuracy for signal-integrity, static timing and statistical analysis. Learn how GoldTime give you the freedom to close 100M gate designs that break PrimeTime. Whether verifying timing at 65nm or yield at 40nm, the GoldTime 'No Compromise' platform delivers the right answers you need – FAST!"

Fidus Systems Inc.
Booth: 4204

Ottawa, ON, Canada

www.fidus.com

Fidus Systems Inc. develops electronic products for a wide range of industries including aerospace, defence, consumer, medical, industrial, semiconductors and telecommunications. Fidus has extensive design experience in turnkey product development and technology knowledge in System Design, Architecture, Wireless, Signal Integrity, Hardware, PCB layout, FPGA/ASIC, Software and Mechanical. Fidus has delivered on more than 700 products and projects for 140 customers across North America. For more information, please visit www.fidus.com.

FishTail Design Automation, Inc.
Booth: 3064

Lake Oswego, OR

www.fishtail-da.com

FishTail Design Automation offers a unique approach to improving chip implementation by automatically generating and verifying golden timing constraints early in the design cycle. FishTail's products allow designers to drive chip-implementation with complete constraints that are formally proven to be correct and to then manage these constraints as chip-implementation progresses. The result is a shorter chip-implementation schedule with much fewer back-end timing closure iterations. Also, by formally proving the correctness of design constraints you eliminate the risk of silicon failure resulting from incorrect timing exceptions.

Forte Design Systems
Booth: 1225

Redmond, WA

www.forteds.com

Forte Design Systems is a leading provider of software products that enable design at a higher level of abstraction. Forte's advanced SystemC synthesis technology delivers production-quality RTL in one tenth the time and eliminates downstream timing closure problems. Cynthesizer uses a high-level SystemC description to give you the flexibility to build designs with custom interfaces and challenging architectural requirements. It can automatically retarget designs to new speeds and process technologies without code changes and supports a level of reuse that is impossible at RT level. Cynthesizer is the practical, silicon-proven high-level synthesis solution you have been waiting for. Visit http://www.ForteDS.com for more information.

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Exhibiting Company Descriptions

FTL Systems, Inc.
Booth: 1215

Rochester, MN

www.ftlsystems.com

FTL Systems Auriga® HDL/ESL verification, Merlin(TM) behavioral synthesis/optimization and StarStream(TM) application-specific supercomputers take your products to the next level. Standard HDL/programming interfaces, clocked/asynchronous logic technology, digital/analog/RF/MW realization technology and multi-billion transistor/gate parallel tools from FTL Systems help you make your products reliable and unique. Established in 1994, FTL Systems products are on the cutting edge of the EDA industry.

GateRocket, Inc.
Booth: 3550

Bedford, MA

www.gaterocket.com

GateRocket is the only company that focuses exclusively on verification and debugging solutions for today's most advanced FPGAs. GateRocket's products work seamlessly with your existing HDL simulation environment to boost verification throughput and identify bugs in your RTL, IP and tool flow that would otherwise slip through to your system-integration lab. GateRocket's unique Device Native® architecture exploits the speed and flexibility of FPGA hardware to turbo-charge and extend your software simulation environment, shaving months off your verification and debugging schedule.

GiDEL
Booth: 810

Santa Clara, CA

www.gidel.com

GiDEL is a successful, profitable and innovative company which was founded in 1993. GiDEL has become one of the market leaders as a company that continuously provides cutting-edge reconfigurable technology utilizing FPGAs. Customers in semiconductor, consumer product, communications, machine vision, medical imaging, and military/aerospace markets purchase the PROC family of reconfigurable PROCessors (1) for SoC and ASIC verification, (2) as COTS (Commercial Off-The-Shelf) acquisition and accelerator boards, and (3) to validate complex algorithms. For more information, contact GiDEL in North America at 408-969-0389, or on the web at www.gidel.com.

Gradient Design Automation
Booth: 2024

Santa Clara, CA

www.gradient-da.com

Gradient Design Automation pioneered accurate, fine-grain IC thermal simulation that produces a 3-dimensional temperature map of a chip or stacked-die SiP. Our products fit into the standard EDA flows, and help to reveal thermally induced circuit failures and performance degradations before tapeout, so that corrective actions can be taken. By adding temperature-awareness to the design ecosystem, Gradient improves electrical simulation accuracy and reveals opportunities to neutralize the temperature effects as well as improve the chip design.

Helic, Inc.
Booth: 1824

San Francisco, CA

www.helic.com

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For more information you can visit our website www.helic.com

Hewlett-Packard Co.
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IBM Corp.
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Armonk, NY

www.ibm.com

IBM Rational is a premier provider of solutions for software, systems and products. The Rational Systems and Software Delivery Platform, which has been recently enhanced with the acquisition of Telelogic, features an open and extensible portfolio to help companies manage the complexity of development across the entire lifecycle of software, systems or products. IBM Rational delivers an integrated suite of tools and methods for systems and software development - from requirements management, to modeling and testing.

IC Manage, Inc.
Booth: 1810

Los Gatos, CA

www.icmanage.com

IC Manage, Inc. provides enterprise level design management solutions for IC development, enabling companies to efficiently and reliably manage single and multi-site design efforts. IC Manage's Global Design Platform (GDP) – utilizing the Perforce Fast SCM engine – offers design assembly and derivative management in addition to scalable, high performance revision control and configuration management. IT infrastructure integration for backup, high availability and disaster recovery is also available. IC Manage is headquartered at Suite 100, 15729 Los Gatos Blvd, Los Gatos, CA 95032. (www.icmanage.com).

IMEC / Europractice
Booth: 820

Leuven, Belgium

www.europractice-ic.com

The EUROPRACTICE IC service offers low cost and easy access to ASIC prototyping and small volume fabrication in industrial CMOS processes from 0.8µ to 40nm at well-known foundries (ONSemi, austriamicrosystems, IHP, TSMC,UMC, Faraday). A total manufacturing flow is offered (cell library, design kit access, support, deep submicron RTL-to-layout, prototyping, volume fabrication, qualification, assembly and test).

Imera Systems, Inc.
Booth: 3964

San Jose, CA

www.imera.com

Imera Systems is the global leader in network virtualization solutions for enterprises. Imera SAVI™ Platform features a secure and auditable virtual network infrastructure that enables EDA vendors to instantly debug and resolve customers' tool problems without IP leakage, resulting in higher tool availability, lower support costs and more compressed design cycle.

Incentia Design Systems, Inc.
Booth: 808

Santa Clara, CA

www.incentia.com

Incentia will showcase its powerful static timing analysis and design closure tool suite. Anchored by its high-speed, industry proven TimeCraft™ STA, the tool suite includes stage & location based on-chip-variation, signal integrity, statistical STA, constraint checker & debugger, and post-layout hold time & leakage power ECO. Using Incentia's multi-task and multi-thread technologies, more modes and corners can be run in parallel, greatly reducing total turnaround time.

Learn our tool advantages and customers tape-out success. Incentia – More Corners in Less Time!

Infiniscale
Booth: 3065

Grenoble-Montbonnot, France

www.infiniscale.com

InfiniScale is the unique worldwide expert EDA Company in behavioral Modeling and Model-Based solutions.

Our exclusive behavioral modeling innovation, based on a 2nd generation of intelligent Design-of-Experiment technology, makes possible today the modeling of very complex and highly non-linear phenomena. Modeling the behavior of a SEU, a passive or a MEMS including resonances, …. is possible for the first time. The model-based analysis or sizing thus takes only some minutes.

Designing an analog circuit in sub 100nm technologies with important process variability, mismatch and environment become too sensitive to be treated by hand or by too costly simulator-based solutions! The need for new tools is indispensable. Our DFY solution is unique by offering a model-based approach helps analog designers:

• exploring and analyzing their design in minutes • Sizing in minutes • yield & robustness optimization in Hour Come and visit us at DAC'09 to see an impressive innovation!!

Infotech Enterprises Electronic Design Services, Inc.
Booth: 711

San Jose, CA

www.infotech-enterprises.com

Infotech Enterprises Electronic Design Services, Inc. (Formerly known as Time To Market, Inc) is an ASIC design services company from San Jose, USA, with headquarters in Hyderabad, India. "Infotech EEDS" specializes in RTL Design/ Verification, ASIC physical design, DFT, and Embedded software solutions. IEEDS enables our customers to implement an in-house COT strategy by providing required interfaces to packaging, testing and foundry. The company has completed over 140 ASIC projects for leading semiconductor companies in the consumer, networking, and communications markets.

Innovative Logic Inc.
Booth: 1306

Santa Clara, CA

www.inno-logic.com

Innovative Logic is the fastest growing technology services company providing high quality and reliable design services in ASIC, FPGA, and Embedded Systems Design. Our flexible business model allows you to choose onsite, offsite, or offshore consulting. We have expertise in Logic Design & Verification, Design for Testability (DFT), Circuit Design, Physical Design & Verification, Board Design, and FPGA Design. Innovative Logic has a world class team of engineers who have successfully executed different projects using the latest tools and the technologies. Innovative Logic is headquartered in Santa Clara, CA and has state of art Design Centers in Bangalore, India. For details, please visit our website at www.inno-logic.com .

conference and exhibition

COME AND VISIT US AT BOOTH 1115

DATE 10

Dresden, Germany
March 8 - 12, 2010

The 13th DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. It puts strong emphasis on both ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.

Structure of the Event

The five-day events consists of a conference with industry keynotes, regular papers, panels, hot-topic sessions, tutorials, workshops, two special focus days and a management track. The scientific conference is complemented by a commercial exhibition showing state-of-the-art in design and test tools, methodologies, IP and design services, reconfigurable and other hardware platforms , embedded software, and industrial design experiences from different applications domains, such as automotive, aeropsace, wireless, telecom and multimedia applications. The organisation of user group meetings, fringe meetings, a university booth, research project demonstrations, a PhD forum, and social events offers a wide variety of opportunities to meet and exchange information on relevant issues for the design and test community.

Areas of Interest

Within the scope of the conference, the main areas of interest are: embedded systems, design methodologies, CAD languages, algorithms and tools, testing of electronic circuits and systems, embedded software, applications design and industrial design experiences. Please visit the DATE website for a list of the topics of interest for DATE 2010.

Submission of Papers

Papers can be submitted for standard oral presentation or for interactive presentation. All papers have to be submitted electronically before **September 6th, 2009,** via the conference web page: **www.date-conference.com**

Chairs

General chair:
Giovanni De Micheli, EPFL, Lausanne, Switzerland,
Email: giovanni.demicheli@epfl.ch

Programme chair:
Wolfgang Mueller, University of Paderborn, Germany
Email: wolfgang@acm.org

DATE Secretariat - European Conferences Sue Menzies, 3 Coates Place, Edinburgh EH3 7AA, United Kingdon
Tel: +44 131 225 2892 • **Fax:** +44 131 225 2925 • **Email:** sue.menzies@ec.u-net.com

www.date-conference.com

Photo by Christoph Münch

Exhibiting Company Descriptions

iNoCs
Booth: 4303

Lausanne, VD, Switzerland

www.inocs.com

iNoCs is the supplier of next-generation on-chip interconnection technology for System-on-Chips, multicore products and FPGAs. Founded by a pioneering team in Networks-on-Chips, iNoCs develops NoC design tools and NoC RTL IP libraries to tackle on-chip communication demands quickly, efficiently and in a plug&play fashion. Advantages include much faster timing closure; improved product time-to-market; reduced design effort; scalable performance; easy integration with existing EDA flows.

Instigate
Booth: 3449

Portland, OR

www.instigatedesign.com

Instigate provides services in the following two major areas:

Electronic System Level design and verification

- Transaction level modeling
- Hardware-software codesign
- Early hardware-software trade-off

Software design and verification

- EDA
- Algorithmic software
- High performance computing
- Embedded/mobile applications

Instigate also reduces development costs for its customers by deploying its internally developed EDA Application Framework for rapid development of applications.

Instigate has served nearly 30 customers to date throughout Europe and North America and has over 100 employees.

Institution of Engineering and Technology
Booth: 1308

Edison, NJ

www.theiet.org

The Institution of Engineering and Technology is one of the world's leading professional societies for the engineering and technology community with over 150,000 members. The IET is a producer of science and technology resources including books, research journals, conference proceedings and electronic databases (Inspec & more). Please visit www.theiet.org for ordering and pricing information on all of our products.

InternetCAD.com, Inc./Timberwolf Systems
Booth: 1208

Dallas, TX

www.internetcad.com

Internet CAD, Inc. is proud to present Itools, a complete timing-driven placement and routing package that will not break your bank. Itools is capable of placing and routing any design style with impressive results. New enhancements are always being added which are included in one extremely low subscription price. Why pay more and get less? See a demonstration of Itools and learn how it can save you a fortune with all your IC designs.

Interra Systems, Inc.
Booth: 1316

Cupertino, CA

www.interrasystems.com

Interra Systems is a broad-based software products and services provider in Design Automation and Digital Media industries. Interra Design Automation solutions are led by Memory development system (MC2), standards-compliant EDA building blocks (EDA Objects) and HDL coverage test suites. EDA Objects from Interra have been in production use for over fifteen years. They include Verilog/VHDL parsers, elaborator, and synthesis engine. Products and Services from Interra are differentiated by deep engineering knowhow and proven track record in working with customers. www.interrasystems.com

Jasper Design Automation, Inc.
Booth: 3767

Mountain View, CA

www.jasper-da.com

Jasper Design Automation offers high-value solutions for the design and verification of semiconductors and electronic systems, based on formal technologies. Jasper delivers advanced formal technology, software and services to the global electronics market including consumer, wireless, computing, network, graphics, and other markets. Flagship products JasperGold and ActiveDesign give customers a competitive advantage by delivering value throughout the design cycle, with targeted ROI effects. Headquartered in Mountain View, California, Jasper is privately held and has offices and distributors in North America, South America, Europe, and Japan. Visit Jasper for Formal Verification Unleashed: http://jasper-da.com.

Jspeed Design Automation, Inc.
Booth: 817

San Jose, CA

www.jspeedda.com

Jspeed Design Automation, Inc. is specialized in routing large-sclae flat designs. The company's flagship product, JaguarRoute (JRoute), is a cutting-edge IC router for both standard and custom cell designs with process technology of 65 nm and below. Currently, it accepts both placed or partially routed designs, and is capable of fixing geometry related violations created by other routers. Our technology can handle flat designs of an almost unlimited size, and reduce the wire count up to 50%, via count 10%, and runtime 93% (14X). With its superior scalable performance, JRoute will outperform most routers on the market.

Kilopass Technology, Inc.
Booth: 1514

Santa Clara, CA

www.kilopass.com

Kilopass is a leading supplier of embedded non-volatile memory (NVM) IP, manufactured in standard logic CMOS process. Kilopass's embedded NVM technology, XPM or Extra Permanent Memory, delivers highly reliable, secure, and cost-effective one-time programmable (OTP) solutions for SOC applications, including electrically field-programmable firmware storage, security IDs and/or keys, analog circuit calibration, yield enhancement, self-repair, and IC configuration. Kilopass has over 60 customers from 0.18um to 40nm in over 150 designs, 70% of which are in high volume production. Kilopass embedded NVM product lines include XPM™, SnapXPM™, and BriteXPM™.

Laflin HOTSCOPE
Booth: 3448

Portland, OR

www.laflinltd.com

Laflin/HOTSCOPE introduces its latest updates of HOTSCOPE V7.4.0 including:

Performance improvements (since V7.2.0):

- GDS2: 2X faster (Open)
- OASIS: 1.6X faster (Open), 10X-200X faster (Viewing)
- LEFDEF: 2X faster (Open), 3X-10X faster (Viewing)

New functionality including:

- Coloring (used in CMP Simulation Analysis for example)
- Cross-section Viewing
- Mesh-based Image Checking
- OASIS Utilities
- CD Checking Utilities

Prototypes of Node DRC/Trace/Handling capabilities will also be on display.

HOTSCOPE is a high performance GDS and mask data browser developed by DNP and JEDAT of Japan and distributed by Laflin Limited in the U.S..

Legend Design Technology, Inc.
Booth: 1510

Santa Clara, CA

www.legenddesign.com

Legend Design Technology offer a total solution for IP characterization and circuit simulation products.

CharFlo-Memory! and CharFlo-Cell! provide timing and power characterizations for memories, standard cells and I/Os libraries. Model Diagnoser enables designers to check on standard cells and I/Os reliability and manufacturability to ensure first-silicon success.

MSIM and Turbo-MSIM delivers the package solution for circuit simulation either for spice-level accuracy, or full-chip functional verification for large SoC designs.

Library Technologies, Inc.
Booth: 1714

Saratoga, CA

www.libtech.com

Exhibiting ChipTimer, Timing Closure Tool, 30-200% speed-up, 10% area reduction using special techniques and custom CellOpt generated libraries; SolutionWare, Cell, IO and Memory Characterization-Modeling for Timing, Power, SI, CCS and ECSM; automatic verification including memories; CellOpt, timing and power Optimizer for cells and simple blocks like adders and multipliers; YieldOpt, statistical process variation analyzer which does away with SSTA and Monte-Carlo; PowerTeam: dynamic gate level power Verilogbased simulator using special libraries generated by SolutionWare; UnBlock/RcBack for custom block modeling and RC back-annotation.

Logic Perspective Technology Inc.
Booth: 3257

Milpitas, CA

www.logicperspective.com

Logic Perspective Technology Inc. pioneered low power design gate / physical level verification through its breakthrough GSIM simulator product, the fastest, most efficient gate/physical level simulator on the market, achieves 75X speed up at power aware modeling on a quad core system and handles 200 million gates within 4GB memory at run time. Its power analysis capability offers a painless flow to find real hot spot to guide your power planning and power analysis at sign off. GSIM solution also enables low power design IP distribution for more effective go-to-market strategies.

The Network For Advanced IC Designers

Magazines

In-depth coverage of all the technical challenges and implementation options that engineers face in the development and manufacturing of today's complex integrated circuits (IC)

Resource Catalogs

Locate vendors and products including IP, ASIC's, FPGA's, SoC, EDA tools, design services and more

Websites

Online source for the latest tools, technologies and methodologies to better navigate the challenges that face modern IC design environments

Email Newsletters

Email newsletters and online periodicals with news, commentary and analysis

Market Research

Valuable market intelligence on Chip Design trends

www.chipdesignmag.com

Exhibiting Company Descriptions

LogicVision, Inc.
Booth: 1614

San Jose, CA

www.logicvision.com

LogicVision provides proprietary built-in-self-test (BIST) technologies for achieving the highest quality silicon manufacturing test while reducing test costs for complex SOC devices. BIST functionality automatically integrated into the design is used during semiconductor production test and throughout the useful life of the chip. LogicVision's complete Dragonfly Test Platform™, including the ETCreate™, Silicon Insight™ and Yield Insight™ product families, improves profit margins by reducing device field returns and test costs, accelerating silicon bring-up times and shortening both time-to-market and time-to-yield.

Lynguent, Inc.
Booth: 4060

Portland, OR

www.lynguent.com

Lynguent®, Inc. enables innovation by breaking through the traditional barriers in the design and verification of complex analog and mixed-signal (AMS) electronic systems and components. Customers, using Lynguent's productivity tools, are able to rapidly create and validate AMS models; efficiently bridge system and circuit design; and encapsulate the AMS portion of their design so that it can be used in their existing digital simulator. Lynguent also provides expert consulting and modeling services.

Magillem Design Services
Booth: 3348

Paris, France

www.magillem.com

Magillem has developed an easy to use, state of the art platform to cover electronic systems design flow challenges in a context where complexity, interoperability and design re-use are becoming critical issues to manage design cycle time of SOC. Main benefits include:

- Maximizing Design and IP Re-use
- Using a virtual platform to configure their system and IPs
- Controlling the Design Flow
- Exploring their Design Flow architecture and optimizing it
- Improving their independence from CAD tools vendors
- Relying on worldwide adopted standards

Magma Design Automation, Inc.
Booth: 1414

San Jose, CA

www.magma-da.com

Get on the Fastest Path to Silicon™ with Magma. For digital implementation, our 40-nm-proven Talus® system delivers the fastest turnaround on the largest most complex SoCs and includes advanced technologies for low-power design. The Quartz™ tools provide superior runtime and read files from third-party DRC/LVS tools. The Titan™ system accelerates analog design migration. FineSim™ enables fast, accurate simulation of the most challenging analog designs. And, only Magma integrates analog and digital implementation, circuit simulation, and verification – providing a quantum leap in designer productivity.

Magwel NV
Booth: 3357

San Jose, CA

www.magwel.com

Magwel's Power Transistor Modeling solution simulates very large power transistor arrays to extract resistance and analyze electro-migration with 3-D accuracy and unprecedented speed. Substrate Noise Modeling solution models noise injection, propagation and coupling in large critical layouts. 3-D Parasitic Extraction Tool extracts R, L and C on large critical nets.

3-D simulation technology co-simulates semiconductors together with metal.

Circuit optimization and modeling solutions provide high quality, robust circuit sizing and performance modeling for cell libraries with statistical process variations.

MathWorks, Inc. (The)
Booth: 3565

Natick, MA

www.mathworks.com

The MathWorks is the leading developer and supplier of software for technical computing and Model-Based Design. Over 1,000,000 engineers and scientists in more than 100 countries, on all seven continents, use MATLAB® and Simulink®. These products have become fundamental tools for work at the world's most innovative technology companies, government research labs, financial institutions, and at more than 3,500 universities. Employing more than 2,000 people, The MathWorks was founded in 1984 and is headquartered in Natick, Massachusetts, with offices and representatives throughout the world.

McGraw-Hill Professional
Booth: 818

New York, NY

www.mhprofessional.com

If information is the gateway to success in today's global economy, McGraw-Hill is the gatekeeper. McGraw-Hill Professional enables technical and trade professionals to succeed in complex global industries by structuring the most current information into concise and authoritative resources. Visit us at booth #818 for special offers and much more! www.mhprofessional.com

Mentor Graphics Corp.
Booth: 3567

Wilsonville, OR

www.mentor.com

ntor Graphics is a technology leader in electronic design automation, providing software and hardware design solutions focused on IC design, place & route, physical verification, functional verification, FPGA/PLD, silicon test and yield analysis, PCB design, embedded software and emerging technologies such as ESL design and verification, system modeling and thermal analysis. Our innovative solutions solve demanding design challenges such as low power and manufacturing variability in the most comprehensive way.

Mephisto Design Automation
Booth: 521

Leuven, Belgium

www.mephisto-da.com

Mephisto Design Automation (MDA) delivers unique analog, mixed-signal and custom-digital design automation solutions based on its flagship platform M-DESIGN™. This flexible tool allows both novice and expert designers to significantly improve circuit performance, productivity and circuit understanding. Including capabilities such as advanced testbench composition, embedded scripting, an extensive toolbox and patent-pending multi-level optimization, M-DESIGN is the tool of choice for the simulation, sizing, optimization, verification and migration of analog, mixed-signal and custom digital designs and IP. More information is available at www.mephisto-da.com.

Methodics LLC
Booth: 1924

San Francisco, CA

www.methodics-eda.com

VersIC is the highest performance design data management solution available for the Cadence design environment. Its open architecture allows it to benefit from the latest generation SCM tools (Subversion and Perforce and Clearcase) used by millions of software developers worldwide, making VersIC the most robust and bug free solution available today.

VersIC includes "DM Enabled" design tools that add value to the DM platform including Visual Schematic/Layout Diff and Merge tools, Design Review tools, Continuous Integration tools for Mixed-Signal designs.

Micro Magic, Inc.
Booth: 1219

Sunnyvale, CA

www.micromagic.com

MMI Advanced EDA Tools are built by IC designers for IC designers, are easy to learn and use, and are field proven. For design entry and layout, Micro Magic tools ensure consistent, dependable performance for the most demanding IC designs.

Micrologic Design Automation
Booth: 3249

Haifa, Israel

www.micrologic-da.com

Micrologic Design Automation, Inc. develops physical verification systems to detect and eliminate design violations early during IC layout design stages, enabling integrated circuit corporations to meet or shorten time-to-market objectives, improving designs quality, reliability and performance.

Mirabilis Design Inc.
Booth: 3345

Sunnyvale, CA

www.mirabilisdesign.com

Mirabilis Design provides systems engineering solutions for performance analysis, power estimation and architecture exploration of electronics and real-time software. The product, VisualSim, starts prior to ESL for project feasibility, selection of the right platform and establish cost, schedule, size and power. The output of VisualSim is a specification for development and marketing; and an environment for early software prototyping and system verification. VisualSim is a graphical, environment where designers construct models using pre-built parameterized and custom components. VisualSim accelerates system design and virtual prototyping by over 12X i.e. 6 months to 15 days.

Mixel, Inc.
Booth: 3454

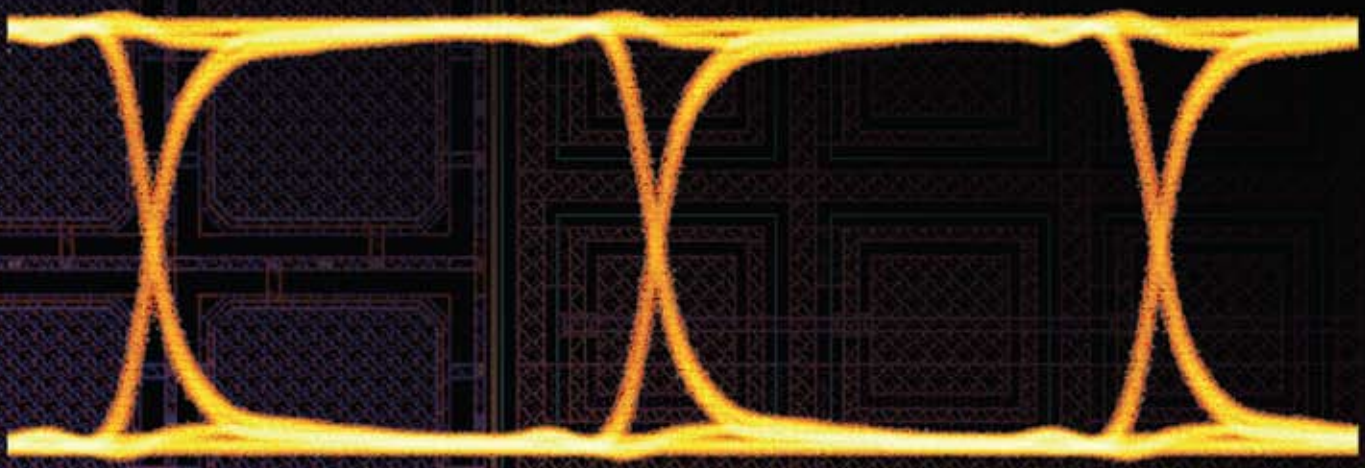
San Jose, CA

www.mixel.com

Mixel is a leading provider of Silicon-proven mixed-signal IP cores to the semiconductor and electronics industries. Mixel licenses high-performance analog and mixed-signal IP cores to the communications, consumer and storage markets for use in system-on-chip, ASICs and embedded systems.

Mixel's mixed-signal IP portfolio includes high performance PHYs, SerDes, PLLs, DLLs, and analog building blocks. They are used in Mobile applications such as MIPI, and MDDI, networking and storage applications such as PCI-Express, SATA, XAUI, Back-Plane, Fibre-Channel, and a variety of transceivers such as LVDS, DDR2, PCI-X, SSTL, HSTL, CE-ATA, CardBus, and Parallel-ATA. Mixel technology has been deployed in products designed by several first-tier players in the high-tech industry, as well as innovative and up-and-coming startup companies.

Let Our Eyes Catch Yours



Mobile
- MIPI
- MDDI

Timing
- Frequency Synthesis
- Spread-spectrum
- De-skewing
- CDR

Storage & Networking
- PCI-Express
- XAUI
- Fibre-Channel
- SATA
- GPON

Interface
- LVDS
- CE-ATA
- CardBus
- PATA
- DDR2
- SSTL
- HSTL
- PCI-X

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www.Mixel.com

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Exhibiting Company Descriptions

MOSIS Service (The)
Booth: 1415

Marina del Rey, CA

www.mosis.com

MOSIS offers designers worldwide IC prototyping, medium-quantity, and low-volume production (e.g. dedicated run) fabrication services. Packaging, including flip-chip, and functional testing are available. Available processes include

- TSMC 65nm, 90nm, 130nm, 180nm, 250nm, 350nm
- IBM SiGe BiCMOS (to 130nm), CMOS (to 45nm)
- ON Semi (was AMI) 350nm, 500nm, 700nm
- austriamicrosystems 350nm HV CMOS

MunEDA GmbH
Booth: 3867

Munich, Germany

www.muneda.com

MunEDA provides leading EDA software technology for analysis, modelling and optimization of yield and performance of analog, mixed-signal and digital designs. MunEDA´s products and solutions enable customers to reduce the design times of their circuits and to maximize robustness, reliability and yield. MunEDA´s solutions are in industrial use by leading semiconductor companies in the areas of communication, computer, memories, automotive, and consumer electronics.

Nangate
Booth: 3265

Herlev, Denmark

www.nangate.com

Nangate offers software and services for physical library IP creation, characterization, optimization and validation.

By ensuring that the digital cell library exactly fits the application, IC power consumption, yield loss and costs can be significantly reduced and performance increased.

The Nangate software suite brings together all required cell library design disciplines to achieve these benefits with the tool chain seamlessly integrating with SoC design flows from the major EDA vendors.

NextOp Software, Inc.
Booth: 903

San Jose, CA

www.nextopsoftware.com

Nusym Technology, Inc.
Booth: 622

Los Gatos, CA

www.nusym.com

Nusym Technology provides significant improvement in verification productivity by using design insight to enable rapid verification closure. This approach requires little change in current verification methodologies. Nusym maximizes coverage for a given testbench and provides feedback on what to change to get better coverage. Currently being used on a number of leading edge designs at our semiconductor partners before general release.

Oasys Design Systems, Inc.
Booth: 3061

Santa Clara, CA

www.oasys-ds.com

When designing a 20M gates or larger chip, the "Chip Synthesis" product from Oasys Design Systems is a must see at this years DAC show. This revolutionary technology can handle the full chip RTL, timing constraints and floorplan. It produces placed gates in record time (20X - 40X faster) and with the best QoR! No floorplan? Then we will automatically place the macros and create a floorplan. Intrigued? Come and see for yourself.

OneSpin Solutions GmbH
Booth: 3465

Munich, Germany

www.onespin-solutions.com

OneSpin's 360 MV product family mainstreams formal assertion-based verification (ABV) for ASIC and FPGA designs. It supports the broadest range of use cases – from early RTL analysis all the way to highest quality gap-free verification – for design, verification, and integration engineers, saving testbench development effort and achieving early verification closure. Visit Booth #3465 to see our tutorials "Get Going in a Day - Use Cases for Formal ABV Starters" and "Get More for Less - Advances in SVA-based Formal ABV".

OptEM Engineering Inc.
Booth: 3351

Calgary, AB, Canada

www.optem.com

OptEM Engineering's software and services focus on interconnect design, extraction, modeling and analysis for high-speed analog, digital, and mixed-signal ICs and cable/connector systems. For deep-submicron ICs, the OptEM Inspector software provides layout-to-circuit device extraction, and 2-D/3-D substrate and interconnect RC extraction for detailed analysis of crosstalk and delay effects at the cell level. For cable/connector systems, the OptEM Cable Designer software models high-performance multi-conductor flex, twisted-pair, and specialty cables in telecommunication and data transmission applications.

Optiwave Systems Inc.
Booth: 916

Ottawa, ON, Canada

www.optiwave.com

Optiwave is the leading provider of innovative circuit design software for analysis of integrated circuits including interactions of optical and electronic components. Design opto-electronic circuits at the transistor level, from laser drivers to transimpedance amplifiers, optical interconnects, and electronic equalizers. To download our software for a free evaluation, please visit our online resource center at optiwave.com.

Orora Design Technologies, Inc.
Booth: 4151

Redmond, WA

www.orora.com

Leading analog design automation, ODT will roll out Arana Custom-IC Behavioral Modeling Platform at DAC09.

Arana automatically extracts and validates Verilog-A/AMS behavioral models from SPICE netlists. Tested on over 40 complex mixed-signal IC production circuits including PLL, ADC/DAC, SerDes, and DC-DC converters, Arana offers 100x-1000x speedup over SPICE, and is the industry's only solution for mixed-signal functional verification.

OVM World
Booth: 3450

www.ovmworld.org

The Open Verification Methodology (OVM) is the industry's only truly open and interoperable solution, guaranteed to run on multiple leading simulators and supporting multiple languages. The OVM fosters easier verification reuse and the development of plug-and-play verification IP. OVM World (www.ovmworld.org) is a one-stop site for OVM news and information as well as downloads of the OVM open-source library, documentation, and extensive community contributions. The OVM World booth will feature partners and users from this community sharing their OVM successes.

Pextra
Booth: 1825

College Station, TX

www.pextracorp.com

For the first time, full-chip RC extraction using a field solver becomes possible. With PexRC you can extract interconnect parasitics that match silicon within 3%, instead of the 10-30% from traditional pattern matching LPE tools, yet the extraction speed of PexRC rivals that of pattern matching tools. Proven by the industry and highly ranked by the experts, PexRC is the next generation LPE tool for high performance circuits.

Physware, Inc.
Booth: 1814

Bellevue, WA

www.physware.com

Physware is a provider of high-speed 3-D fullwave solutions that enable broadband verification and design across the chip-package-board ecosystems at unprecedented speed and capacity. Today, Physware helps customers solve their SI, PI, EMI and SNI challenges in a variety of design areas including memory, wireless RF systems, high-speed serial and parallel channels, FPGAs, analog systems and microprocessors. Speedups of 10x for SI and PI, and 100x for EMI over competing 3-D field solutions are observed by several customers.

PLD Applications (PLDA)
Booth: 511

Aix-en-Provence, France

www.plda.com

PLDA designs and sells a wide range of FPGA and ASIC interfacing solutions for USB, PCI and derivative markets (PCI Express, PCI-X and CompactPCI)

We provide complete solutions to a global market, including IP cores, hardware, software, consulting services, and technical support provided by the IP designers.

Our success is driven by our expertise in designing IP Cores and related boards for ASICs, Structured-ASICs, and FPGAs.

Founded in 1996, PLDA products are available worldwide through a strong distribution network. www.plda.com

POLYTEDA Software Corp.
Booth: 814

Toronto, ON, Canada

www.polyteda.com

POLYTEDA Software Corporation flagship product is a unique next-generation physical verification tool PowerDRC/LVS to handle challenges of deep sub-micron manufacturing processes.

- Processing speed: checking 2 billion transistor design on full rule deck on 64 CPUs takes 1 hour of runtime
- Maximum size of designs: up to 30 billion transistors
- Supported manufacturing technologies: 65/45/32-nm
- Scalable to support future technologies - 28/22 nm and below

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Exhibiting Company Descriptions

Prentice Hall Prof. / Pearson Education
Booth: 909

Upper Saddle River, NJ

www.prenhallprofessional.com

PH Professional and PH College ESM description for DAC 2009.

Prentice Hall Professional and PH Higher Education, divisions of Pearson Education, are amongst the world's largest and most well respected publishers of professional and educational computer science and engineering books. Our products are authored and developed by the most prominent technology experts in their respective fields. Some of our products on display will include: books in our highly regarded Modern Semiconductor Design Series and Signal Integrity Library. For more information, visit www.prenhallprofessional.com.

Prolific, Inc.
Booth: 3543

Newark, CA

www.prolificinc.com

Prolific's products automate physical design optimization. ProPower® and ProTiming™ run after any place-and-route flow, reducing leakage power by 25%-70% on previously optimized designs, and improving TNS and WNS by an average of 10%. ProGenesis® automatically produces standard cell layout, including completed 32nm libraries. It reduces development time, allows architectural exploration, and adapts to changes in design requirements or rules automatically. This year, Prolific unveils its DFM optimization tool, which designs in manufacturability at the right time: library creation.

Pulsic Ltd.
Booth: 815

Bristol, United Kingdom

www.pulsic.com

Pulsic's Unity™ is a complete custom design automation solution for the physical design. Unity combines four key components -UniPlan™ (hierarchical floorplanning), UniPlace™ (placement), UniRoute™ (routing) and UniEdit™ (editing) - with UniSignal/Timing, Signal Integrity, incremental and hierarchical ECO to provide a design environment for high productivity.

Pulsic has delivered successful tapeouts at 45nm and below for IDMs and fabless customers in the memory, FPGA, custom digital, LCD, Imaging and analog/mixed signal markets for over 45 customers worldwide.

QThink, Inc.
Booth: 1216

San Diego, CA

www.qthink.com

QuantumThink Group, Inc. offers ASIC and SoC design services to leading edge semiconductor companies involved in wired and wireless communications, high-speed networking, multimedia, high-speed computing, medical and military applications. Services include: Design-flow engineering and implementation • System Level Modeling and Design Exploration • Hardware/Software Co-Verification • Embedded Software Development • Micro Architecture Design • Logic synthesis • Design for test • Timing analysis • Formal verification • Floor-planning and chip integration • Physical design place and route • Signal integrity analysis • Physical verification • Post tape-out manufacturing management • Professional project management.

QThink has offices in San Diego, San Jose, and Bangalore, India.

R3 Logic Inc.
Booth: 813

Waltham, MA

www.r3logic.com

R3Logic, world leader in EDA for 3-D system and IC design will showcase its latest tools for heterogeneous IP integration. Come view R3Integrator for package-interposer-chip codesign, TSV automation, routing and verification.

Real Intent, Inc.
Booth: 1728

Sunnyvale, CA

www.realintent.com

Real Intent, Inc. delivers verification confidence by providing automatic verification solutions for ASIC and FPGA designs. Through innovation and unique application of formal techniques, the Real Intent tools provide powerful solutions to important design and verification problems. Exhibited products at DAC include Meridian CDC for Clock Domain Crossing verification; Ascent for early functional verification; and PureTime for false and multi-cycle paths verification. In use at over 40 major customers worldwide, Real Intent tools help make the most complex designs possible.

Reed Business Information
Booth: 1209

Waltham, MA

www.reedbusiness.com

EDN is published by Reed Business Information and for more than 50 years has served the vital information needs of design engineers and engineering managers worldwide. The EDN franchise includes EDN, EDN Europe, EDN Asia, EDN China, and EDN Japan. EDN.com, the Internet home of EDN, delivers a three-dimensional view of the electronics industry via breaking news coverage, strategic business information, and in-depth technical engineering content. www.edn.com

Runtime Design Automation
Booth: 1117

Santa Clara, CA

www.rtda.com

Runtime Design Automation specializes in enterprise resource management. We offer a unified family of software products to monitor, manage, and optimize the utilization of software licenses and CPU resources used for design tasks. We have the ability to manage and visualize your workflows, regardless of how complex they may be. We can distribute your workload across your computing resources. We can also monitor and report on the utilization of your expensive software licenses, as well as help you to develop an optimized configuration containing the right mix of licenses and hardware for your current and upcoming needs.

Sagantec
Booth: 522

Santa Clara, CA

www.sagantec.com

For analog and custom IP designers, Sagantec enables the fastest migration path to advanced process technologies without compromising handcrafted quality and control. Sagantec solutions offer an order of magnitude productivity increase in implementation of custom IP in the 65nm, 45nm and 32nm process technologies.

Meet our customers and learn how they use Sagantec solutions to implement cutting-edge analog IP design acceleration in 40nm and 65nm technologies. Get on the fastest path to implement your custom IP in a new process technology.

Satin IP Technologies
Booth: 2124

Montpellier Cedex 2, France

www.satin-ip.com

Committed to design quality closure with fast ROI, Satin IP Technologies delivers software solutions for fact-based design quality monitoring. Working within customers' design flows, VIP Lane® turns customers' design practices for IP blocks or SoCs into a robust set of quality criteria and automates the implementation and documentation of design quality metrics at no extra cost in engineering time or resources. VIP Lane® shortens time-to-market by delivering effective flow integration and on-the-fly quality monitoring at zero overhead to design teams.

Seloco, Inc.
Booth: 1419

Seoul, Korea

www.seloco.com

Since 1990, MyCAD offers a Windows-based EDA toolset installed in thousands of copies around the world – America, Europe, Asia recently including China and India. The main product for industrial application is MyChip Station, a set of IC layout editing and verification tools. MyCAD tools' economical, handy and practical features have encouraged small to medium size designs of ICs, LEDs, Opto-devices, MEMs, and LCDs recently. MyChip Station is also used to convert AutoCAD data to photolithographic mask data generation. A new feature is its added cross section view capability for an IC/device layout. MyCAD's educational tool set includes VHDL simulator/synthesizer, schematic capture/logic simulator, SPICE simulator and an FPGA experimental kit. Try free at www.mycad.com

Semifore, Inc.
Booth: 812

Mountain View, CA

www.semifore.com

Semifore, Inc. provides the CSRCompiler, an advanced tool that bridges the gap between hardware, software, verification, and documentation. The designer can hierarchically specify the register address space of a design in a reusable manner to generate: Verilog and VHDL RTL; Verilog, or C headers; Perl, and Spirit IP-XACT; HTML web pages; and Adobe Framemaker or Microsoft Office documentation. The evolving specification is effortlessly and consistently available to all members of the product team to reduce cost and time to market.

Sequence Design, Inc.
Booth: 3455

Sunnyvale, CA

www.sequencedesign.com

Sequence Design – winner of a 2009 IEC DesignVision Award, featured in EDN's Hot 100 Products for 2008 and SiliconIndia's Top 5 EDA Companies – provides Design For Power (DFP™) solutions that accelerate the ability of SoC designers to bring high-performance, power-aware ICs to market. Sequence's power and signal-integrity software give customers the competitive advantage necessary to excel in aggressive technology markets. For more information, visit www.sequencedesign.com.

Si2
Booth: 1400

Austin, TX

www.si2.org

Si2 is an organization of industry-leading semiconductor, systems, EDA, and manufacturing companies focused on improving the way integrated circuits are designed and manufactured in order to speed time to market, reduce costs, and meet the challenges of sub-micron design. Si2 is uniquely positioned to enable collaboration through a strong implementation focus driven by its member companies. Si2 focuses on developing practical technology solutions to industry challenges. Si2 represents 90 companies involved in all parts of the silicon supply chain.

EDN

CONNECT WITH THE GLOBAL ENGINEERING COMMUNITY

www.EDN.com

Reed Business Information (RBI)

Exhibiting Company Descriptions

SIGDA/DAC University Booth
Booth: 1828

New York, NY

www.sigda.org

The SIGDA/DAC University Booth has been providing an opportunity for the university community to demonstrate EDA tools, design projects, and instructional materials at the Design Automation Conference since 1987. The University Booth also provides space for the presentation of EDA vendor literature and programs of interest to the university community. The University Booth provides booth space and poster areas for participating universities. The University Booth is sponsored by ACM/SIGDA, EDAC, and the Design Automation Conference, and our corporate sponsors.

http://www.sigda.org/programs/Ubooth/Ubooth2009/

Sigrity, Inc.
Booth: 708

Santa Clara, CA

www.sigrity.com

Sigrity provides advanced software analysis solutions to ensure power integrity and signal integrity in chips, packages and printed circuit boards; and physical design tools for single die and SiP implementations. Over 190 companies utilize Sigrity products as part of industry standard design flows. Sigrity solutions help companies overcome design challenges and get to market faster while avoiding costly respins and field failures. Sigrity products have won technology innovation awards and the company receives high marks for customer support.

Silicon Design Solutions
Booth: 1410

Milpitas, CA

www.silicondesignsolutions.com

SDS is an IP and Design Services Provider.

Headquartered in Milpitas California USA

Offering a wide range of Embedded Memories delivered as a Compiler or as a single Instance.

SRAM, ROM, MPRF, CAM & TLB products available on Leading Foundry processes from 250nm to 28nm.

Design Services include Custom Embedded Memory Compilers or Instances Optimized to meet Customer application, Complete Test Chip development, Bit Cell development and contracted augmentation of internal memory design teams.

Engagement/Business Models are flexible and varied.

Silicon Frontline Technology
Booth: 3165

Los Gatos, CA

www.siliconfrontline.com

Endorsed by leading foundries and IDMs, Silicon Frontline provides "Guaranteed Accurate" post-layout verification software. High performance, full-chip parasitic extraction and integration with standard flows ensure the shortest path to quality and reliability.

F3D (Fast 3-D extraction) applications include analog/AMS circuits – ADCs, MIM/MOM Caps, image sensors, RF, high speed and advanced nodes, 65, 40 and 32nm.

R3D (Resistive 3-D extraction) applications include discrete or embedded power devices, where efficiency and reliability and analysis of large metal interconnects are critical.

Silicon Image
Booth: 3243

Sunnyvale, CA

www.siliconimage.com

Silicon Image is a leading provider of semiconductor and intellectual property (IP) products for the secure distribution, presentation and storage of high-definition content. The company targets consumer and mobile electronics, storage and PC/display markets with High-Definition Multimedia Interface™ technology (HDMI™), Mobile High-Definition Link (MHL™), Camera Image Signal Processor, Serial ATA (SATA) and Digital Video Decoder (H.264, MPEG-2, VC-1) solutions. The company has shipped more than 200 million standards-based semiconductors and licenses its silicon-proven IP for system-on-chip (SoC) implementations.

SKILLCAD INC.
Booth: 3261

San Jose, CA

www.skillcad.com

SKILLCAD is dedicated to custom routing and productivity enhancement tools for IC layout design, providing optimized by construction solutions to achieve better layout quality and shorter time-to-market. SKILLCAD is seamlessly integrated with Cadence Virtuoso Layout Platform, supporting both IC5.x and IC6.x, so customers can gain extra productivity without changing their design environment. SKILLCAD introduces innovative methods for bus/path routing, matched routing, shield wiring, auto via filling, pin labeling, dummy pattern filling and slot hole cutting etc. Those methodologies can also be adopted by other layout platforms if there are sophisticated public API functions. Despite the down turn of economy, SKILLCAD has a growing list of customers including top IC design companies.

SmartPlay Technologies
Booth: 520

San Jose, CA

www.smartplayin.com

Taking Design Services to the next level - VLSI design & Embedded Software

SmartPlay Technologies is a fast growing technology services company focused on Semiconductors, Embedded Software, and Systems Design. With a team of 130+ and growing experienced professionals, we provide vertical and end to end services in Chip Design, Mobile/Consumer Software & System Design solutions. Our vision is to be a leading service provider of end to end solutions by creating innovative business models that provide value, quality and execution excellence to its customers.

Founded in May 2008, SmartPlay acquired a leading semiconductor design services company – TechForce, Inc. with offices in San Jose, CA and Bangalore, India, comprising of highly skilled professionals and engineers possessing significant industry experience. SmartPlay has an extremely flexible engagement model tailored to specific needs of the customer. We strive to understand individual customer's needs, evaluate options and propose innovative solutions.

SoftJin Technologies
Booth: 3547

Santa Clara, CA

www.softjin.com

SoftJin offers customized EDA solutions using EDA building blocks and custom software development services across the design flow. We also offer complex GUI development, OpenAccess, Design Flow and Validation Services. Our Hardware Design services include System/RTL level design, FPGA based Implementation and IP Development & Customization Services.

Products

SoftJin offers a suite of customizable EDA components such as STA, Synthesis and Routing Engines targeted at FPGAs. Post Layout EDA is a special focus area where SoftJin offers several Products for IC Layout / Mask Data Preparation and Verification.

Solido Design Automation Inc.
Booth: 3060

Saskatoon, SK, Canada

www.solidodesign.com

Solido Design Automation will be highlighting Variation Designer, the first scalable and extensible solution for eliminating design loss caused by process variation in analog/mixed-signal and custom integrated circuits. With Variation Designer, Solido will demonstrate: Statistical applications which utilize PVT corners and/or design specific True Corners to account for global, local and environmental variation, and the new, Well Proximity application that enables designers to proactively solve for well proximity effects at the circuit design stage, saving design time and reducing area.

Sonnet Software, Inc.
Booth: 3349

N. Syracuse, NY

www.sonnetsoftware.com

Sonnet Software is dedicated to the development of high-frequency electromagnetic analysis software. Sonnet's software is aimed at today's demanding design challenges involving predominantly 3-D planar circuits and antennas (including microstrip, stripline, coplanar waveguide, PCB (single and multiple layers) and RF packages incorporating any number of layers of metal traces embedded in stratified dielectric material. Sonnet introduces the Sonnet Suites Release 12, with up to 30x or faster analysis over the previous release.

Spatial
Booth: 3245

Broomfield, CO

www.spatial.com

With 1.75 million seats worldwide, Spatial provides the leading 3-D software component technology for engineering applications. For decades, Spatial has enabled customers to bring innovative applications to market in less time and at lower 3-D development costs.

If you are developing AEC, CAD, CAM, EDA, Metrology, Shipbuilding, or any 3-D software application: learn what our ACIS 3-D modeling software, CAD translation software, and HOOPS 3-D visualization software components and services can do for you.

Springer
Booth: 1000

New York, NY

www.springer.com

Springer is one of the world-leaders in Engineering book publishing, boasting a broad range of subject matter, and a history of working with the most prestigious scholars in the field. Additionally, Springer publishes an astute collection of Journals, with a track record of generating the latest sought after content. For additional information about all our engineering publications, please stop by our booth, or visit us at Springer.com.

SpringSoft, Inc.
Booth: 3367

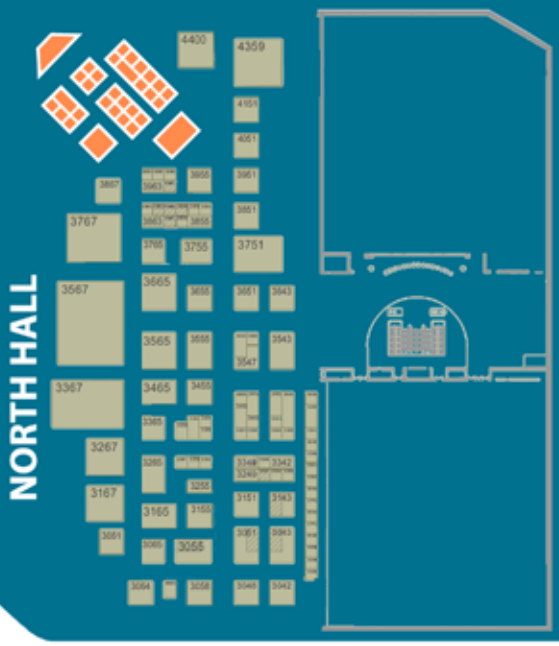
San Jose, CA

www.springsoft.com

SpringSoft specializes in unique automation technologies for design and verification. It's Novas® Verification Enhancement product line is comprised of the Verdi™ Automated Debug System that cuts debug time in half, the Siloti™ Visibility Automation System that speeds up simulation, and the Certitude™ Functional Qualification System that ensures verification quality. It's Laker® Custom IC Design product line delivers unsurpassed controllable automation to the layout process. Visit us at booth no. 3367 to learn more about out how SpringSoft is accelerating engineers.

ICDC

DESIGNAUTOMATIONCONFERENCE



PARTNER PAVILION

EDA and... IC:

- IP
- Design Services
- Foundry
- Test/BIST
- Interconnect
- TechPub Services
- Workload Management
- and More!

The ICDC Partner Pavilion is a combination of exhibit booths and 30-minute presentations by each participating vendor. The combination of product displays in the exhibits and technical product presentations in the ICDC Theater offers attendees an in-depth look into flows and methodologies from vendors featuring a variety of products and services for the entire design ecosystem.

Exhibiting Company Descriptions

StarNet Communications
Booth: 819
Sunnyvale, CA
www.starnet.com

At Booth 819, StarNet will introduce LinuxLIVE, which for the first time provides Linux workstations critical persistent connections to remote EDA tool servers and even allows for session sharing with Windows machines.

StarNet will also demo the latest X-Win32 release, the most powerful and advanced PC X server on the market. With features such as Suspend and Resume, SSH, OpenGL Support, Copy/Paste, Session Sharing and Low Cost, X-Win32 is the perfect connectivity solution for EDA engineers.

Summit Exec, Inc.
Booth: 3859
Eagle, ID
www.summitexec.com

Synapse Design Automation
Booth: 913
San Jose, CA
www.synapse-da.com

Synapse Design is an authorized & preferred Design Services Partner for over a dozen Tier 1 System & Semiconductor providers (including AMD, Broadcom, Microsoft, NEC-Japan, Qualcomm, ST Micro and TI). Our engagement model is flexible all the way to placing individuals or teams on site (internationally) on a contracted, hourly basis. We support our clients with front-end, back-end, verification and software engineering, in both the analog & digital realm

Synchronicity - see Dassault Systèmes
Booth: 716
Lowell, MA
www.3ds.com

See "Dassault Systemes"

Synfora, Inc.
Booth: 1440
Mountain View, CA
www.synfora.com

Synfora is the premier provider of algorithmic synthesis tools used to design complex SoCs and FPGAs. The PICO algorithmic synthesis platform offers designers of large, complex subsystems productivity gains by creating application accelerators from an untimed C algorithm. PICO products provide the best productivity using the highest level of abstraction; yield QoR competitive with manual design and enables high-level verification giving access to 100x speed-up. Synfora serves customers worldwide in the audio, video, imaging, wireless, and security segments. Productivity = Abstraction x QoR

Synopsys, Inc.
Booth: 1120
Mountain View, CA
www.synopsys.com

Synopsys, Inc. is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. Visit Synopsys online at http://www.synopsys.com/

Synopsys, Inc. - Standards Booth
Booth: 1016
Mountain View, CA
www.synopsys.com

Standards based interoperability and teamwork lead to greater productivity for successful design projects. Synopsys, a world leader in software and IP for semiconductor design and manufacturing, has been a strong proponent of creating and proliferating standards in design flow. This booth will highlight teamwork activities based on IEEE 1800 (SystemVerilog based verification methodology), IEEE 1801 (Unified Power Format – UPF), OSCI SystemC (System Level Design) and IPL (Interoperable PDK Libraries).

Synopsys-ARM-Common Platform Innovation
Booth: 1114, 1240
Mountain View, CA
www.synopsys.com

This booth is dedicated to the unique design enablement collaboration between the Common Platform (IBM, Chartered Semiconductor Manufacturing and Samsung Electronics), ARM and Synopsys. Leveraging our industry leadership, this collaboration is enabling a proven turnkey design solution for optimizing innovation and accelerating your design with best-in-class technology, physical and processor IP and tool/flow solutions for the Common Platform's 32nm/28nm high-k metal-gate (HKMG) process technology.

SynTest Technologies, Inc.
Booth: 3643
Sunnyvale, CA
www.syntest.com

Since 1990, SynTest has developed and commercialized many market-leading design-for-test (DFT) products, including Logic/Memory BIST (TurboBIST), Scan/ATPG (TurboScan), test compression (VirtualScan), and fault simulation (TurboFault). SynTest's DFT IP, e.g., at-speed scan/BIST, are silicon-proven and protected by a rich portfolio of 38+ patents. The TurboBIST-Logic product is used today by leading companies to reduce test-cost and improve quality. The newly released MULTICORE feature dramatically improves ATPG performance using multicpu systems. SynTest tools are backed by the most dedicated support team.

Tanner EDA
Booth: 3655, 1310
Monrovia, CA
www.tannereda.com

Tanner EDA provides Windows and Linux based electronic design automation software solutions for the design, layout and verification of analog and mixed-signal ICs and MEMS. Tanner EDA's HiPer Silicon is a complete IC design suite that encompasses schematic capture, circuit simulation, waveform probing, physical layout, foundry-compatible DRC, extraction, and verification.

Tanner EDA products enable faster time to market, lower costs, and shorter design cycles and are used to develop devices in the biomedical, consumer electronics, next-generation wireless, imaging, power management and RF markets.

Target Compiler Technologies NV
Booth: 3365
Leuven, Belgium
www.retarget.com

Target is the leading provider of software tools used to accelerate and optimize the design and programming of application-specific processor cores (ASIPs). ASIPs are used to build multicore SoCs for demanding embedded applications - including co-processors, accelerators and programmable datapaths.

Target's "IP Designer" tool-suite enables designers to create ASIPs with the right balance between performance, low power/cost, and flexibility. IP Designer has been applied by customers worldwide for diverse application domains, including GSM/WCDMA/HSDPA handsets, VoIP, audio/video/image codec/processing, automotive, ADSL/VDSL modems, wireless LAN, hearing instruments, and mobile/low-power applications.

TeamEDA
Booth: 910
N. Chelmsford, MA
www.teameda.com

TeamEDA, Inc. is a software technology company dedicated to effective management of EDA software licenses. License Asset Manager is a proven product and methodology for getting your arms around and controlling shared or standalone engineering licenses. Major EDA Vendors and Toolsare all preloaded. Expiration dates are monitored, and Alerts sent to allow adequate time to renew. License Inventory, Utilization, Denial, and Renewal Cost Reports are provided. License Asset Manager information and/or a brief demo, are available at TeamEDA, Booth 910.

Tech Source Media, Inc./SCDSource
Booth: 1624
San Jose, CA
www.scdsource.com

SCDsource™, a Tech Source Media, Inc. e-zine, provides in-depth technical news, news analysis and other vital industry information to help decision-makers up and down the electronics supply chain make better informed purchasing decisions. SCDsource editorial is written 'by engineers for engineers', making it a trusted and reliable news source. Unique to SCDsource is the first-of-its-kind SolutionSource™ Supplier Directory and DesignAware™ search engine that comprehends electronics industry terminology and taxonomy to enable quick and easy access to what engineering managers need and want.

Teklatech
Booth: 614
Copenhagen, Denmark
www.teklatech.com

A technology visionary and industry pioneer, Teklatech provides targeted EDA solutions to the semiconductor industry. With innovations in noise and power integrity, floorplanning and clock distribution networks, Teklatech's FloorDirector technology helps design teams to minimize dynamic IR drop and reduce power grid noise in digital ASICs. Teklatech works closely with industry leaders to ensure the compatibility of tools and design flows in order to serve customers with full solutions.

Tela Innovations
Booth: 710
Campbell, CA
www.tela-inc.com

Tela Innovations offers innovative, lithography optimized design solutions that lower power, reduce die area and improve performance of integrated circuits in advanced technologies. With the acquisition of Blaze, Tela adds additional capability to its line up aimed specifically at reducing leakage power. This technology will compliment Tela's solution of on-grid, straight line, one dimensional layout structures. These lithography-optimized structures enable manufacturing process optimization resulting in significant improvements in performance, power and area. For more information on the company visit www.tela-inc.com.

Innovation, Optimized!

EDA leader Synopsys and IP leader ARM are collaborating with the companies behind the Common Platform - IBM, Chartered and Samsung – to bring to market best-in-class process, design and IP innovation for 32nm/28nm high-k metal-gate (HKMG) technology in a more meaningful way.

Raising the bar, we are collectively engaging earlier to provide optimized innovation for truly differentiated customer solutions that reach the market more quickly.

Innovation becomes meaningful and relevant when it is put to work, solving problems, providing benefits and making a real difference.

Not all innovation is optimized. Make sure yours is.

Visit us in Booth #1114 to learn more about how optimized innovation can benefit you.

ARM®

common platform™
a collaboration of
IBM, Chartered & Samsung

SYNOPSYS®

Exhibiting Company Descriptions

The RTC Group
Booth: 3355

San Clemente, CA

www.rtcgroup.com

EDA Tech Forum journal is a quarterly publication for the Electronics Design Automation community including design engineers, engineering managers, industry executives, and academia. EDA Tech Forum journal provides an ongoing medium in which to discuss, debate, and communicate the electronic design automation industry's most pressing issues, challenges, methodologies, problem-solving techniques, and trends. The EDA Tech Forum journal is published by The RTC Group along with COTS Journal and RTC Magazine.

Tiempo
Booth: 4104

Montbonnot St Martin, France

www.tiempo-ic.com

TIEMPO develops and markets powerful Core IPs designed in an innovative clock-less and delay-insensitive technology. TIEMPO design technology represents the next breakthrough for ultra-low power and green semiconductor devices as it enables the design of chips that are ultra-low power, ultra-low noise, ultra-low voltage, very robust versus process-voltage-temperature variations and highly secured. TIEMPO IP portfolio includes various microcontroller and crypto-processor cores, and is supported by a design and synthesis flow using standard languages only. For more information, please visit www.tiempo-ic.com.

TOOL Corp.
Booth: 721

Tokyo, Japan

www.tool-corp.com

TOOL Corporation provides EDA tools and innovative solutions for chip designers and manufacturers. Showcased is LAVIS, a layout viewer not only capable of displaying VLSI design data quickly but also offering you rich functionality for your visual validation in timing closure, layout verification, lithography verification, and failure analysis. Stop by our booth and learn more about our software solutions that can dramatically optimize your design flow. For more information, visit www.tool-corp.com/.

True Circuits, Inc.
Booth: 1101, 3346

Los Altos, CA

www.truecircuits.com

True Circuits, Inc. (TCI) is the leading provider of timing IP for the semiconductor, systems and electronics industries. TCI develops robust state of the art circuits using a methodical and proven design strategy and in close association with the world's leading fabs, IDMs and design service providers. TCI offers a complete family of high quality, low-jitter and standardized PLLs and DLLs in a range of frequencies, multiplication factors, sizes and functions in TSMC, UMC, CHRT and Common Platform processes from 180nm to 40nm.

TSMC
Booth: 822

San Jose, CA

www.tsmc.com

TSMC is the world's largest dedicated semiconductor foundry, providing the industry's leading process technology and the foundry's largest portfolio of process-proven libraries, IP, design tools and reference flows. Total managed capacity exceeds 9 million 8-inch equivalent wafers from two 12-inch - GigaFabs™, seven eight-inch fabs and one six-inch fab. TSMC's Open Innovation Platform increases return on investment, improves time-to-market and reduces waste for customers and ecosystem partners. TSMC provides Platform infrastructure through enablement building blocks and ecosystem interfaces. Visit http://www.tsmc.com.

TSMC Open Innovation Forum, Cadence
Booth: 822

San Jose, CA

www.cadence.com

Cadence will demonstrate results of its long-standing colloboration with TSMC to enable predictable SoC design to meet today's time-to-volume requirements. In the TSMC Reference Flow 10.0, through unique capabilities such as SiP (System-in-Package), SNA (Substrate Noise Analysis) and integrated model-based DFM, you will see how advanced nanometer SoCs can be implemented successfully. We will also showcase a RF Reference Kit recently released by TSMC and Cadence – enabling a predictable AMS / RF design flow. We collaborate, so you can innovate!

TSMC Open Innovation Forum,Global UniChip
Booth: 822

www.globalunichip.com

GUC will show case the recent achievements in areas like ESL design environment, low power methodology, SSD (Solid State Disk) total solution and SiP design flow. Presentations, supporting literatures and live demo will be available during the exhibition.

TSMC Open Innovation Forum, Integrand
Booth: 822

Berkeley Heights, NJ

www.integrandsoftware.com

Integrand Software, Inc. provides tools to design high frequency, RF/Mixed Signal ICs for the semiconductor and electronics industries. Our advanced full-wave 3-D EM simulation tool, EMX, is fast, accurate and easy to use. It is 10-50 times faster and handles problems several times larger than other commercial EM tools. The world's top four foundries use EMX to develop scalable models for their design kits. Many major IC companies use EMX for designing inductors, transformers, MiM/MoM capacitors, VCOs, LNAs and filters.

TSMC Open Innovation Forum, Lorentz
Booth: 822

Milpitas, CA

www.lorentzsolution.com

Lorentz Solution is a growing EDA company to provide an unique electromagnetic (EM) simulation-based design and verification environment to enable analog RF IC designers to design, analyze and eliminate high frequency effects during circuit design. Its flagship product, PeakView, is adopted by top RF/wireless, analog and FPGA companies in the world. These companies chose PeakView because of its unique Layout EM (LEM), highly efficient PCircuit and flexible simulation model generation within the toolsuite. PeakView is proven and ready for tomorrow advanced processes in most major foundries.

TSMC Open Innovation Forum, Magma
Booth: 822

www.magma-da.com

Get on the Fastest Path to Silicon™ with Magma. For digital implementation, our 40-nm-proven Talus® system delivers the fastest turnaround on the largest most complex SoCs and includes advanced technologies for low-power design. The Quartz™ tools provide superior runtime and read files from third-party DRC/LVS tools. The Titan™ system accelerates analog design migration. FineSim™ enables fast, accurate simulation of the most challenging analog designs. And, only Magma integrates analog and digital implementation, circuit simulation, and verification – providing a quantum leap in designer productivity.

TSMC Open Innovation Forum, Mentor
Booth: 822

Wilsonville, OR

www.mentor.com

Mentor Graphics (R) is a world leader in EDA products, consulting services and award-winning support for electronics and semiconductor companies. Mentor offers a complete solution for IC physical implementation, signoff verification, manufacturing variability management, production testing, and diagnosis-driven yield analysis, including the Olympus-SoC (TM) place-and-route system, the Calibre (R) verification and DFM suite, and the TestKompress (TM) ATPG solution. Mentor products are fully qualified for TSMC's most advanced reference flows.

TSMC Open Innovation Forum, SpringSoft
Booth: 822

www.springsoft.com

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TSMC Open Innovation Forum, Synopsys
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Verific Design Automation
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Alameda, CA

www.verific.com

Verific Design Automation develops and sells C++ source code Verilog, SystemVerilog, and VHDL front-ends (parsers, analyzers, and elaborators) for EDA applications. With more than 50 licensees worldwide, Verific's software is being found in applications ranging from simulation, synthesis, emulation, design-for-test, virtual prototyping, logic equivalence checking, and model checking, to HDL entry. More than 20 exhibitors at DAC 2009 will demo products that incorporate Verific's technology. The 4 leading FPGA vendors all use Verific as their RTL front-end. When will YOU switch ?

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www.veritools.com

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ViASIC Inc.
Booth: 1522

Durham, NC

www.viasic.com

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Palo Alto, CA

www.warthman.com

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Booth: 3963

Roseville, MN

www.winterlogic.com

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Cambridge, United Kingdom

www.xjtag.com

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Booth 3440

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Enterpoint Ltd.
Booth 4207

www.enterpoint.co.uk

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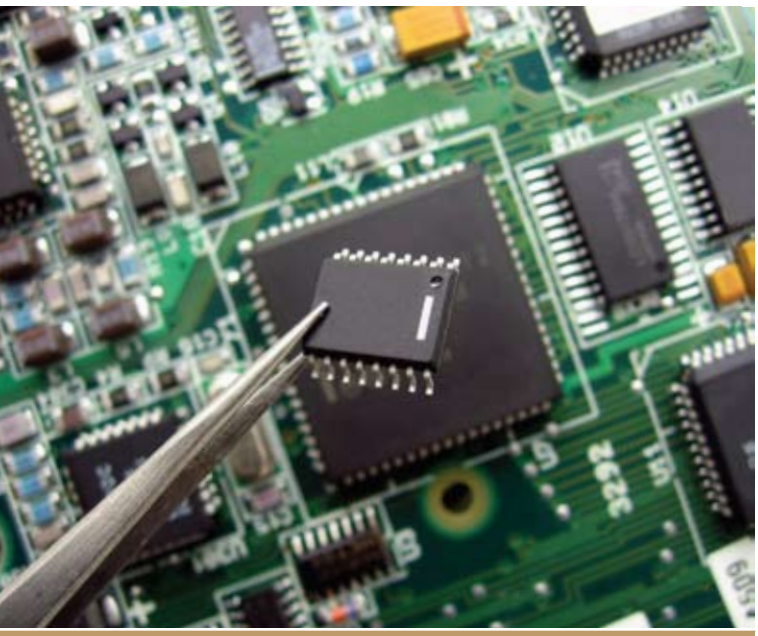

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n. *Informal*

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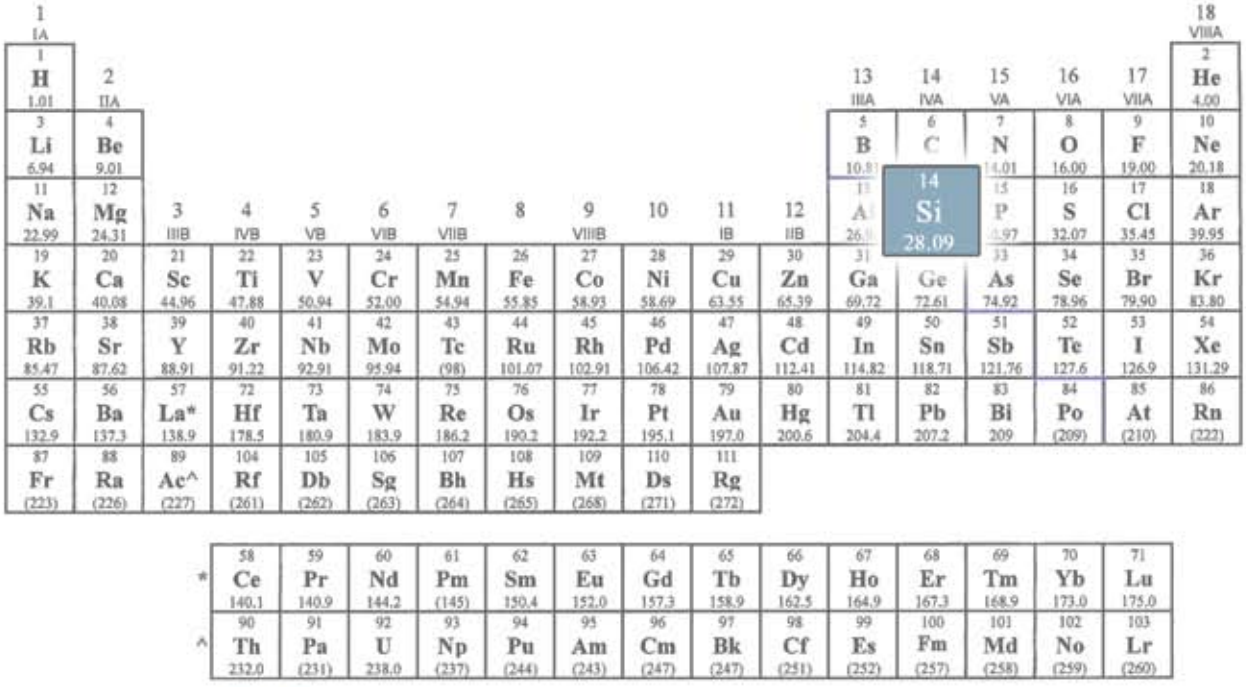

sil·i·con (sĭl'ĭ-kən, -kŏn')

n. Symbol Si

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19 Presentations...

See pages 22-23 for more details.

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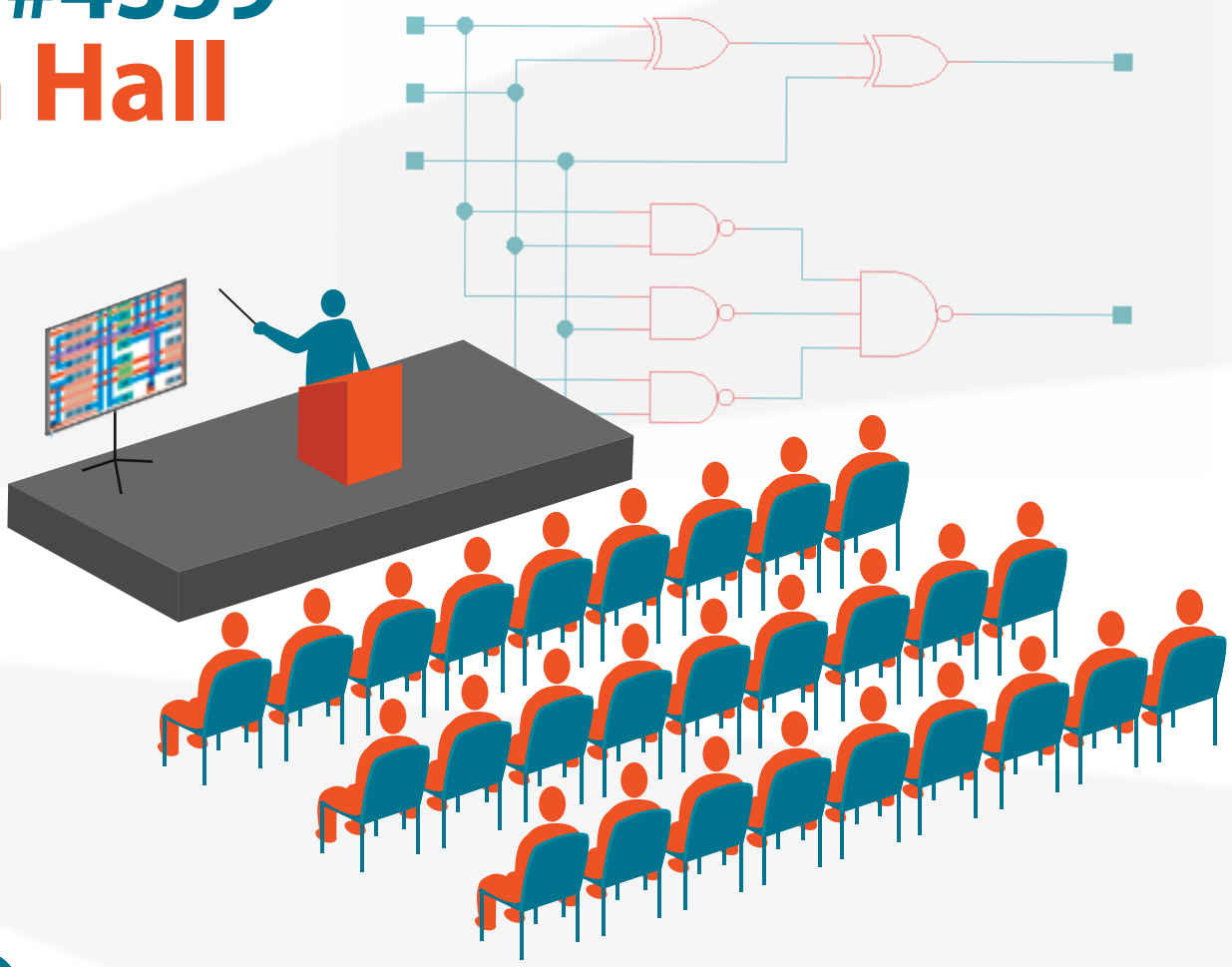
North Hall



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