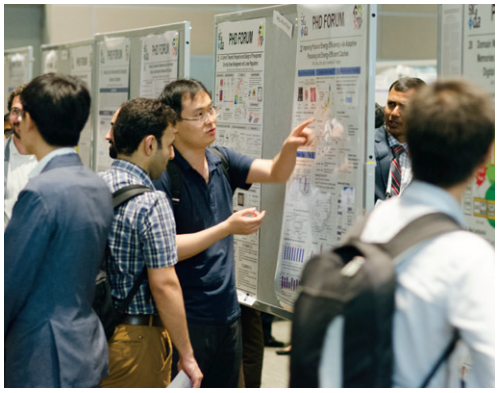
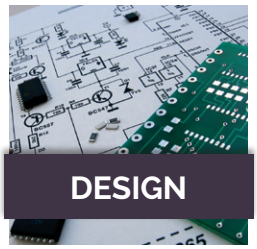


54 DESIGN AUTOMATION CONFERENCE

CONFERENCE PROGRAM & EXHIBITS GUIDE


DESIGN


EDA


ESS & AUTO

IoT


IP

SECURITY

JUNE 18-22, 2017 | AUSTIN, TX

SPONSORED BY: sigda, Electronic System Design Alliance, CEDA IEEE Council on Electronic Design Automation

IN TECHNICAL COOPERATION WITH: SSCS

#54DAC

GET THE DAC APP!

DOWNLOAD FOR FREE!

GET THE LATEST INFORMATION
RIGHT WHEN YOU NEED IT.
DAC.COM

- *Search the Technical Program*
- *Find Exhibitors*
- *Create Your Personalized Schedule*

DAC ATTACK

- *Play DAC Attack & Win Prizes!*

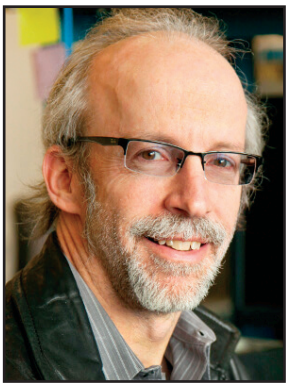
ANDROID APP ON Google play

Available on the App Store

*Visit **DAC.com** for more details and to download the **FREE** app!*

GENERAL CHAIR'S WELCOME

Welcome to the Home of the 54th Design Automation Conference: Austin, Texas!



What does the future hold for EDA and IP? How did a small startup company reinvent power supplies? Will machines understand human emotion? What's the opportunity for innovation in China?

These are just a few of the thought-provoking presentations you'll find in this year's 54th Design Automation Conference program, which I'm honored to share with you. Here are some additional highlights from throughout the week and I hope to see you around the conference:

Exhibits: We assembled hundreds of the finest vendors of design automation tools and IP, with the best products available to the market, some announced to the world for the first time this week! Our exhibitors are eager to meet with you, learn about your design and verification challenges, and discover how they can help you overcome these challenges with better methodologies using the tools you own; or how you can apply new tools to get even better results, more quickly, and with more predictable design cycles. Visit our exhibitors on the main floor of the Convention Center Monday through Wednesday from 10:00 am until 6:00 pm.

Conference: We selected the best 160 original research papers on new technical work in our area, and assembled these into a technical program together with a dozen special sessions on the most current topics in both the core of design automation, as well as in related areas including Security, Internet of Things, Automotive, Machine Learning, Intellectual Property, and Embedded Software and Systems. As a conference within the conference, attendees of the DAC Research Program enjoy a special access lounge on the top floor of the Convention Center, the Research Grove. You gain access to this very special program with the DAC Full Conference Pass.

Design: We've verified a Designer Track of 8 invited sessions, 2 panels and the best 48 papers where users of design automation technology share their experiences in using cutting edge tools to solve the most difficult problems; enabling you the audience to learn from their experiences and achieve better success in your practical design and verification experiences.

IP: We've assembled an IP Track with 3 invited sessions, 4 panels and the best 12 submitted papers on how to choose, deploy, monetize and reduce your design complexity and risk by employing IP in your next design. You gain access to the Design and IP Tracks with the Designer Special Pass.

Education: We've created an education program with 9 tutorials on Monday and 6 training sessions on Thursday to enable you to gain insight into topics that while mainstream, might not be areas where you personally have the expertise that you would like to have. Access these educational opportunities by purchasing the Monday Tutorial Pass and also sign up for the Thursday Training Sessions that attract your interest at the DAC website.

Keynotes: IoT is everywhere this year, and our 9:00 am Keynotes reflect this. **Joe Costello** opens the day on Monday, telling us about his IoT startup, "Enlighted," which is bringing automation to commercial and industrial buildings. **Chuck Grindstaff** begins our Tuesday sharing with us the many reasons why Siemens bought Mentor Graphics; I suspect one is to enable the joint company to be an even better design partner for your teams developing IoT products. **Tyson Tuttle** starts Wednesday off for us, sharing with us the unique challenges of providing Silicon IP for IoT, and how companies like his are meeting these challenges. Professor **Rosalind Picard** opens Thursday, sharing with us the surprising things she has learned in her research at the MIT Media Lab on teaching machines to understand human emotions.

SkyTalks: Just after lunch we present educational talks from those deeply involved in the business or technology of design. On Monday, listen to Professor **Shojun Wei** share with us the explosive growth of the Chinese IC industry, and some of the unique challenges and opportunities of this amazing expansion. On Tuesday, enjoy a friendly argument between long friends **Simon Segars** and **Lucio Lanza** as they debate how developing and deploying products for IoT will upset our market and change the world; and jot down their predictions of who will be the winners and losers in the market place. On Wednesday listen to **Dinesh Ramanathan** describe how his company has reinvented the power supply! Today's power conversion was developed in the 1980's and provides about 85% efficiency in converting AC to DC for our semiconductors – the rest is wasted as heat. His company's new technology, and new transistors convert power at greater than 95% efficiency – which is extremely interesting to anyone running huge data centers, electric motors for cars, or big solar arrays.

How are you going to navigate all of this? Well, you are holding the paper guide to find out what to do when! Read through this guide, mark each event, talk, panel, exhibit, session, and tutorial you want to see, and bring this with you every day, all week long. Or, if you are not that organized, **Download the DAC APP** from iTunes or Google Play, and mark the events and booths you want to see, and your phone will take you where you need to be, when you need to be there!

And, I expect to see each one of you at the networking events Sunday night, and each evening after the show, and at the evening venues up and down 6th Street!

Mac

Michael 'Mac' McNamara
General Chair, 54th DAC

TABLE OF CONTENTS

CONFERENCE SPONSORS

ACM/SIGDA

IEEE/COUNCIL ON ELECTRONIC DESIGN AUTOMATION

ELECTRONIC SYSTEM DESIGN ALLIANCE

DAC ATTACK GAMING RULES & ACHIEVEMENTS

Game Begins: 10:00am, Monday, June 19 | Game Ends: 4:00pm, Wednesday, June 21

HOW DO I GET POINTS?

1. Scan the QR Code at each participating exhibitor booth located on the DAC Exhibit Floor

There are different point categories for the exhibitors:

All Exhibitors	**50 points**
Reception Sponsor	**75 points**
Amiq: Booth 1639	
I Love DAC Sponsors	**100 points**
ClioSoft: Booth 613	
OneSpin: Booth 1547	
TrueChip: Booth 741	
Platinum Exhibitors	**125 points**
Cadence: Booth 107	
Synopsys: Booth 149	

Encounter the World of IoT: Booth 521

- Maker's Market
- Find Your IP at DAC
- Teardowns
- VR Experience: Enter Another Realm of Reality

DAC ATTACK

- Keep IoT Weird Tech Puzzle
- Find your IP @ DAC

All activities part of DAC ATTACK
Download the App and Play to Win

ANDROID APP ON Google play

Available on the App Store

2. Find a member of the DAC Executive Committee: **100 points**

Each member of the committee will be wearing a button with a QR code to scan.

3. Participate in DAC Activities: **50 points**

Participate in the activities listed below located throughout the show floor and scan the individual QR codes (each QR code can only be scanned once): Virtual Reality Experience in World of IoT Pavilion, Virtual Reality Experience in DAC Entertainment Lunch Corral, TechShop Puzzle Experience in World of IoT Pavilion, TechShop Puzzle Experience in DAC Entertainment Lunch Corral, and Roving DAC Magician.

4. Find the missing treasure hidden around the show each day: **150 points**

This gets you the most points! Each day of the exhibit (Monday, Tuesday and Wednesday) DAC will hide Elliott, the Engineering Superhero action figure. Elliott will have a QR code on him, scan the code and earn the point. Please return Elliott to his hidden area for the next person to find.

5. Attend the morning key notes: 20 points

Scan the QR code at the end of each morning's keynote.

PRIZES

*DAC Attack ends at **4:00pm on June 21st.** Raffle prizes and the grand prize winner will be announced on Wednesday, June 21, 2017, at 5:00pm at the DAC Pavilion and by broadcast message within the App.*

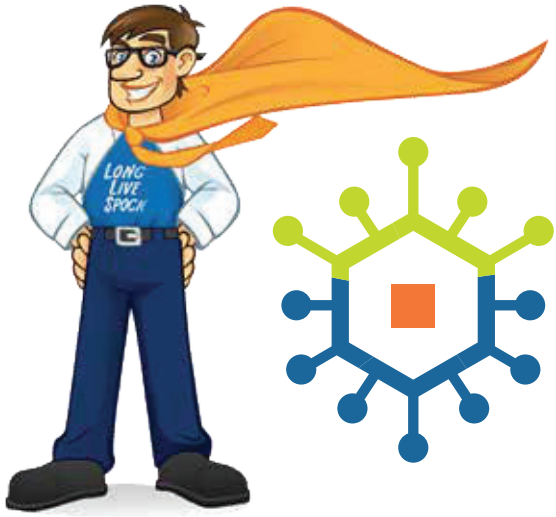
Registered attendees are eligible to win any of the prizes! There are two types of prizes: raffle prizes and the grand prize. Raffle winners will be selected from the top 50% of highest points scored. The Grand Prize will be randomly selected from the top 10% of the highest points scored.

Grand Prize:
Samsung Virtual Reality Headset

Raffle Prize:
Bose Wireless Headphones - $150 Gift Card to the Amazon Store - Google Home - Nest Cam Outdoor Security System

RULES AND HELPFUL INFORMATION

- Please play fair! We reserve the right to remove points that were obtained in a fraudulent manner.
- Look for the QR markers around the exhibit fl oor located at each booth. If you do not see a QR code, ask the exhibitor where they are placed. Each code you scan through the DAC Mobile App earns you a variety of points that go towards your total tally.
- Check the leaderboard in the app or the Social Media boards at the show to see how many points you have, and where you stand on the leaderboard. Please note that the leaderboard updates approximately every 5 minutes.
- Registered attendees are eligible to win any of the prizes! Exhibitors and exhibit staff are not eligible to win.
- As some prizes may be shipped to winning contestants, you do not need to be present to win.



DAC ATTACK

DAC ATTACK MOBILE APP GAME IS BACK!

Be Part of the Experience! Visit Exhibitors. Collect Points. Win Big.

DAC ATTACK Mobile App Game is Back - Be Part of the Experience! Visit Exhibitors. Participate in Activities. Collect Points. Win Big. Go big or go home the DAC Mobile App Game – DAC Attack is a mobile-enhanced persistent game that allows you to collect points throughout the DAC exhibit floor. Use your iOS or Android mobile devices to scan QR markers wherever you see them located in various exhibitors' booths and at activity centers.

Have fun and meet people as you make your way towards becoming one of this year's big winners!

Raffle prizes and the grand prize winner will be announced on Wednesday, June 21, 2017, at 5:00pm at the DAC Pavilion. As some prizes may be shipped to winning contestants, you do not need to be present to win.

Grand Prize: Samsung Gear Virtual Reality Headset

Raffle prizes: Bose Wireless Headphones
$150 Gift Card to the Amazon Store
Google Home
Bose Wireless Headphones
Nest Cam Outdoor Security System

ANDROID APP ON Google play

Available on the App Store

*Visit **DAC.com** for more details and to download the **FREE** app!*

CONFERENCE INFORMATION

EXHIBIT HOURS

LOCATION: EXHIBIT HALLS 1-4

Monday, June 19	10:00am - 6:00pm
Tuesday, June 20	10:00am - 6:00pm
Wednesday, June 21	10:00am - 6:00pm

REGISTRATION HOURS

LOCATION: AUSTIN CONVENTION CENTER ATRIUM

Friday, June 16 - Sunday, June 18	8:00am – 6:00pm
Monday, June 19 - Wednesday, June 21	7:00am – 7:00pm
Thursday, June 22	7:00am – 5:00pm

Thank You to Our Sponsor

Empyrean

ONLINE PROCEEDINGS

DAC Proceedings and tutorials will be delivered electronically online via a username and password.

To access: http://proceedings.dac.com
Username = Email address
Password = Registration ID (on your badge)

Please refer to your registration receipt to be reminded of what package and associated files you are eligible to view.

STAY CONNECTED

WIRELESS INTERNET

Austin Convention Center has complimentary wireless internet service throughout the facility.

"BIRDS-OF-A-FEATHER" MEETINGS

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal, non-commercial meetings, held after hours, are referred to as "Birds-of-a-Feather" (BOF). All BOF meetings are held at the Austin Convention Center, Tuesday, June 20 from 7:00 - 8:30pm.

To arrange a BOF meeting, please contact Corinne@dac.com. An LCD projector and screen will be provided.

FIRST AID ROOM

First Aid Room is located between Exhibit Halls 3 & 4 on the Trinity Street side of the building.

First Aid Room Hours:
Saturday, June 17 - Sunday, June 18: 8:00am to 6:00pm
Monday, June 19 - Thursday, June 22: 7:00am to 7:00pm

Non-emergency: 311

In-house security: 512-404-4111

DAC MOBLE APP

Download the DAC App!

Review the conference program, find exhibitors, and create a personalized schedule all from your phone or mobile device.

The DAC App is **FREE** for registered attendees! Check your email for your personalized invite or visit DAC.com for more information

ANDROID APP ON Google play

Available on the App Store

DAC NETWORKING OPPORTUNITIES

WELCOME RECEPTION

Sunday, June 18
5:30 - 7:00pm | 4th Floor Foyer

Join fellow attendees for the first event to network and kick-off DAC 2017!

DESIGNER/IP TRACK POSTER NETWORKING RECEPTION

Monday, June 19 - Wednesday, June 21
5:00 - 6:00pm each day | Exhibit Hall 1

Join us in Exhibit Hall 1 and while viewing the Designer and IP Track posters, take part in networking with light hors' d' oeuvres and beverages.

Thank You to Our Sponsors

Mentor® A Siemens Business

ChipEstimate.com

NETWORKING RECEPTION

Monday, June 19
6:00 - 7:00pm | Trinity St. Foyer

Join attendees for refreshments and lively discussion recapping the day's events.

Thank You to Our Sponsor

AMIQ

NETWORKING RECEPTION

Tuesday, June 20
6:00 - 7:00pm | Trinity St. Foyer

Join us in the Foyer to see Work-in-Progress posters and enjoy light hors' d'oeuvres and beverages.

Thank You to Our Sponsor

AMIQ

NETWORKING RECEPTION

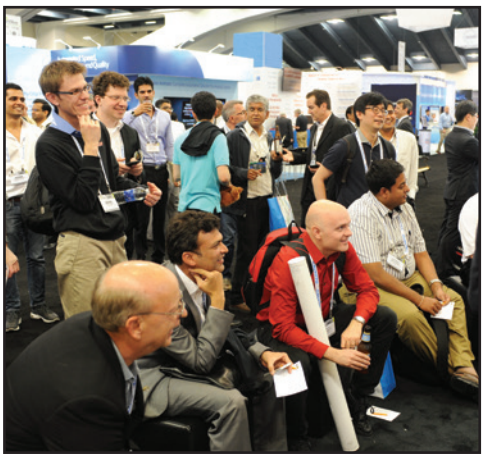
Wednesday, June 21
6:00 - 7:00pm | Trinity St. Foyer

Join us in the Foyer to see Work-in-Progress posters and enjoy light hors' d'oeuvres and beverages.

NETWORKING RECEPTION

Thursday, June 22
5:30 - 6:30pm | 4th Floor Foyer

Join attendees for refreshments and lively discussion recapping the day's events.



KEYNOTE PRESENTATIONS

KEYNOTE: IOT: TALES FROM THE FRONT LINE

JOE COSTELLO – *Enlighted, Inc., Sunnyvale, CA*

▶ ***Monday, June 19 || 9:15 – 10:00am || Ballroom A***

There is a lot of talk about the potential of the Internet of Things. But what is happening on the front lines? Where are the examples of real impact?

Enlighted CEO Joe Costello will discuss how the IoT is impacting commercial real estate, the largest asset class in the world, by giving buildings a "sensory system" akin to a human body. Once deployed, there are a multitude of new opportunities to improve business processes thanks to granular data that has never been available before.

Learn how this technology is currently being developed and applied, the challenges, along with predictions for the future of IoT in commercial buildings.

See page 17 for more details.

KEYNOTE: THE AGE OF DIGITAL TRANSFORMATION

CHUCK GRINDSTAFF – *Siemens PLM Software Inc., Plano, TX*

▶ ***Tuesday, June 20 || 9:00 – 10:00am || Ballroom A***

EDA has continually moved to higher levels of abstractions, changing how electronics are designed and created. Now we are seeing the need in the industrial world for further digitalization and virtualization. In his keynote, Chuck Grindstaff, Executive Chairman of Siemens PLM Software, will discuss the global impact of this digital transformation. EDA pioneered this revolution and paved the way for today's digital industrial revolution that is transforming and disrupting all industries. For system companies, their products are evolving into advanced system of systems. As a result, SoCs and application software are now the core differentiation and enabling technologies. This is spurring growth and opportunity for IC designers in the convergence of semiconductor and systems. Siemens and Mentor together are setting the vision for this new era of digital transformation.

See page 33 for more details.

KEYNOTE: ACCELERATING THE IOT

TYSON TUTTLE – *Silicon Labs, Austin, TX*

▶ ***Wednesday, June 21 || 9:00 – 10:00am || Ballroom A***

The Internet of Things (IoT) has been hailed as the next frontier of innovation in which the everyday "things" in our homes, offices, cars, factories and cities connect to the Internet in ways that improve our lives and transform industries. The IoT market is poised to reach 70 billion connected devices by 2025, but several challenges remain in achieving the market's full potential. Tyson Tuttle, CEO of Silicon Labs, will explore what it will take to accelerate the promise of the IoT. In his keynote, Tyson will consider the market imperatives and engineering challenges of adding connectivity to electronic devices, including cost, ease of use, energy efficiency, interoperability, future extensibility, and security. Addressing these challenges will unleash the limitless possibilities of a more connected world.

See page 51 for more details.

KEYNOTE: EMOTION TECHNOLOGY, WEARABLES, AND SURPRISES

ROSALIND PICARD – *Massachusetts Institute of Technology, Cambridge, MA*

▶ ***Thursday, June 22 || 9:10 – 10:00am || Ballroom A***

Years ago, I set out to create technology with emotional intelligence, demonstrating the ability to sense, recognize, and respond intelligently to human emotion. At MIT, we designed studies and developed signal processing and machine learning techniques to see what affective insights could be reliably obtained. In this talk I will highlight the most surprising findings during this adventure. These include new insights about the "true smile of happiness," discovering new ways cameras (and your smartphone, even in your handbag) can compute your bio-signals without using any new sensors, finding electrical signals on the wrist that reveal insight into deep brain activity, and learning surprising implications of wearable sensing for autism, anxiety, sleep, memory, epilepsy, and more. What is the grand challenge we aim to solve next?

See page 71 for more details.

SKY TALK: CHINA'S IC INDUSTRY: TODAY AND TOMORROW – ITS INFLUENCE ON GLOBAL DESIGN AND DESIGN AUTOMATION COMMUNITY

Shaojun Wei – *Professor, Tsinghua Univ., Beijing, China*

▶ ***Monday, June 19 || 1:00 – 1:25pm || DAC Pavilion – Booth 1737***

See page 19 for more details.

SKY TALK: EXPLORING THE CONNECTIONS BETWEEN THE DIGITAL WORLD AND THE PHYSICAL WORLD WITH SIMONS SEGARS AND LUCIO LANZA

▶ ***Tuesday, June 20 || 1:00 – 1:25pm || DAC Pavilion – Booth 1737***

Simon Segars – *Chief Executive Officer, ARM Ltd., Cambridge, United Kingdom*

Lucio Lanza – *Managing Director, Lanza TechVentures, Palo Alto, CA*

See page 38 for more details.

SKY TALK: POWER ELECTRONICS WITH VERTICAL GaN DEVICES

Dinesh Ramanathan – *Chief Executive Officer, NexGen Power Systems, Inc., Cupertino, CA*

▶ ***Wednesday, June 21 || 1:00 – 1:25pm || DAC Pavilion – Booth 1737***

See page 56 for more details.

IN MEMORY

Robert M. Gardner | 1943 - 2017

Mr. Gardner was member of the Board of Directors for Verific Design Automation since its inception in 1999. He co-founded Missing Link Electronics in 2008 and was its president and chief operating officer at the time of his death.

Mr. Gardner served as the executive director of the Electronic Design Automation (EDA) Consortium, now the Electronic System Design (ESD) Alliance, from 2007 until 2015. In 2016, he was presented with the DATE Fellow Award by the Design Automation and Test in Europe (DATE) Conference and Exhibit in recognition of his long association with EDAC and DATE.

Over a 50-year career, Mr. Gardner held senior management positions at semiconductor and EDA companies Signetics/Philips, AMD, Exemplar Logic, Design Acceleration, Bridges2Silicon, and ITeX. A 1965 graduate of California Polytechnic College in Pomona, he earned a Bachelor of Science degree in Electrical and Electronics Engineering. Mr. Gardner was active in instrumental music education and performances in Silicon Valley. He also was an avid sailor/yacht racer.

He is survived by his wife Monique; son Scott and his wife Sarah and children Zoe and Reese; daughter Lauree Walker and her husband Tim and their children Luke and Lily.

Carl Harris | 1941 - 2017

Mr. Harris spent over 40 years in educational publishing where he worked for Prentice Hall, W.A. Benjamin, Allyn & Bacon, Butterworth, Addison Wesley, Kluwer Academic Publishers, and Springer in a variety of positions from trade salesman to editorial director. Carl was particularly proud of his contribution to the field of Electrical Engineering through innovative publishing of advances in research and technology while at Kluwer Academic Publishers.

Ralph Otten | 1949 - 2016

Last September Ralph Otten passed away as a result of a tragic accident while on vacation in the Caucasian republic of Georgia. Ralph lived life to the fullest until literally the last moment: always curious, always informed and always with a quirky (but well-founded) opinion. With Ralph Otten the EDA community is losing a long time contributor, educator and friend.

Ralph Otten received his PhD from Eindhoven University in the Netherlands in 1976. At IBM TJ Watson Research Center he was on the team that designed the pioneering Yorktown Silicon Compiler, heralding the a new golden age for EDA. At DAC in 1982 Ralph published a key work on floor plan design that has influenced an entire generation of EDA researchers and set countless PhD students on a career in EDA. Later Ralph was full professor and educational director at Delft University of Technology, as well as Eindhoven University. In 2015 he retired and focused on his passions for Verdi, Italy and classical music.

Many of us will remember Ralph as a fixture at DAC, speaking, attending and reviewing for decades. He will be missed. Fortunately, Ralph's wife Carla will continue to assist DAC as before.

Mark Templeton | 1959 - 2016

Mark Templeton, the CEO and co-founder of Artisan Components, was a man who revolutionized the proliferation and distribution of semiconductor IP and he was able to achieve this while keeping an attitude of politeness and intellectual generosity.

Though he originated the idea for a company focused solely on component-level semiconductor IP and was the only CEO for the entire 14 year history of Artisan, Mark always introduced himself as the co-founder. He was modest about his success and profoundly grateful for the work of others: co-founders, employees, investors and partners, that he believed made the success possible.

After ARM acquired Artisan in 2004, Mark joined the board of ARM and was very proud to see Artisan become a significant and strategically crucial part of what was clearly going to be the leader of the expanding IP world.

"He was a great leader because he was always able to look far ahead at the distant horizon, while not taking his eyes off the path in front of him. He knew when it was time to stop and execute and took great care to get all the little things right," said Lucio Lanza, the first investor in Artisan Components.

Mark had an insatiable curiosity and never stopped learning. He loved to share new insights with his team at Artisan and his friends in the industry through the exciting years of Artisan. After Artisan and ARM, Mark continued to satisfy his intellectual curiosity by taking classes at Stanford and San Jose State, and teaching himself modern coding techniques.

Mark was always willing to help young entrepreneurs, new companies, and take meetings with people with only an idea. He never ceased learning from these meetings and never stopped sharing and teaching his insights to others. He was learning and teaching up until his very last days.

Mark was very successful because he was well balanced. He was usually right but never arrogant. Most importantly, he always found the appropriate balance between the demands of a start-up, and later a large growing company, and his family. Mark cherished the time he spent with his wife Betsy, and his two children, by whom he is now survived.

Charles "Chuck" Shaw | 1925 - 2017

Chuck Shaw, former SIGDA chairman, recently passed away. He died peacefully in his home on February 24, 2017, surrounded by three of his kids and a daughter-in-law.

Chuck was instrumental in moving SIGDA from a small group of engineers with an interest in EDA to a thriving professional society with numerous programs in place to advance the profession. To be sure, there were many contributors involved in implementing these programs but it was Chuck's leadership and enthusiasm that transformed the organization.

When Chuck was elected chairman of SIGDA in 1983 the SIGDA newsletter was our only publication and we provided seed money for 2 workshops. By the time his term ended in 1991, SIGDA was a sponsor, co-sponsor or working-in-conjunction-with 20 professional meetings. We also had programs in place to put EDA literature on CD-ROM, a University Booth at DAC, a benchmark program to compare DA algorithm performance, travel and library grants, video tape production of DA lectures and a new journal in the planning process.

Chuck achieved this remarkable transition by restructuring the board of directors. Quoting from his farewell "Letter from the Chair" in the June 1991 issue of the newsletter:

> I set as a prerequisite for Board membership that each person be the implementer of a major project. A person becomes a Board member by proposing or accepting a major project and selling it to the existing Board. He/she then joins the Board to carry it out. The other members of the Board serve as the reviewers, to whom each Board member reports the progress of his/her project(s). The whole Board sets policy. This has worked magnificently.

Magnificently, indeed! It attracted many hard working professionals with bright ideas onto our board and it remains the structure of the SIGDA Board of Directors to this day.

Chuck's enthusiasm and work ethic were contagious. He served 8 years as SIGDA Chairman and 11 years on DAC Executive committee (85-95) all while pursuing a very successful career at GE/Intersil and Cadence Design Systems. He will be sorely missed and long remembered by all of us in EDA.

Michael Lorenzetti

Former SIGDA Chairman

W1

WORKSHOP 1: SECOND INTERNATIONAL WORKSHOP ON DESIGN AUTOMATION FOR CYBER-PHYSICAL SYSTEMS (DACPS)

Time: 8:30am - 4:30pm || Room: 17AB || Event Type: Workshop
Track: EDA, Design || Topic Area: General Interest, Codesign & System Design

ORGANIZERS:

Xin Li - *Carnegie Mellon Univ., Pittsburgh, PA*
Mohammad Al Faruque - *Univ. of California, Irvine, CA*
Shiyan Hu - *Michigan Technological Univ., Houghton, MI*
Yier Jin - *Univ. of Central Florida, Orlando, FL*
Rajiv Ranjan - *Newcastle Univ., Callaghan, Australia*
Bei Yu - *Chinese Univ. of Hong Kong, Shatin, Hong Kong*
Huafeng Yu - *Boeing, Huntsville, AL*
Qi Zhu - *Univ. of California, Riverside, CA*

Cyber-Physical Systems (CPS) are characterized by the strong interactions among cyber components and dynamic physical components. CPS system examples include automotive and transportation systems, smart home, buildig and community, smart battery and energy systems, surveillance systems, cyber-physical biochip, and wearable devices.

Due to the deeply complex intertwining among different components, CPS designs pose fundamental challenges in multiple aspects such as performance, energy, security, reliability, fault tolerance and flexibility. Innovative design automation techniques, algorithms and tools that addressing the unique CPS challenges, such as the fast increase of system scale and complexity, the close interactions with dynamic physical environment and human activities, the significant uncertainties in sensor readings, the employment of distributed architectural platforms, and the tight real-time constraints, are highly desirable.

This workshop will present the state-of-the-art research results on the topic of design automation for CPS, and stimulate the CAD researchers to participate in the interdisciplinary CPS research area in the future.

SPEAKERS:

Jiang Hu - *Texas A&M Univ., College Station, TX*
Tei-Wei Kuo - *National Taiwan Univ., Taipei, Taiwan*
Ramesh S - *General Motors Research and Development, Warren, MI*
Ulf Schlichtmann - *Technische Univ. München, Germany*
Rahul Mangharam - *Univ. of Pennsylvania, Philadelphia, PA*
Mohammad Al Faruque - *Univ. of California, Irvine, CA*
Yier Jin - *Univ. of Central Florida, Orlando, FL*

W2

WORKSHOP 2: DAC WORKSHOP ON AUTONOMOUS VEHICLES, AVIONICS, TRANSPORTATION, AND ROBOTICS (AVATAR)

Time: 9:00am - 5:00pm || 12AB || Track: Automotive, Design
Topic Area: General Interest, Codesign & System Design, Emerging Architectures & Technologes || Event Type: Workshop

ORGANIZERS:

Rasit Topaloglu - *IBM Corp., Hopewell Junction, NY*
Peng Li - *Texas A&M Univ., College Station, TX*
Huafeng Yu - *Boeing, Huntsville, AL*

There have been significant development efforts in autonomous systems in the last decade. We have already started to see successful realization of products that utilize autonomous design and algorithms. Particular achievements have come in vehicle, avionic, and robotic applications. There are still research and development challenges in these systems though and some of these challenges do intersect with the interest of the design automation community. Thus, we would like to hold a workshop to facilitate interaction between autonomous system and design automation communities.

The EDA community has a long history developing a full spectrum of modeling, optimization, design verification and test algorithms and tools for electronic systems. We expect that the strong expertise accumulated in EDA over the past few decades may be well extended for the targeted application areas of this workshop, which, if successful, will stimulate new advancements in autonomous systems and broaden the impacts of EDA research in general.

To realize these goals, we plan to have a full-day workshop with invited talks and panel sessions. We target holding three sessions and invite the following list of speakers. We anticipate being able to understand the challenges they face and discuss if some of the problems can be solved using the skills and experience of the design automation community.

SPEAKERS:

Rahul Mangharam - *Univ. of Pennsylvania, Philadelphia, PA*
Kara Kockelman - *Univ. of Texas at Austin, TX*
Nicholas Gans - *Univ. of Texas at Dallas, Richardson, TX*
Ignacio Alvarez - *Intel Corp., Portland, OR*
Ivan Lozano - *Airspace Systems Inc., San Francisco, CA*
Gaurav Bansal - *Toyota InfoTechnology Center, Mountain View, CA*
Alireza Talebpour - *Texas A&M Univ., College Station, TX*

W3

WORKSHOP 3: CUSTOMIZING PDKS FOR DESIGN-SPECIFIC REQUIREMENTS

Time: 9:00am - 12:00pm || 19AB || Track: Design, EDA
Topic Area: Analog & Mixed-Signal Design, Physical Design & DFM
Event Type: Workshop

ORGANIZER:

Ted Paone - *Silicon Integration Initiative, Inc., Austin, TX*

Good stories often start over a beer. While sharing a libation or n + 1 with several friends from the industry, one of them mentioned a problem with their fab supplied PDK. Another had a similar problem with a different PDK, by the end next round, I had collected a list of common problems that design groups were having with their PDKs.

A process design kit (PDK) models a specific fabrication process for a set of tools used in the design flow blessed by the fab. Using this PDK and following one of the fab supported design flows, the designers can create and verify a design that is manufacturable in that process.

The PDKs available from the fabs not only reflect the specific manufacturing process but can be tailored for markets with the addition of processing steps and devices. This generic PDK works very well for many of the design groups. You can create a design and it can be manufactured.

With the competition in some markets, the design groups must take any advantage it can over its competitors. They choose the tools and methodologies specific to their design market and design style, these may deviate from the supported flows. These groups want to enhance the PDK to meet their needs. It isn't just a drinking problem; these issues are industry wide. An industry wide problem can be solved with a collaboratively developed solution.

In this tutorial, we will explore ways of customizing PDKs to support the tools and devices in your design flow without rewriting the existing PDKs. We will jump in with parameters, resetting defaults and other control and adding new parameters. On to PCells, customize the shapes, connectivity and properties without source code. Add new tools to the flow, integrating the technology and supporting new parameters and models. Integrate your own devices into the PDK and not have them overwritten on an uprev from the fab.

These solutions addressed many of the problems seen by the PDK Users. They represent what can be done by working collaboratively to solve common problems yet allowing each user to customize the implementation.

Working together to address common issues, under the anti-trust protections provided by Si2 membership, SIG members create ideas, write white papers, conduct surveys, and develop prototypes; unique solutions sharing a common understanding of the problems.

SPEAKER:

Ted Paone - *Silicon Integration Initiative, Inc., Austin, TX*

W4

WORKSHOP 4: LEADERSHIP IMPROV

Time: 1:00 - 5:00pm || 19AB || Track: Design, EDA || Topic Area: General Interest
Event Type: Workshop

The purpose of this workshop is to enhance your capacity to lead technology organizations effectively.

Why are some leaders better and more successful than others? One reason involves their ability to communicate with others in the moment, to be mindful and respond to what is happening right now. We borrow techniques from improv to help you learn to better communicate with others.

Improv requires skill, preparation and practice to be able to listen, act and react in the moment. This improv workshop prepares both individual contributors and leaders how to react, adapt and communicate honestly with others.

We use real world examples and cases to make this workshop immediately applicable to your workplace.

You will learn how to listen, ask questions to learn more about your boss or subordinate's goals, objectives and interests, and to respond in ways that improve understanding and cooperation.

The word "improv" brings to mind improv comedy and laughter. While this class is serious business, the workshop is engaging and entertaining while you learn.

In this highly participative class, we use case studies and real-world scenarios from the tech industry, which provide you the opportunity to learn new techniques and put them to immediate use.

SPEAKER:

Leslie Martinich - *IEEE, Austin, TX*

See More Great Content in the DAC Pavilion! Complete schedule can be found on Pages 97 - 101, Additional Meetings: See Pages 89 - 95.

OPENING SESSION & AWARDS PRESENTATION

Time: 8:45 – 9:15am || Room: Ballroom A || Topic Area: General Interest

Join us as we set the stage for the 54th DAC! DAC's Executive Committee will highlight the conference's events, and the award presentations will recognize success and excellence for individuals in the industry.

2016 PHIL KAUFMAN AWARD FOR DISTINGUISHED CONTRIBUTIONS TO EDA

Dr. Andrzej Strojwas, Keithley Professor of Electrical & Computer Engineering, Carnegie Mellon University, Pittsburgh, PA

Dr. Strojwas is being recognized for his pioneering and sustained contributions to design for manufacturing.

IEEE CEDA OUTSTANDING SERVICE AWARD

Charles Alpert, Cadence Design Systems, Inc.

For outstanding service to the EDA community as DAC General Chair in 2016.

IEEE FELLOW

Luca Carloni, Columbia University

For contributions to system-on-chip design automation and latency-insensitive design.

IEEE FELLOW

Xin Li, Duke University / Duke Kunshan University

For contributions to modeling, analysis, and optimization of variability of integrated circuits and systems.

IEEE FELLOW

Frank Liu, IBM Research

For contributions to design for manufacturability of VLSI circuits.

IEEE FELLOW

Walden C. Rhines, Mentor, A Siemens Business

For leadership and technology innovation in integrated circuit design and automation.

IEEE FELLOW

Weiping Shi, Texas A&M University

For contributions to modeling and design of VLSI interconnects.

IEEE CEDA DISTINGUISHED SERVICE AWARD

William H. Joyner, Jr., Semiconductor Research Corporation, Retired

For going above and beyond the call of duty in support of CEDA's activities.

IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS DONALD O. PEDERSON BEST PAPER AWARD

Xiaoqing Jin, Alexandre Donzé, Jyotirmoy V. Deshmukh, and Sanjit A. Seshia

"Mining Requirements from Closed-Loop Control Models," Vol. 34, Issue 11, pp. 1704 - 1717, November 2015.

A. RICHARD NEWTON TECHNICAL IMPACT AWARD IN ELECTRONIC DESIGN AUTOMATION

Matthew W. Moskewicz, Univ. California, Berkeley/ Cadence; Conor F. Madigan, Kateeva, Inc.; Ying Zhao, Wuxi Venture Capital Group; Lintao Zhang, Microsoft Research Asia; Sharad Malik, Princeton Univ.

Sponsored by the IEEE Council on EDA and the ACM Special Interest Group on Design Automation. For seminal contributions to scalable Boolean satisfiability solving including locality-based search and efficient backtracking.

Matthew W. Moskewicz, Conor F. Madigan, Ying Zhao, Lintao Zhang, and Sharad Malik "Chaff: Engineering an Efficient SAT Solver," Proc. of the 38th annual Design Automation Conference, pp. 530 - 535, June 2001.

2017 ACM TODAES BEST PAPER AWARD

Farshad Firouzi, Fangming Ye, Krishnendu Chakrabarty, Mehdi B. Tahoori

"Aging- and Variation-Aware Delay Monitoring Using Representative Critical Path Selection" ACM Design Automation of Electronic Systems, Vol. 21, Issue 1, Nov. 2015.

ACM SIGDA OUTSTANDING NEW FACULTY AWARD

Yier Jin, University of Central Florida

ACM SIGDA OUTSTANDING PH.D. DISSERTATION AWARD

Jeyavijayan Rajendran – "Trustworthy Integrated Circuit Design," New York University

Advisor: Ramesh Karri

ACM FELLOW

Sachin Sapatnekar

For contributions to the enhancement of performance and reliability in integrated circuits.

ACM FELLOW

Rajesh Gupta

For contributions in design of embedded systems and hardware-software codesign.

2017 MARIE R. PISTILLI WOMEN IN ENGINEERING ACHIEVEMENT AWARD

Janet Olson, Vice President of Engineering for RTL Synthesis R&D at Synopsys, Inc

This annual award, named for Marie R. Pistilli, the former organizer of DAC, recognizes individuals who have visibly helped advance women in Electronic Design.

P.O. PISTILLI UNDERGRADUATE SCHOLARSHIP FOR ADVANCEMENT IN COMPUTER SCIENCE AND ELECTRICAL ENGINEERING

Kenia Hale, Yale University

The objective of the P.O. Pistilli Undergraduate Scholarship for Advancement in Computer Science and Electrical Engineering is to increase the pool of professionals in Electrical and Computer Engineering and Computer Science from under-represented groups (female, African-American, Hispanic, Native American, and disabled students). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. DAC funds a $4000 scholarship, renewable up to five years, to graduating high school seniors who have a 3.00 GPA or better (on a 4.00 scale).

UNDER-40 INNOVATORS AWARD

The Under-40 Innovators Award is new this year and is sponsored by Association for Computing Machinery (ACM), the Electronic Systems Design Alliance (ESDA), and the Institute of Electrical and Electronics Engineers (IEEE). The award will recognize the top five young innovators (nominees should be 40 years or younger in age as of June 1, 2017) who are movers and shakers in the field of design and automation of electronics.

KEYNOTE: IOT: TALES FROM THE FRONT LINE

JOE COSTELLO - *Enlighted, Inc., Sunnyvale, CA*

Time: 9:15 - 10:00am || Room: Ballroom A
Track: IoT || Emerging Architectures & Technologies, Embedded System Software, General Interest

There is a lot of talk about the potential of the Internet of Things. But what is happening on the front lines? Where are the examples of real impact?

Enlighted CEO Joe Costello will discuss how the IoT is impacting commercial real estate, the largest asset class in the world, by giving buildings a "sensory system" akin to a human body. Once deployed, there are a multitude of new opportunities to improve business processes thanks to granular data that has never been available before.

Learn how this technology is currently being developed and applied, the challenges, along with predictions for the future of IoT in commercial buildings.

Biography: Joe Costello has been a high tech executive and CEO for the last 28 years. He became the CEO of Cadence Design Systems in 1987 and worked with the company from its inception until it became the largest electronic design automation (EDA) company in the world, with over a billion dollars in annual revenue.

Since the early 90s, Joe has been the mastermind behind numerous start-ups based around the idea of the Internet of Things, even before the phrase was even coined. Specifically, Joe started an incubator in 2000 and worked on IoT from late 2000 – 2004. That incubator included Orb Networks, which pursued IoT for entertainment-oriented applications and led to the creation of a platform for media distribution, management and control called AllPlay. Qualcomm acquired Orb Networks in 2013 and Joe joined its Qualcomm IoT platform group to help spearhead the creation and promotion of AllJoyn.

Costello was named the top CEO of America in 1997 by Chief Executive Magazine. In recognition of his service to the EDA industry, he was awarded the Phil Kaufman award in 2004, the highest accolade in the EDA industry. Costello has also served as a board member of dozens of companies including Oracle, Macromedia, Clarify and Mercury Interactive as well as numerous private companies.

ABOUT ENLIGHTED

Designed to change everything, Enlighted provides the world's most advanced digital sensor and analytics platform for smarter buildings to Fortune 500 companies around the globe. The company is headquartered in Sunnyvale, CA.

1

DESIGNER TRACK: VERIFICATION AUSTIN STYLE!

Time: 10:30am - 12:00pm || Room: Ballroom E || Event Type: Invited Presentations Track: Design, IP || Topic Area: Test & Verification, Simulation & Timing Analysis, General Interest

CHAIR:

Hemendra Talesara - *Synapse Design, Austin, TX*

ORGANIZER:

Harry Foster - *Mentor, A Siemens Business, Plano, TX*
Hemendra Talesara - *Synapse Design, Austin, TX*

Austin has quickly become one of the leading centers of verification expertise within the US and the world. This session invites three internationally recognizable names in verification (all from Austin) and showcases what makes Austin so unique. Each invited speaker will not only describe the challenges and unique solutions they have implemented—but their general philosophy in building a world class verification team.

1.1 Live Oak: Deep Roots of Verification & Design for Verification in Austin (10:30)
Wolfgang Roesner - *IBM Systems and Technology Group, Austin, TX*

1.2 Is it Hardware or Software? It's Both! (11:00)
Bill Greene - *ARM, Inc., Austin, TX*

1.3 Verification Challenges Associated with Automotive Microprocessors and Controllers (11:30)
Xiao (Sean) Sun - *NXP Semiconductors, Austin, TX*

2

DESIGNER TRACK: PHYSICAL DESIGN - NUGGETS FROM THE TRENCHES

Time: 10:30am - 12:00pm || Room: Ballroom F || Event Type: Reviewed Presentations || Track: Design, EDA || Topic Area: Physical Design & DFM, Digital Design

CHAIR:

Gary Ellis - *Encore Semi Inc., Norman, OK*

This session will highlight advanced techniques intended to expedite various areas of the physical design process. From the construction of very large designs using approaches like re-use and divide and conquer, to innovative tools for quicker ECOs and DRC sign-off, this session will help you to improve your design process.

2.1 Enabling Reuse of Logic Blocks Integrated Specialty Intellectual Property (IP) Blocks (10:30)
Sudeep Mandal, **Mukesh Bagul** - *GLOBALFOUNDRIES, Bengaluru, India*
Rashmi Chatty - *GLOBALFOUNDRIES, Austin, TX*
Liang Ge - *GLOBALFOUNDRIES, Shanghai, China*
Karl Vinson - *GLOBALFOUNDRIES, Essex Junction, VT*

2.2 Divide and Conquer Methodology for Ultra-Fast Layout Convergence (10:45)
Satya Seshadri, **Sarath Kumar B**, Sharath G, Murali Sundaram - *Intel Technology India Pvt. Ltd, Bangalore, India*

2.3 Power Efficient Distribution of Pervasive Multi-Cycle Signals (11:00)
William R. Migatz - *IBM Corp., Poughkeepsie, NY*
Shyam Ramji - *IBM Corp., Yorktown Heights, NY*

2.4 Optimized Automation of Design Rule Violations (DRC) Fix (11:15)
Sudeep Mandal, **Mirunalini Gunasekaran** - *GLOBALFOUNDRIES, Bengaluru, India*

2.5 Innovative Metal-Only ECO Methodology to Implement Large/ Complex Functional ECOs (11:30)
Biswajit Maity, Rajasekhara Badana, Arun Kandula, Abhishek Banthia, Viren R. Gajjar, Roshan Bondse - *Intel Technology India Pvt. Ltd, Bangalore, India*

2.6 Colorless Metal Routing for Triple and Quadruple Patterning Technologies (11:45)
Hyosig Won, **Myungsoo Jang** - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Hyounsoo Park - *Samsung Electronics Co., Ltd., Yongin, Republic of Korea*
Dayeon Cho, Taehoon Kim - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

▶ **Q &A Poster Session**
Monday, June 19 5:00 - 6:00 - Exhibit Floor

3

IP TRACK: SECURITY IP FOR IOT FROM SENSORS TO CLOUD

Time: 10:30am - 12:00pm || Room: Ballroom G || Event Type: Invited Presentations
Track: IP, Security || Topic Area: General Interest

CHAIR:
Claude Moughanni - *Lattice Semiconductor Corp., San Jose, CA*

The world of IOT promises the conveniences of remotely accessing our personal information and controlling the devices that permeate our private and working lives 24 hours a day. Being always connected means we are always vulnerable to security breaches. This session deals with evolving approaches in HW and SW security IP from sensors to the cloud, touching on securing access to devices, interfaces between them and corresponding data content.

3.1 Authenticate Everything (10:30)
Pim Tuyls - *Intrinsic ID, Sunnyvale, CA*

3.2 Challenges of the Emerging IoT Security Arena (11:00)
Jacques Fournier, Alain Merle - *CEA-LETI, Grenoble, France*

3.3 Security Assurance Guidance for Third Party IP (11:30)
Brent Sherman - *Intel Corp., Hillsboro, OR*

Thank You to Our Sponsor

ChipEstimate.com

SKY TALK: CHINA'S IC INDUSTRY: TODAY AND TOMORROW - ITS INFLUENCE ON GLOBAL DESIGN AND DESIGN AUTOMATION COMMUNITY

Time: 1:00 - 1:25pm || Room: DAC Pavilion - Booth 1737 || Event Type: SKY Talk
Track: Design, EDA || Topic Area: General Interest

ORGANIZER:
Sharon Hu - *Univ. of Notre Dame, IN*

When China announced its national plan to promote its native IC industry, this raised many questions. With its rapid growth, China's IC industry is becoming an emerging force globally, increasing the importance of understanding the answers to these questions. Few people really understand China's IC industry. For example, what is the real state of the China's IC industry today, what implications does such a promotion have to the global IC, EDA and other related industries, and what goals are China's IC industry working to achieve?

This presentation will give an overview of the Chinese IC market, followed by an introduction of China's IC industry with an emphasis on fabless companies. China's native products, design technologies, and talents will be described in detail to provide an objective and comprehensive picture of China's IC industry. In addition, China's current status in design automation technology and indigenous EDA companies will be discussed.

As China is a unique country with huge population, vast territory, rapidly growing but unbalanced economy, and many diverse cultures, life-styles and traditions, its native product demands are also diverse. How to meet these drastically different requirements with a reasonable time to market while keeping costs low presents a big challenge. A rapidly growing IC industry in China will force design and EDA engineers, both inside and outside China, to explore, to innovate as well as to collaborate. With a large talent pool addressing unique challenges, who can say there will not be new technologies, methodologies and products emerging to change the rules of the global information technology landscape?

Biography: Prof. Shaojun Wei is the Dean of the Department of Microelectronics and Nanoelectronics, Tsinghua University, Member of National IC Industry Development Advisory Committee, Vice President of China Semiconductor Industry Association (CSIA), Fellow of Chinese Institute of Electronics (CIE).

Prof. Wei received Master degree in Engineering from Tsinghua University in 1984 and Doctor Degree in Applied Science in 1991 from the Faculté Polytechnique de Mons (FPMs), Belgium and then became the assistant professor in FPMs. He returned to China in 1995. His research interest includes high-level synthesis, embedded systems design and reconfigurable computing technology. He has published nearly 190 papers, one monograph and participated in the writing of three monographs.

Prof. Wei worked for Datang Telecom Technology Co., Ltd. successively as Vice-President, President & CEO from 1998 to 2005 and CTO of Datang Telecom Industry Group from 2005 to 2006.

Prof. Wei had won many awards including China National Technical Invention Second Prize, China National Science and Technology Progress Second Prize, China Patent Golden Award (SIPO and WIPO), Technical Invention First Prize (Ministry of Education, China), Electronic Information Science and Technology First Prize (CIE), Outstanding Youth Award (CAST), Science and Technology Progress First Prize (Beijing Municipal), etc

SPEAKERS:

Shaojun Wei - *Tsinghua Univ., Beijing, China*

4

DESIGNER TRACK: EMBEDDED SYSTEMS AND SOFTWARE SOLUTIONS

Time: 1:30 - 3:00pm || Room: Ballroom E || Event Type: Reviewed Presentations
Track: Embedded Systems, Design || Topic Area: Embedded System Software, SoC & Embedded System Architectures, Emerging Architectures & Technologies

CHAIR:
Andrew Putnam - *Microsoft Corporation, Seattle, WA*

CO-CHAIR:
Michael Brogioli - *Network Native, Austin, TX*

This ESS session explores topics in heterogeneous computing, virtualization, FPGA design and Neural Networks. These topics are presented as they pertain to the design and implementation of modern embedded computing systems and software solutions.

4.1 Behavior Sampling Based Fast Power Analysis for SSD Design (1:30)
Kwanghyo Ahn, Hyungwoo Lee, Dongeun Lee, Jongbae Lee - *Samsung Electronics Co., Ltd., Hwaseong, Republic of Korea*

4.2 N2D2: A Deep Neural Networks Design, Optimization and Code Generation Framework for CoTS and Dedicated Hardware IPs (1:45)
Olivier Bichler, Alexandre Carbon, David Briand, Vincent Lorrain, Jean-Marc Philippe - *CEA-LIST, Gif-Sur-Yvette, France*

4.3 Using Virtual Platforms for Early Architectural Exploration: Experimentation on an Image Processing System (2:00)
Hubert Guérard - *Space Codesign Systems, Montreal, QC, Canada*
Eric Jenn - *IRT Saint-Exupery & Thales, Toulouse, France*
Guy Bois - *Space Codesign Systems, Montreal, QC, Canada*

4.4 The More the Merrier – Building Integrated Heterogeneous Virtual Platforms (2:15)
Jakob Engblom - *Intel Corp., Stockholm, Sweden*

4.5 Arch: A New Language for the Next Wave of Network-Connected Embedded Development (2:30)
Richard Moats, Bill Games - *Network Native & Rice University, Austin, TX*
Michael Brogioli - *Network Native, Austin, TX*

4.6 Automating Communication of Complex Data in FPGA Accelerated Software Systems (2:45)
Adam Sapek - *Microsoft Corporation, Redmond, WA*
Andrew Putnam, Daniel Lo - *Microsoft Research, Redmond, WA*
Derek Chiou, Kalin Ovtcharov, Shlomi Alkalay - *Microsoft Corporation, Redmond, WA*

Q &A Poster Session 2
Monday, June 19 5:00 - 6:00 - Exhibit Floor

Thank You to Our Sponsor

Mentor®
A Siemens Business

WELCOME TO AUSTIN

Austin is the capital of Texas, home of the University of Texas at Austin and gateway to the beautiful Hill Country. Shop in the one-of-a-kind boutiques that line South Congress and the 2nd Street district, or head out to hill country to relax in a world class destination spa.

More than 300 days of sunshine lend itself to a refreshing dip in Barton Springs or try stand-up paddle boarding on Lady Bird Lake. Find out more at austintexas.org.

5

DESIGNER TRACK: EMPOWERING DESIGN

Time: 1:30 - 3:00pm || Room: Ballroom F || Event Type: Reviewed Presentations Track: Design, EDA || Topic Area: Low-Power & Reliability, Physical Design & DFM, Digital Design

CHAIR:
Badhri Uppiliappan - *Analog Devices, Inc., Wilmington, MA*

This session will focus on all considerations for power and reliability. Minimizing power at chip level will be a focus, as well as ensuring electromigration sign-off in large and complex designs.

5.1 Resistance Driven Routing Methodology of Power Supply Network for Low Power and Multiple Voltage Design (1:30)
Makoto Minami, Mathieu S. Molongo, Kenji Aoyama, Chen Lingfeng, Zhu Xiaoke, Kouji Ishihara, **Nobuto Ono**, Shunichi Kuwata, Kazuhiro Miura - *Jedat, Inc., Tokyo, Japan*
Koutaro Hachiya - *Jedat, Inc., Chuo-ku, Japan*

5.2 Cost Effective Super Cut-Off Power Gating Circuits (1:45)
Insub Shin - *Samsung Electronics Co., Ltd., Gyeonggi-do, Republic of Korea*
Jaehan Jeon - *Cadence Design Systems, Inc., San Jose, CA*
Jun Seomun - *Samsung Electronics Co., Ltd., Yongin, Republic of Korea*
Wook Kim, Kyungtae Do - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*

5.3 ESD 2kV HBM – Case Study on Connecting Signal IO Cells to Bumps on a Flip-Chip SoC (2:00)
Pritesh Pawaskar - *Seagate Technology, LLC, Pune, India*
Yehuda Smooha - *Seagate Technology, LLC, Allentown, PA*
Anant Narain - *Apache Design, Inc., A Subsidiary of ANSYS, Inc., Noida, India*
Shrikrishna N. Mehetre - *Seagate Technology, LLC, Pune, India*

5.4 Comprehensive Power Rail Constraint Verification for Large Analog Designs at Early Stage (2:15)
Shuichi Teramoto - *Renesas System Design Co., Ltd., Kodaira-shi, Japan*
Hisato Inaba - *Renesas System Design Co., Ltd., Takasaki-shi, Japan*
Kunihiro Yanagida - *Mentor, A Siemens Business, Shinagawa-ku, Japan*

5.5 Physics-Based Electromigration Assessment for Analysis of EM Degradation in 3D IC Test Structures (2:30)
Jun-Ho Choy, Valeriy Sukharev - *Mentor, A Siemens Business, Fremont, CA*
Sandeep Chatterjee, Farid N. Najm - *Univ. of Toronto, Toronto, ON, Canada*
Stéphane Moreau - *CEA-LETI Minatec, Grenoble, France*

5.6 Machine Learning Based Electromigration Waiver System (2:45)
Ting Ku, Rex Lin - *NVIDIA Corporation, Santa Clara, CA*
Ajay Baranwal, Norman Chang, Rahul Rajan, Kanishka De, Mallik Vusirikala - *ASYS, Inc., San Jose, CA*

▶ **Q &A Poster Session 2**
Monday, June 19 5:00 - 6:00 - Exhibit Floor

Thank You to Our Sponsor

Mentor®
A Siemens Business

6

IP TRACK: THE IP PARADOX: GROWING BUSINESS DESPITE CONSOLIDATIONS

Time: 1:30 - 3:00pm || Room: Ballroom G || Event Type: Panel || Track: IP Topic Area: General Interest

MODERATOR
Dan Nenni - *SemiWiki.com, San Jose, CA*

ORGANIZER:
Eric Esteve - *IP-nest, Paris, France*

The Design IP has become the largest category of EDA in 2016/17 (ESD Alliance, 2016 report), growing by 10% YoY in spite of the semiconductor industry affected by consolidation and exponential SoC development cost. What are the market forces that are fueling IP business growth? IP license price increases? Number of IP in an SoC? Make vs Buy trends? These forces can be linked with price, number of IP in a SoCs, technology node and/or make vs buy trends. Is injection of money from International funds creating short term growth?

PANELISTS:

Elias Lozano - *Open-Silicon, Inc., San Jose, CA*
Sujoy Chakravarty - *SilabTech, Bangalore, India*
Chengyu Zhu - *Semconductor Manufacturing International Corp., San Jose, CA*
Sanjive Agarwala - *Texas Instruments, Inc., Dallas, TX*

Thank You to Our Sponsor

ChipEstimate.com

7

DESIGNER TRACK: SAFE PLATFORMS AND SOLUTIONS APPLIED IN HIGHLY AUTOMATED DRIVING

Time: 3:30 - 5:00pm || Room: Ballroom E || Event Type: Invited Presentations
Track: Automotive, Embedded Systems || Topic Area: Emerging Architectures & Technologies, SoC & Embedded System Architectures, Codesign & System Design

CHAIR:

Selma Saidi - *Univ. of Hamburg, Germany*

ORGANIZERS:

Rolf Ernst - *Technische Univ. Braunschweig, Germany*
Gerardo Daalderop - *NXP Semiconductors, Eindhoven, The Netherlands*

In many automotive applications, from Advanced Driver Assistance Systems (ADAS) to highly automatic and coordinated driving, high performance requirements have reached safety-critical, real-time architectures.

This entails a paradigm shift in programming and integration methods to meet tight timing and safety requirements demanded by safety standards, such as IEC 61508 or ISO 26262.

Consequently, to accommodate these partially contradictory requirements, new platforms and solutions from MPSoCs and software architectures to cyber-physical networking are necessary.

We begin with a short introduction to the field and continue with novel industrial solutions and research addressing the challenges.

In the first talk, NXP will present an architecture that applied in a next step-up in platooning including wireless communication and fail-operational modes.

Next, Elektrobit will present a SW platform for automated driving capable of comfort and safety updates.

Finally, TUBS will show a HW architecture allowing smooth transition from Multi- to Manycore systems in automotive context.

7.1 Architectures and Solutions Applied in Highly Automated Platooning (3:30)
Gerardo Daalderop - *NXP Semiconductors, Eindhoven, The Netherlands*
Tjerk Bijlsma - *TNO, Eindhoven, The Netherlands*
Geoffrey Waters - *NXP Semiconductors, Austin, TX*
Lars Reger - *NXP Semiconductors, Hamburg, Germany*

7.2 The Multifaceted Platform: New HAD Software Functions From Development to Volume Production (4:00)
Sebastian Ohl - *Elektrobit Automotive GmbH, Erlangen, Germany*

7.3 From Multi - to Manycore Systems in Safety-Critical Automotive Applications (4:30)
Adam Kostrzewa, Rolf Ernst - *Technische Univ. Braunschweig, Germany*

8

DESIGNER TRACK: GROWING IC DESIGN AND ECOSYSTEM IN CHINA: OPPORTUNITIES AND CHALLENGES

Time: 3:30 - 5:00pm || Room: Ballroom F || Event Type: Panel || Track: Design, EDA
Topic Area: Digital Design, General Interest

MODERATOR:

Junko Yoshida - *EE Times, Manhasset, NY*

ORGANIZER:

Zhuo Li - *Cadence Design Systems, Inc., Austin, TX*
Jason Xing - *ICScape Inc., San Jose, CA*

China has now become the largest semiconductor market in the world. About 1/3 of consumer electronic circuits are based on demand from China. While there is still high dependency for chip supplies from US and Europe, there is a growing trend that more chips are designed in China, from both design teams in big global companies, as well as fast growing domestic companies. The high growth rate now extends from traditional manufacturing and packaging sectors to the IC design area. According to some data sources, the CAGR of chip design sector from 2000 to 2015 is about 45%. China domestic chip industry is about 22% of global market share and contributes to the global semiconductor growth. At the same time, such growth is limited to certain types of chips, such as ASIC, communication chips, FPGA and some mixed-signal circuits, and there is clearly a shortage on high end IC designs. How does the growth in China change the chip design and manufacturing industry globally? Is that a threat or win-win for US and Europe IC design companies? Will consumer market in China boost global semiconductor industry? In this panel, the executives from design, manufacturing and EDA companies in China, as well as research directors from US and Europe will share their views on these questions and discuss opportunities and challenges for growing IC design and ecosystem in China.

PANELISTS:

Xiaoning Qi - *Hangzhou C-Sky Microsystems Co. Ltd., Hangzhou, China*
Weiping Liu - *Huada Empyrean Software Co., Ltd, Beijing, China*
Nanxiang Chen - *China Resources Microelectronics Ltd., Wuxi, China*
Ahmed Jerraya - *CEA Tech, Grenoble, France*
TianShen Tang - *Semiconductor Manufacturing International Corp., Shanghai, China*

9

IP TRACK: MINIMIZING IC POWER CONSUMPTION: TOP DOWN OR BOTTOM UP DESIGN METHODOLOGY. WHAT IS THE STARTING POINT?

Time: 3:30 - 5:00pm || Room: Ballroom G || Event Type: Panel || Track: IP, Design
Topic Area: Low-Power & Reliability

MODERATOR:

John Blyler - *Electronic Design Magazine, Portland, OR*

ORGANIZER:

Farzad Zarrinfar - *Mentor, A Siemens Business, San Jose, CA*

In this panel, implementation techniques and tradeoffs for designing ultra Low-power Semiconductor IP, SOCs, ASSPs, and ASICs will be discussed. These techniques are critical for devices requiring thermal management, are battery-powered and need package cost reduction. IP suppliers and EDA vendors now offer low-power IPs with optimization tools.

Topics such as FinFet and FDSOI devices will be compared with planar CMOS, power harvesting, and using UPF for low power implementation.

Designers apply reduced or Dynamic Voltage & Frequency Scaling, power shutdown, and retention logic. Typical low-power designs have over 30 different power modes and domains. Dual-rail memories operate in full power, partial power, or shutoff modes. Designs include isolation cells, level shifters, and retention cells with multiple modules in each power domain.

Optimization of these techniques for various applications such as portable Gaming, IOT, Automotive, Wireless, Networking, wearable computing. low power techniques are paramount for differentiation and gaining market share.

PANELISTS:

Aditya Mukherjee - *Microsoft Corporation, Mountain View, CA*
Tim Saxe - *QuickLogic Corp., San Fransisco Bay Area, CA*
Abhishek Ranjan - *Mentor, A Siemens Business, Noida, India*
Ronald Martino - *NXP Semiconductors, Austin, TX*
Lluis Paris - *Taiwan Semiconductor Manufacturing Co., Ltd., San Jose, CA*
Jon Adams - *ON Semiconductor, San Jose, CA*

Thank You to Our Sponsor

ChipEstimate.com

DESIGNER/IP TRACK POSTER SESSION

Time: 5:00 - 6:00pm || Room: Exhibit Floor || Event Type: Poster Session
Track: Design, IP || Topic Area: General Interest

During the poster presentation, you will interact directly with poster presenters in a small group setting.

As the limited time available in the Designer/IP Track session program was exceeded by the quantity of great submitted content, we present the following posters in the Designer/IP Track Poster Session held Monday, June 19 from 5:00 to 6:00pm on the Exhibit Floor.

Thank You to Our Sponsors

Mentor® A Siemens Business

ChipEstimate.com

122.1 Converging Designs in Nanometer Era
Ambar Mukherji - *Intel Corp., Bangalore, India*
Niraj A. Mehta - *Intel Technology India Pvt. Ltd, Bangalore, India*

122.2 Novel Method for Test Time Reduction in Scan Optimization
George Antony - *IBM Systems and Technology Group & Indian Institute of Technology Madras, Bangalore, India*
Mary P. Kusko - *IBM Corp., Poughkeepsie, NY*
Sridhar Rangarajan - *IBM Corp., Bangalore, India*
Shrinivas Shenoy - *IBM Corp., Bengaluru, India*

122.3 Programmable Repeater Station Approach for Hierarchical SoC
Jasmeet Singh, Suresh Raman, Subbarao Govardhanagiri - *Xilinx Inc., Hyderabad, India*

122.4 Flexible Hierarchy Management in the IBM Microprocessor Flow
Alex Suess - *IBM Server and Technology Group, Poughkeepsie, NY*
Michael Kazda - *IBM Systems and Technology Group, Poughkeepsie, NY*
Friedrich Schroeder, Peter Verwegen, Niels Fricke - *IBM Deutschland Research & Development GmbH, Boeblingen, Germany*

122.5 A Method for Efficient Design Closure Using Incremental Synthesis
Vinay K. Singh - *IBM Corp., Bangalore, India*
George Antony - *IBM Systems and Technology Group & Indian Institute of Technology Madras, Bangalore, India*
Sridhar Rangarajan - *IBM Corp., Bangalore, India*

122.6 Reducing Noise Impact on Function by Isolation Routing
Michael Kazda - *IBM Systems and Technology Group, Poughkeepsie, NY*
Dirk Müller - *Univ. of Bonn, Germany*
Christian Schulte - *IBM Systems and Technology Group, Boeblingen, Germany*

122.7 SDC Exceptions Verification: Bridge Functionality and Timing with Confidence
Vlad Goldman - *Marvell Semiconductor, Inc., Yokneam, Israel*

122.8 Next Generation Power Grid Prototyping and Package-Aware Analysis of High-Current Transient Events
Yiyong (Eason) Sun, **Dawn M. Graves** - *Xilinx Inc., San Jose, CA*
Anusha Prakash - *ANSYS, Inc., San Jose, CA*

DESIGNER/IP TRACK POSTER SESSION

122.9 Effective CTS Strategy on Multi-Scenario Complex Clock Design
Wei Wei - *Huawei Technologies Co., Ltd. & HiSilicon, Shenzhen, China*
Xiao Yong - *Huada Empyrean Software Co., Ltd, Beijing, China*

122.10 A Vectorless Methodology for Drop-Aware Early PDN Optimization of Scan Chains
Arun James - *Broadcom Limited, Bengaluru, India*
Abhijith MV - *ANSYS, Inc., Bangalore, India*

122.11 Prototyping of Power Grid in 7nm Designs
Yongchan Ban - *GLOBALFOUNDRIES, Santa Clara, CA*
Jongwook Kye - *GLOBALFOUNDRIES, Sunnyvale, CA*

122.12 Clock Trees with Low Process Variation - Part 2
Gary Ellis - *Encore Semi Inc. & GLOBALFOUNDRIES, Norman, OK*
Mark Lasher - *GLOBALFOUNDRIES, Williston, VT*
Bertram L. Bradley - *GLOBALFOUNDRIES, Austin, TX*
Phillip Normand - *GLOBALFOUNDRIES, Chippewa Falls, WI*

122.13 Timing Rule Verification Tool for Custom Circuit Macros
Ben Bowers, **Josh Puckett** - *Qualcomm Technologies, Inc., Raleigh, NC*

122.14 Timing Optimization by Utilizing Net-Based Target Congestion Ratios in Routing
Diwesh Pandey, - *IBM Systems and Technology Group, Bangalore, India*
Sven Peyer - *IBM Systems and Technology Group, Boeblingen, Germany*
Yaoguang Wei - *IBM Corp., Austin, TX*

122.15 Significantly Improving Place & Route Runtime by Minimizing Clocks/Register
Kalyan R. Hampapuram, **Venkatraman Ramakrishnan** - *Texas Instruments India Pvt. Ltd., Bangalore, India*

122.16 Securing an IP Product in the World of Automotive Validation
Brian Eplett, Randy Caplan - *Silicon Creations, Suwanee, GA*
Emmanuel Peddi - *Silicon Creations & IEEE, Suwanee, GA*
Greg Curtis - *Mentor; A Siemens Business, Wilsonville, OR*

122.17 Customising APIS IQ Software for ISO26262 Safety Analysis
Krishnapriya C. Ramamoorthy, David Addison - *Infineon Technologies UK Ltd., Bristol, United Kingdom*

122.18 A Cost-Effective IP Integration & Design Restructuring Methodology for Large SoC Designs at RTL
Ishay Vaisid, Sara Hassar - *Marvell Semiconductor, Inc., Yokneam, Israel*
Sylvain Danjean - *DeFacTo Technologies, Grenoble, France*
Chouki Aktouf - *DeFacTo Technologies, Moirans, France*

122.19 Augmentation of Static and Dynamic Checks for Electrical Verification of Mixed Signal Circuits
Deepon Saha, Krishnan T. Sukumar, Hariprasad TT - *Advanced Micro Devices, Inc., Bangalore, India*

122.20 Custom Decap Analysis Flow for Accurate EM/IR Sign-Off
Deepon Saha, Hariprasad TT, Krishnan T. Sukumar - *Advanced Micro Devices, Inc., Bagalore, India*

122.21 Managing CSR Design Complexity Using a Single-Source, Unified-Flow Approach
Dave Burgoon - *Microsoft Corporation, Fort Collins, CO*
Miguel Comparan - *Microsoft Corporation, Redmond, WA*

122.22 A High Level Synthesis (HLS) Design Flow for Scaling to Multiple IP, SoC, & Process Targets
Hans L. Yeager - *Qualcomm Datacenter Technologies, Inc., Raleigh, NC*
Chris Platt - *Qualcomm Technologies, Inc., Boulder, CO*
Anoop Lobo - *Qualcomm Technologies, Inc., San Diego, CA*

122.23 Low Power IP Design Exploration Using RTL Power Flow
Ashish Mishra - *Qualcomm India Pvt. Ltd., Bangalore, India*
Saurabh Shrimal - *Mentor, A Siemens Business (India) Pvt. Ltd., Noida, India*
Gopi Dabbadi - *Qualcomm India Pvt. Ltd., Bangalore, India*

122.24 RTL Power Bug Review System
Sali Huang - *MediaTek, Inc., Hsinchu, Taiwan*

122.25 Evolved Supply Set based UPF Methodology
Aman Jain - *Seagate Technology, LLC, Pune, India*

Thank You to Our Sponsors

Mentor® A Siemens Business

ChipEstimate.com™

WELCOME TO AUSTIN

Austin is the capital of Texas, home of the University of Texas at Austin and gateway to the beautiful Hill Country. As the Live Music Capital of the World, the city has a soundtrack all its own.

More than 250 live music venues flourish with rock, indie, pop and Tejano. Top notch restaurants with legendary barbeque and farm-to-table cuisine whet your appetite.
Find out more at austintexas.org.

T1

TUTORIAL 1: LINUX BRING UP ON HETEROGENEOUS MULTIPROCESSOR SOCS

Time: 10:30am - 12:00pm || Room: 17AB || Event Type: Monday Tutorial
Track: Embedded Systems, IP || Topic Area: Embedded System Software, SoC & Embedded System Architectures, Emerging Architectures & Technologies

ORGANIZER:

Larry Lapides - *Imperas Software Ltd., Thame, United Kingdom*

Heterogeneous multiprocessor SoCs are becoming more common for use in application areas such as advanced driver assistance systems (ADAS) and autonomous vehicles, networking, industrial automation, security, video analytics and machine learning. These SoCs often have GPUs and/or hardware accelerator units that work together on a common set of data, however, the simplest coherent processing systems use multiple clusters of CPUs. These CPU clusters can be homogeneous, or heterogeneous, such as with ARM's big.LITTLE configuration or Imagination's MIPS I6500 architecture.

Linux has become the general purpose operating system of choice for embedded systems, and now for these heterogeneous multi-cluster architectures Linux needs to be modified to support the coherence between the clusters, as well as whatever differences exist between the clusters in terms of number of processors, processor type, and other features and capabilities. Most vendors use an open source Linux distribution from their processor IP vendor, then build a custom distribution representing the cluster/processor configuration and device tree supported for the specific SoC. This custom Linux distribution needs to include the necessary drivers for the peripherals on the SoC, as well as supporting other customizations and unique features. Obviously, this gets quite complex, and the complexity keeps increasing with increasing device complexity, including coherence.

This need to port, customize and bring up Linux on these heterogeneous SoCs requires significant engineering effort by the SoC developer. Also, their customers do not always reward this effort by paying more for the SoCs. So how can the semiconductor vendors make this Linux task more efficient? What are the best practices for Linux porting and bring up on heterogeneous multi-cluster/multiprocessor SoCs?

This tutorial is presented in two sections. In the first section (Imagination Technologies), the various components of the Linux distribution are covered, including the basic Linux kernel, device trees and other customizations, SMP variations and drivers, both static and dynamic. Coherency for multi-cluster architectures is also discussed. The methodology used for bring up of the Linux kernel, starting with boot loaders including U-boot, on hardware is presented.

The second section (Imperas) discusses the development of a robust test environment using virtual platform technology. The virtual platform provides a complementary approach to porting and bring-up on hardware. The benefits of controllability, observability and repeatability for virtual platform use are covered. Automated testing, such as needed for an Agile Continuous Integration (CI) development and test methodology is discussed. Specific OS-aware tools are also highlighted, plus other tools such as non-intrusive memory monitors, the use of software assertions, and code and functional coverage techniques for the operating system and drivers.

SPEAKERS:

John Min - *Imagination Technologies Ltd., Santa Clara, CA*
Simon Davidmann - *Imperas Software Ltd., Thame, United Kingdom*

T2

TUTORIAL 2: SECURITY VALIDATION IN MODERN SYSTEMS-ON-CHIP

Time: 10:30am - 12:00pm || Room: 18AB || Event Type: Monday Tutorial
Track: Security || Topic Area: Test & Verification, SoC & Embedded System Architectures

Modern systems-on-chip (SoCs) implement many security features to protect various assets like end user data, keys, fuses and OEM assets. As hardware security features and related attacks are increasing, functional validation of these security features is proving inadequate to address these challenges. While functional validation ensures proper functionality of the product, security validation allows for a more secure and robust product by evaluating features with security implications, analyzing the security impact and business risk of bugs/vulnerabilities that are discovered, and verifying bug fixes.

In this tutorial, using a generic System on Chip (SoC) as an example, we describe a security assurance methodology, some recent research results and discuss some open problems for the hardware security community. The focus areas of the tutorial are based in part on the learnings from security evaluations performed on commercial (Intel) products as well as our own expertise. This tutorial will be organized as follows:

Part I (Security Architecture): To lay foundation for the security assurance process, we describe the general security architecture features such as access control, isolation and cryptographic primitives using a simple and generic SoC architecture. We will describe the security objectives, security requirements of this SoC, the adversary model and the threat model under consideration.

Part II (Common HW Security Vulnerabilities): We will describe the concepts of vulnerability analysis and determine the severity of some example hardware and firmware vulnerabilities. We will suggest a generic classification of hardware security vulnerabilities and common mitigation techniques.

Part III (Methodology for SoC Validation): We describe our methodology and best known methods for SoC security validation. We first show how SoC security requirements are translated into specific validation objectives. We will then discuss tools and techniques -- such as randomized testing and formal/semi-formal methods for information-flow verification -- that can be used to ensure these objectives are met by the SoC. We will conclude with a discussion of open research challenges in SoC security validation.

The topics covered are generally applicable to all SoC products. Through this tutorial, we are looking to engage with security researchers from academia and industry and hope this will eventually lead to the development of improved security validation techniques and best practices.

SPEAKERS:

Sharad Malik - *Princeton Univ., Princeton, NJ*
Jason M. Fung - *Intel Corp., Hillsboro, OR*
Pramod Subramanyan - *Univ. of California, Berkeley, CA*

**Tutorials require special registration.*

T3

TUTORIAL 3: MULTICORE SOFTWARE DEVELOPMENT ON ARM

Time: 10:30am - 12:00pm || Room: 19AB || Event Type: Monday Tutorial
Track: Embedded Systems || Topic Area: Embedded System Software

An increasing number of embedded systems are built on a multicore architecture, whether this be a homegeneous collection of identical processors or a heterogeneous set of specialised processors. In either case, a multiplicity of symmetric and asymmetric programming paradigms are possible. Whatever the chosen software architecture, ultimately the design is built on top of hardware features provided by the processor and the surrounding bus and memory fabric which support software deployment and execution across multiple processors.

A solid understanding of these features and how they are employed by bare metal applications and operating systems is essential when designing a performant software architecture.

The first part of this session will examine multicore software architectures and then provide a comprehensive tutorial on the architectural and implementation features of hardware platforms which make them possible. Among other features, this will include hardware and software cache coherency, memory coherency, locks and semaphores, interprocess and interprocessor communication, interrupt management and distribution, multicore booting, memory management, context switching and power management. Examples, where applicable, will be drawn from the ARM architecture.

In the second part, David Black will look at the higher-level aspects of designing and architecting a software system to exploit a multiprocessing architecture. He will outline a variety of multi-processing design decomposition architectures, how to model the data flow between different processing elements, how to statically and dynamically configure process scheduling to avoid lockup, and how to interact with power management subsystems to dynamically control system power consumption and operating frequency.

Intended Audience: Embedded system software engineers

Pre-requisites: Experience of embedded software development

About the Speakers:

Chris Shore, Director, Technical Marketing at ARM Ltd

Chris has worked at ARM for over 16 years, currently as Director, Technical Marketing. For the previous 15 years, he was responsible for ARM's customer training activity – delivering over 200 training courses every year to ARM's customers and end users all over the world. He also managed ARM's Active Assist onsite services and the ARM Approved partner program.

Chris is a regular speaker at conferences and industry events and has addressed audiences on ARM technology on every continent except Antarctica - opportunities there are limited but it is surely only a matter of time!

Chris has lived and worked in Cambridge for over 30 years. He holds an MA in Computer Science from Cambridge University, is a Chartered Engineer and a member of the Institute of Engineering and Technology (MIET).

David Black, Senior Member of Technical Staff, Doulos Ltd

David works for Doulos as an expert trainer in multiple technical languages as well as ARM processors. He holds ARM AAE and AAME certifications. His bleeding edge experiences in industry led to the co-authoring books and papers like "SystemC from the Ground Up", which provides helpful SystemC knowledge to the novice, even to today.

David spends considerable time investigating and creating useful white papers for the Doulos and hitech community, most recently, "Migrating to UVM 1.2" and "Transforming Slow Software into Fast Hardware using Vivado HLS", including webinars and source code for both. Today's presentation is a good example of the practicality and applicability of David's investigations.

David's home is Austin, Texas, the heartthrob of the state, though on any day he could be in any state or country providing Doulos training ranging from SystemC/TLM-2.0 and SystemVerilog/UVM to serveral ARM processor training sessions, and including Doulos training for the novice such as Embedded C programming.

SPEAKERS:

Chris Shore - *ARM Ltd., Cambridge, United Kingdom*
David Black - *Doulos Ltd., Austin, TX*

**Tutorials require special registration.*

T4

TUTORIAL 4: MACHINE LEARNING AND SYSTEMS FOR BUILDING THE NEXT GENERATION EDA TOOLS

Time: 10:30am - 12:00pm || Room: 18CD || Event Type: Monday Tutorial
Track: EDA || Topic Area: General Interest, Emerging Architectures & Technologies

ORGANIZER:

Manish Pandey - *Synopsys, Inc., Mountain View, CA*

This tutorial covers the basics of machine learning, systems and infrastructure considerations for performing machine learning at scale, specialized hardware architectures for neural networks, and approaches for using machine learning for building the next generation of EDA tools.

The tutorial starts with Naïve Bayes, Support Vector Machines, and Decision Trees, followed by blackbox classifier training with gradient descent. With examples, the tutorial illustrates feature selection, model validation and how to avoid overfitting machine learning models. Dimensionality reduction techniques become important for data with high dimensionality for reducing computational and storage requirements. We discuss singular value decomposition (SVD), and principal component analysis (PCA) techniques for dimensionality reduction.

Next, the tutorial discusses k-means clustering for unsupervised learning, and efficient parallel algorithms for solving this problem for large datasets.

The tutorial proceeds on to deep network training and simple convolutional neural networks. It covers common neural net architectures, including ResNet, and Recurrent Neural Networks (RNNs), that are commonly used for many pattern recognition tasks.

We then covers topics related to performing machine learning at scale on large data sets, starting with the performance and throughput limitations of traditional compute and storage systems, and software frameworks that help solve these problems.

We discuss one such framework, Apache Sparc, and MLlib, a distributed machine learning library, which simplifies creation of large scale parallel machine learning pipelines.

Hardware assisted-speedups are becoming increasingly common for machine learning. We discuss how some of the algorithms take advantage of GPUs to deliver an order of magnitude speedup. We also discuss emerging trends of purpose built processors and hardware for acceleration of deep learning. In particular, we discuss new approaches for efficiently representing and computing deep neural networks, with compression, weight sharing and other optimizations that yield orders of magnitude of power efficiency and computational speedup over conventional CPU/GPU architectures.

Finally, the tutorial describes several ways in which machine learning can be applied to solve common optimization and classification problems encountered in the traditional CAD flows. We discuss several problems, including logic optimization, functional verification, and debug that can benefit from machine learning.

SPEAKERS:

Manish Pandey - *Synopsys, Inc., Mountain View, CA*
Claudionor Coelho - *NVXL Technologies, Fremont, CA*

T5

TUTORIAL 5: HANDS-ON IOT TUTORIAL: CONNECTING DEVICES TO THE CLOUD VIA AN IOT DESIGN PLATFORM

Time: 1:30 - 5:00pm || Room: 17AB || Event Type: Monday Tutorial || Track: IoT
Topic Area: Codesign & System Design, Embedded System Software, Digital Design

IoT systems promise to play a central role in smart cities, health tech, retail, home, supply chain, wearables, transportation and other domains. Current IoT systems consist of various building blocks including smart devices for sensing and actuation, networking components, and cloud platforms. Most current IoT designs are ad hoc and far from optimal in terms of latency, power dissipation, quality of service, and other performance metrics. Design automation of IoT systems in the form of specification, synthesis, simulation and optimization is still a nascent science, requiring expert knowledge in all facets of IoT design.

The goals of this tutorial are to present fundamental concepts in IoT system design and apply them in the form of a series of hands-on exercises, and to outline some promising research directions.

The tutorial will cover the following:

1. Short overview of IoT, and its value proposition, highlighting key findings from a recent McKenzie report on IoT
2. Program an Arduino and its WiFi shield, and configure the Arduino to operate as a server or client, and measuring the latency and bandwidth of a client-server application
3. Review of the IoT Network stack, and programming the Arduino to communicate with a cloud database using REST and MQTT
4. Use the ThingWorx IoT design platform to model and instantiate devices as objects, and compose a visualization mashup for real-time visualization for temperature and humidity data collected via Arduinos
5. Use Thingworx IoT design platform to orchestrate and transform data between different clouds

Attendees should be proficient in C/C++ programming, and should bring their own laptop. Arduino hardware and sensors will be provided

SPEAKERS:

Soha Hassoun - *Tufts Univ., Medford, MA*
Benjamin Norman - *PTC, Needham, MA*

**Tutorials require special registration.*

T6

TUTORIAL 6: LOGIC SYNTHESIS IS EVERYWHERE

Time: 1:30 - 3:00pm || Room: 18AB || Event Type: Monday Tutorial
Track: EDA, Design || Topic Area: Logic & High-Level Synthesis, Emerging Architectures & Technologies, Digital Design

ORGANIZER:

Mathias Soeken - *École Polytechnique Fédérale de Lausanne, Switzerland*

Logic synthesis, which is the design of logic circuits and their optimization, emerged in the 1950s with pioneering work at Bell Laboratories and IBM Research. Until today logic synthesis systems enabled the widespread use of semicustom logic design by assisting designers in the development of system- and word-level models to optimized gate-level netlists. Logic synthesis algorithms have always been facing the challenge to handle designs with an extremely large number of gates. Consequently, logic synthesis and digitial design have used and led to some of the most important and intriguing algorithms and data structures in computer science; the Quine-McCluskey algorithm and binary decision diagrams are probably one of the most notable ones. Today, logic synthesis is applied to larger and more complex design problems and therefore advancing the use of algorithms and data structures in logic synthesis systems is inevitable.

In this tutorial, we present today's challenging design problems and solutions to them. The tutorial covers three parts: (i) the use of Boolean satisfiability techniques to scale logic synthesis algorithms, (ii) new data structures and algorithms for delay optimization, and (iii) the application of logic synthesis in the design of quantum computers.

In the first part, it is shown how SAT solvers can be used to implement classical logic synthesis algorithms, such as technology mapping, LUT mapping, collapsing, and logic rewriting, in order to obtain better quality and higher flexibility. Key is to tightly integrate one or more SAT solvers into the algorithm and use them in an agile and reliable way. It is shown how SAT solvers can be used to generate canonical solutions. Consequently, SAT solvers can be used as a replacement for decision diagrams, retaining all their benefits but avoiding drawbacks such as memory explosion.

The second part introduces new algorithms and data structures for delay optimization, a crucial optimization criteria. An enumeration based algorithm is introduced that allows to find optimum networks for given delay constraints. Majority-inverter graphs are introduced as a logic data structure that allows for significant delay optimization due to effective algebraic rewriting techniques.

The third part illustrates an emerging application of logic synthesis. It shows how classical logic synthesis algorithms can be applied for the scalable design of quantum computers. Recent progress in fabrication makes the practical application of quantum computers a tangible prospect. And as quantum computers scale up to tackle problems in computational chemistry, machine learning, and cryptoanalysis, logic synthesis and design automation will be necessary to fully leverage the power of this emerging computational model.

This tutorial shows the state-of-the-art and research frontier of today's logic synthesis algorithms. The tutorial is supported by the use of state-of-the-art academic and industrial tools.

SPEAKERS:

Alan Mishchenko - *Univ. of California, Berkeley, CA*
Luca Amaru - *Synopsys, Inc., Sunnyvale, CA*
Mathias Soeken - *École Polytechnique Fédérale de Lausanne, Switzerland*
Robert Brayton - *Univ. of California, Berkeley, CA*

**Tutorials require special registration.*

T7

TUTORIAL 7: THE FUTURE OF SOC SYSTEM VALIDATION & DEBUG... AND WHY YOU SHOULD CARE!

Time: 1:30 - 5:00pm || Room: 19AB || Event Type: Monday Tutorial
Track: Design, Embedded Systems || Topic Area: Test & Verification, Embedded System Software, Codesign & System Design

ORGANIZERS:

Priyadarsan Patra - *Intel Corp., Chandler, AZ*
Nicola Nicolici - *McMaster Univ., Hamilton, ON, Canada*

Troubleshooting how and why systems fail, and preventing such flaws are of critical importance during the product development life cycle and it is rapidly growing in industry significance. System Validation and Debug (SVD) is needed for correcting/improving the design function/performance/power, process monitoring and yield improvement, failure mode learning for research and development, or just getting a working first prototype. This detective work is however inherently cumbersome and challenging. Sources of difficulty include system complexity, limited physical access, error reproducibility, large data logs, and so on. Efficient solutions for system validation and debug have a much needed and highly visible impact on productivity and business value.

After introductory remarks, five of the IEEE-CEDA System Validation and Debug Technology Committee member experts will provide greater understanding and appreciation in the following areas:

- The main characteristics and challenges in a taxonomy of validation domains -- from Analog & Electrical Validation to Power & Performance Validation to Fullchip Functional Validation to Reliability, Marginality to Security and Compliance validation.

A System Level Validation Reality Check (good, bad, and the ugly) will be provided.

- Firmware (FW) debug in early-boot, run-time, and low-power debug scenarios - Firmware is a type of software that provides control, monitoring and data manipulation. Typical examples of devices containing FW are computing and embedded systems, such as personal computers, peripherals, mobile phones, cameras, watches, etc. FW consists of many techniques, starting with printing statements to the use of post-codes for PCs to ICE/JTAG debuggers etc. With the emergence of complex low-power processors/embedded controllers, FW debug needs to consider the three major aforementioned scenarios.
- Concurrency validation is one of most critical pieces required for the deployment of successful silicon which involves system-level interacting traffic and events from multiple intellectual property (IP) blocks. Concurrency tests typically target issues in arbitration, traffic priority, credits/flow controls, ordering rules, address holes, etc., created by traffic from IP blocks. It involves carefully crafting content to generate traffic with tight control to create a right scenarios mixed with randomly hitting events/transactions. Here we discuss the three cornerstones of concurrency validation - namely, validation content, coverage metrics and debug hooks.
- Validation of security features in post-silicon - It is a major challenge to verify the security and trust requirements of system-on-a-chip (SoC) designs, primarily due to the fact that they are designed using various hardware, software and firmware IP blocks to reduce cost. Growing reliance on these 'pre-verified' IPs, often gathered from untrusted third-party vendors, severely affects the security and trustworthiness of SoC platforms. These IPs may come with malicious or accidental vulnerabilities and undesired modifications, which are extremely difficult to detect during manufacturing test since they are usually triggered by a sequence of rare events. In this section of the tutorial, we discuss how to effectively combine logic testing with side channel analysis to combine their relative advantages.
- The tutorial will conclude with two real case studies, one involving detection and root causing of a security bug and another on a coherency bug.

SPEAKERS:

Sharad Kumar - *NXP Semiconductors, Delhi, India*
John Schumann - *IBM Corp., Austin, TX*
Sukhbinder Singh - *Intel Corp., Portland, OR*
Sankaran Menon - *Intel Corp., Austin, TX*
Prabhat Mishra - *Univ. of Florida, Gainesville, FL*

**Tutorials require special registration.*

T8

TUTORIAL 8: AN INTRODUCTION TO THE ACCELLERA PORTABLE STIMULUS STANDARD

Time: 1:30 - 3:00pm || Room: 18CD || Event Type: Monday Tutorial || Track: EDA, Embedded Systems || Topic Area: Test & Verification, Embedded System Software, Codesign & System Design

ORGANIZER:

Tom Fitzpatrick - *Mentor, A Siemens Business, Groton, MA*

Much of the history of electronic design automation (EDA) has involved replacement of manual effort by automated processes. Place-and-route tools replaced hand layout, logic synthesis supplanted gate-level netlists, and constrained-random testbenches reduced or eliminated hand-written test vectors. Standardized formats used as input to the automation tools include SystemVerilog, Property Specification Language (PSL), and the Universal Verification Methodology (UVM).

In 2014, the Accellera standards organization observed that the level of automation provided by the UVM was insufficient to provide portability across all phases of chip verification. The Portable Stimulus Working Group (PSWG) was formed in December of that year to standardize "portable stimulus" models that can be used to generate tests at multiple integration levels and across multiple verification platforms.

The PSWG is nearing completion of the first phase of its work to define a standard for portable test and stimulus models. The group has defined a declarative domain-specific language (DSL) with an alternative semantically-equivalent C++ input format to specify these models. Users can choose either format or mix and match models from different sources, as well as incorporate legacy code into the models via a direct procedural interface.

The new standard will raise the abstraction level of stimulus and test intent specification by modeling resource and data dependencies of behaviors, and composing them into scenarios using flow graphs. The abstract model can be analyzed by tools to solve constraints and dependencies at the scenario level, from which, along with a hardware/software interface library, target implementations may be automatically generated for the desired platforms.

This tutorial is an introduction to the standard, starting with background on the intended scope and defining goals. The main concepts behind the standard will be reviewed, including the key semantics underlying the model formats. Portable stimulus is not intended as a replacement for the UVM, but rather as a complement to it.The tutorial provides guidance on when and where the new methodology can be applied for maximum benefit on a chip project. Attendees will learn how to:

- Develop abstract, portable test and stimulus models for their chip designs
- Use constraints to guide randomization of both data and control flow
- Create low level driver sequences or reuse existing low-level sequences or drivers in the generation of tests
- Generate tests tuned for IP, subsystem, and full system verification
- Execute the generated tests across all verification engines: virtual platforms, simulation, acceleration, emulation, FPGA prototype, and silicon in the bring-up lab
- Specify and gather coverage metrics at every step to assess verification completeness

The tutorial takes a building-block approach, starting with simple models and showing how these can be expanded and combined for more complex designs and more sophisticated verification scenarios. The ultimate goal is to generate use cases that reflect how the chip will be used in real applications.

Attendees will learn how to use the standard to specify and verify realistic system-level behavior, and will leave the tutorial educated on the value of portable stimulus and the basics of the standard.

SPEAKERS:

Faris Khundakjie - *Intel Corp., Hudson, MA*
Tom Fitzpatrick - *Mentor, A Siemens Business, Groton, MA*
Sharon Rosenberg - *Cadence Design Systems, Inc., Petah Tikva, Israel*
Adnan Hamid - *Breker Verification Systems, Inc., San Jose, CA*
Srivatsa Vasudevan - *Synopsys, Inc., Mountain View, CA*
Karthick Gururaj - *Vayavya Labs Pvt., Ltd., Bangalore, India*

**Tutorials require special registration.*

T9

TUTORIAL 9: HOW POWER MODELING STANDARDS POWER YOUR DESIGNS

Time: 3:30 - 5:00pm || Room: 18AB || Event Type: Monday Tutorial
Track: EDA, Embedded Systems || Topic Area: Digital Design, Low-Power & Reliability, Simulation & Timing Analysis

ORGANIZER:

Jerry Frenkil - *Silicon Integration Initiative, Inc., Austin, TX*

Energy and power concerns continue to grow and become more challenging in all design phases. Increasing attention is being paid to modeling techniques for system- and software-level power management.

Today, multiple modeling standards are being developed to address these challenges, covering the full range from low-level hardware to high-level software. Each standard is evolving to address particular problems, but the modeling space is sufficiently large that different capabilities are needed to cover highly varied applications and methodologies.

Due to the wide range of design and application scenarios, one modeling technology does not fill all power modeling needs.

Software-level power modeling, representing a system's power characteristics, forms a programmer's view of power behavior. In this approach, all major hardware functions and how to control their power characteristics are abstracted. Functions can be put into low-power states as often as possible by real-time power management software.

System-level power modeling tends to focus on the hardware description of the system and its power behavior.

The system may be described in System C or RTL, or even in spreadsheets during the earliest design phases. It often focuses on meeting localized thermal constraints.

Both of these modeling approaches differ from conventional gate-level modeling in which process-voltage-temperature (PVT) specific power models are built only for primitive logic cells, such as Nand and Nor gates, multiplexors, and flip-flops.

This tutorial will present the latest state of the IEEE 1801, 2415, and 2416 power standards, and show why multiple standards are required to cover the broad design and operational space. Speakers will explain the features of these three standards and how they enable new capabilities and power management methods. Early users of the standards and underlying technologies will describe how the new modeling capabilities impacted their design processes and end products.

- Developers of the 1801 standard for Power Intent will describe recent extensions for Power State modeling. These enhancements enable the description of the power state space for IP Blocks and hardware systems.
- Developers of the 2415 standard, currently in development, will describe their work on a power hardware abstraction and layer based upon the Linux Device Tree. Prototype usage of this hardware abstraction will also be presented.
- Developers of the 2416 standard for Power Data modeling, also currently in development, will describe their power contributor approach for PVT independent power modeling.

They will also describe how such models can be used with conventional gate- level tools and system-level modeling, including detailed electro-thermal analyses.

This tutorial is intended for engineers concerned about power (software, EDA, IP, and SoC developers) who want to understand advanced power modeling, and which standard is best applied to different applications.

Attendees will learn about PVT independent power modeling, its uses and advantages, power state modeling, system level hardware power modeling, and software power modeling.

SPEAKERS:

Nagu Dhanwada - *IBM Systems Group, Poughkeepsie, NY*
Jerry Frenkil - *Silicon Integration Initiative, Inc., Austin, TX*
Davorin Mista - *Aggios, Inc., Irvine, CA*
Amit Srivastava - *Synopsys, Inc., Mountain View, CA*

**Tutorials require special registration.*

See More Great Content in the DAC Pavilion! Complete schedule can be found on Pages 97 - 101, Additional Meetings: See Pages 89 - 95.

KEYNOTE: THE AGE OF DIGITAL TRANSFORMATION

CHUCK GRINDSTAFF – *Siemens PLM Software Inc., Plano, TX*

Time: 9:00 – 10:00am || Room: Ballroom A || Track: Design
Topic Area: General Interest

EDA has continually moved to higher levels of abstractions, changing how electronics are designed and created. Now we are seeing the need in the industrial world for further digitalization and virtualization.

In his keynote, Chuck Grindstaff, Executive Chairman of Siemens PLM Software, will discuss the global impact of this digital transformation. EDA pioneered this revolution and paved the way for today's digital industrial revolution that is transforming and disrupting all industries. For system companies, their products are evolving into advanced system of systems. As a result, SoCs and application software are now the core differentiation and enabling technologies. This is spurring growth and opportunity for IC designers in the convergence of semiconductor and systems. Siemens and Mentor together are setting the vision for this new era of digital transformation.

Biography: Chuck Grindstaff is executive chairman of Siemens PLM Software, a business unit of the Siemens Digital Factory Division Grindstaff first joined the company in 1978 when it was known as Unigraphics Solutions, holding a variety of R&D positions during his first decade with the organization. He subsequently left the company to serves as president and CEO of Waveframe Corp., which developed and manufactured digital signal processing systems for high-end motion picture applications. He was awarded a Scientific and Engineering Award from the Motion Picture Academy of the Arts and Sciences for his groundbreaking work and its long-term impact on the industry. Upon his return to the company in 1994, Grindstaff took over leadership of the Unigraphics product business unit before assuming a broader role as vice president of Unigraphics products and operations in 2000. In 2001, Unigraphics merged with Structural Dynamics Research Corporation (SDRC) to form the PLM business later known as UGS, which Siemens acquired and re-branded as Siemens PLM Software in 2007. In October 2010 Mr. Grindstaff was appointed president and in 2011 also assumed the role of CEO until his appointment as executive chairman in 2016.

10

SAVE POWER FROM DELIVERY TO DISPLAY

Time: 10:30am - 12:00pm || Room: 17AB || Event Type: Reviewed Presentations
Track: EDA, Embedded Systems || Topic Area: Low-Power & Reliability, SoC & Embedded System Architectures, Codesign & System Design

CHAIR:
Yiyu Shi - *Univ. of Notre Dame, IN*

CO-CHAIR:
Leonardo Piga - *Advanced Micro Devices, Inc., Austin, TX*

Power delivery and power management are substantial yet related challenges in heterogeneous computing systems. The first paper presents novel design space exploration method pertaining to power delivery. The next paper presents an approach based on control theory for dynamic power management in GPUs. The third paper tackles dynamic thermal management for 3D systems with stacked DRAMs. The last paper presents power models for novel high end low power displays.

*Indicates Best Paper Candidate

***10.1 Ivory: Early-Stage Design Space Exploration Tool for Integrated Voltage Regulator (10:30)**
An Zou - *Washington Univ., St. Louis, MO*
Jingwen Leng - *Shanghai Jiao Tong Univ., Shanghai, China*
Yazhou Zu - *Univ. of Texas at Austin, TX*
Tao Tong - *Kolmostar, Inc., Fremont, CA*
Vijay Janapa Reddi - *Univ. of Texas at Austin, TX*
David Brooks, Gu-Yeon Wei - *Harvard Univ., Cambridge, MA*
Xuan Zhang - *Washington Univ., St. Louis, MO*

10.2 Multi-Variable Dynamic Power Management for the GPU Subsystem (10:45)
Pietro Mercati - *Univ. of California, San Diego, La Jolla, CA*
Raid Ayoub, Michael Kishinevsky - *Intel Corp., Hillsboro, OR*
Eric Samson - *Intel Corp., Santa Clara, CA*
Marc Beuchat - *Intel Corp., Folsom, CA*
Francesco Paterna - *Intel Corp., Santa Clara, CA*
Tajana Simunic Rosing - *Univ. of California, San Diego, La Jolla, CA*

10.3 Adaptive Thermal Management for 3D ICs With Stacked DRAM Caches (11:00)
Dawei Li, Kaicheng Zhang, Akhil Guliani, Seda Ogrenci-Memik - *Northwestern Univ., Evanston, IL*

10.4 3 Channel Dependency-Based Power Model for Mobile AMOLED Displays (11:15)
Seongwoo Hong, Suk-Won Kim, Young-Jin Kim - *Ajou Univ., Suwon, Republic of Korea*

▶ **A Q&A poster session will immediately follow the presentations from 11:30am - 12:00pm.**

11

GO WITH THE FLOW: SECURITY ANALYSIS AND DEFENSE

Time: 10:30am - 12:00pm || Room: 18CD || Event Type: Reviewed Presentations
Track: Security || Topic Area: Digital Design

CHAIR:
Lawrence Case - *NXP Semiconductors, Austin, TX*

Information flow analysis is a broad technique for understanding how data affects and propagates through hardware. This session has four papers that utilize information flow analysis in different ways: to verify that the hardware adheres to security properties, finding rare conditions to detect potential Trojans, and modeling the effects of faults in cryptographic hardware.

11.1 Arbitrary Precision and Complexity Tradeoffs for Gate-Level Information Flow Tracking (10:30)
Andrew Becker - *École Polytechnique Fédérale de Lausanne, Switzerland*
Wei Hu - *Univ. of California, San Diego, La Jolla, CA*
Yu Tai - *Northwestern Polytechnical Univ. & Univ. of California, San Diego, Xi'an, China*
Philip Brisk - *Univ. of California, Riverside, CA*
Ryan Kastner - *Univ. of California, San Diego, La Jolla, CA*
Paolo Ienne - *École Polytechnique Fédérale de Lausanne, Switzerland*

11.2 Secure Information Flow Verification with Mutable Dependent Types (10:45)
Andrew Ferraiuolo, Weizhe Hua, Andrew C. Myers, G. Edward Suh - *Cornell Univ., Ithaca, NY*

11.3 Toggle MUX: How X-Optimism Can Lead to Malicious Hardware (11:00)
Christian Krieg, Clifford Wolf, Axel Jantsch, Tanja Zseby - *Technische Univ. Wien, Vienna, Austria*

11.4 XFC: A Framework for Exploitable Fault Characterization in Block Ciphers (11:15)
Punit Khanna, Chester D. Rebeiro, Aritra Hazra - *Indian Institute of Technology Madras, Chennai, India*

▶ **A Q&A poster session will immediately follow the presentations from 11:30am to 12:00pm.**

12

WHAT'S NEW IN THE ANALOG TOOLBOX?

Time: 10:30am - 12:00pm || Room: 19AB || Event Type: Reviewed Presentations
Track: EDA, Design || Topic Area: Analog & Mixed-signal Design, Simulation & Timing Analysis

CHAIR:
Shih-Hsu Huang - *Chung Yuan Christian Univ., Taoyuan, Taiwan*

This session is devoted to the most recent advances in CAD for analog and mixed signal (AMS) design with four exciting papers covering key aspects of the AMS design flow. The first paper deals with the use of Bayesian co-learning for the hierarchical modeling of performance in analog circuits. The second paper presents recent results on the co-simulation of distributed and lumped-parameter circuits. The third paper addresses the important issue of yield optimization in analog and SRAM circuits. Finally, the fourth paper describes a synthesis methodology for the design of analog-to-digital converters.

*Indicates Best Paper Candidate

12.1 Efficient Hierarchical Performance Modeling for Integrated Circuits via Bayesian Co-Learning (10:30)
Mohamad B. Alawieh, Fa Wang - *Carnegie Mellon Univ., Pittsburgh, PA*
Xin Li - *Duke Kunshan Univ. & Duke Univ., Suzhou, China*

12.2 Coupled Circuit/EM Simulation for Radio Frequency Circuits (10:45)
Hans-Georg Brachtendorf, Kai Bittner - *Upper Austrian Univ. of Applied Sciences, Hagenberg, Austria*
Wim Schoenmaker - *Magwel, Leuven, Belgium*
Pascal Reynier - *ACCO Semiconductor, Inc, Louveciennes, France*

***12.3 Efficient Bayesian Yield Optimization Approach for Analog and SRAM Circuits (11:00)**
Mengshuo Wang, Fan Yang, Changhao Yan, Xuan Zeng - *Fudan Univ., Shanghai, China*
Xiangdong Hu - *Shanghai High Performance Integrated Circuit Design Center, Shanghai, China*

12.4 A Scaling Compatible, Synthesis Friendly VCO-Based Delta-Sigma ADC Design and Synthesis Methodology (11:15)
Biying Xu, Shaolan Li, Nan Sun, David Z. Pan - *Univ. of Texas at Austin, TX*

▶ **A Q&A poster session will immediately follow the presentations from 11:30am - 12:00pm**

13

PATCH YOUR CAR LIKE YOUR PHONE - DESIGN FOR EXTENSIBILITY IN AUTOMOTIVE SYSTEMS

Time: 10:30am - 12:00pm || Room: 12AB || Event Type: Invited Presentations
Track: Automotive, Design || Topic Area: Embedded System Software, Codesign & System Design, General Interest

CHAIR:
Chung-Wei Lin - *Toyota InfoTechnology Center, Mountain View, CA*

ORGANIZERS:
Samarjit Chakraborty - *Technische Univ. München, Germany*
Qi Zhu - *Univ. of California, Riverside, CA*

Extensibility measures the difficulty to conduct system updates without incurring significant redesign and re-verification cost. It is a critical design objective for long-lifetime and large-volume systems such as cars, in particular with the rapid emergence of new features and the trends towards software updates. However, while the importance of extensibility is well recognized, there is a lack of design methodologies, algorithms and tools for building extensible designs and guiding design updates. This has often prohibited timely updates and greatly undermines system availability and reliability. Further, there are currently no systematic methods to evaluate multiple designs from the perspective of extensibility. The main underlying challenge is the unknown aspect of future changes or updates that need to be accounted for. In this session, experts from academia and industry in US and Europe will demonstrate the importance of extensibility for automotive systems, discuss major challenges and industry practices, and present promising solutions.

13.1 Extensibility-Driven Automotive In-Vehicle Architecture Design (10:30)
Qi Zhu, Hengyi Liang - *Univ. of California, Riverside, CA*
Licong Zhang, Debayan Roy - *Technische Univ. München, Germany*
Wenchao Li - *Boston Univ., Boston, MA*
Samarjit Chakraborty - *Technische Univ. München, Germany*

13.2 Extensibility in Automotive Security: Current Practice and Challenges (11:00)
Sandip Ray, Wen Chen, Jayanta Bhadra - *NXP Semiconductors, Austin, TX*
Mohammad Abdullah Al Faruque - *Univ. of California, Irvine, CA*

13.3 Dynamic Platforms for Uncertainty Management in Future Automotive E/E Architectures (11:30)
Philipp Mundhenk - *Audi Electronics Venture GmbH, Gaimersheim, Germany*
Ghizlane Tibba - *Robert Bosch GmbH, Stuttgart, Germany*
Licong Zhang - *Technische Univ. München, Germany*
Felix Reimann - *Audi Electronics Venture GmbH, Gaimersheim, Germany*
Debayan Roy, Samarjit Chakraborty - *Technische Univ. München, Germany*

14 LIFE AFTER CMOS?

Time: 10:30am - 12:00pm || Room: 18AB || Event Type: Invited Presentations
Track: Design, EDA || Topic Area: Emerging Architectures & Technologies

CHAIR:
Azad Naeemi - *Georgia Institute of Technology, Atlanta, GA*

ORGANIZER:
Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

In recent years, a number of exciting options for next-generation computing models and substrates have emerged. The goal of this session is to provide insights into some of the most promising possibilities in this direction. The three talks present a vision of future system design, as seen from three different Centers in the STARnet research program. The talks discuss new devices that perform computations in different and unconventional ways, and energy-efficient information processing system design based on new abstractions such as nanofunctions, as opposed to conventional switch-based computations.

14.1 A Pathway to Enable Exponential Scaling for the Beyond-CMOS Era (10:30)
Jian-Ping Wang - *Univ. of Minnesota, Minneapolis, MN*
Kaushik Roy - *Purdue Univ., W. Lafayette, IN*
Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*
X. Sharon Hu - *Univ. of Notre Dame, IN*
Supriyo Datta - *Purdue Univ., W. Lafayette, IN*
Steven Koester - *Univ. of Minnesota, Minneapolis, MN*
Caroline Ross - *Massachusetts Institute of Technology, Cambridge, MA*
Chia-Ling Chien - *Johns Hopkins Univ., Baltimore, MD*
Paul Crowell - *Univ. of Minnesota, Minneapolis, MN*
Roland K. Kawakami - *Ohio State Univ., Columbus, OH*
Chris Kim - *Univ. of Minnesota, Minneapolis, MN*
Azad Naeemi - *Georgia Institute of Technology, Atlanta, GA*
Anand Raghunathan - *Purdue Univ., West Lafayette, IN*
Michael Niemier - *Univ. of Notre Dame, IN*

14.2 In Quest of the Next Information Processing Substrate (11:00)
Suman Datta, Alan Seabaugh, Michael Niemier - *Univ. of Notre Dame, IN*
Arijit Raychowdhury - *Georgia Institute of Technology, Atlanta, GA*
Darrell Schlom, Debdeep Jena, Grace Xing - *Cornell Univ., Ithaca, NY*
H.-S. Philip Wong, Eric Pop - *Stanford Univ., Stanford, CA*
Sayeef Salahuddin - *Univ. of California, Berkeley, CA*
Sumeet Gupta - *Pennsylvania State Univ., State College, PA*
Supratik Gupta - *Univ. of Chicago, IL*

14.3 A Systems Approach to Computing in Beyond CMOS Fabrics (11:30)
Ameya Patil, **Naresh Shanbhag**, Lav Varshney - *Univ. of Illinois at Urbana-Champaign, IL*
Eric Pop - *Stanford Univ., NVIDIA, Stanford, CA*
H.-S. Philip Wong, Subhasish Mitra - *Stanford Univ., Stanford, CA*
Jan Rabaey - *Univ. of California, Berkeley, CA*
Jeffrey Weldon, Larry Pileggi - *Carnegie Mellon Univ., Pittsburgh, PA*
Sasikanth Manipatruni, Dmitri Nikonov, Ian Young - *Intel Corp., Hillsboro, OR*

15 DESIGNER TRACK PANEL: PORTABLE STIMULUS AND TESTBENCHES—ONE RING TO BIND THEM?

Time: 10:30am - 12:00pm || Room: Ballroom E || Event Type: Panel
Track: Design, EDA || Topic Area: Test & Verification, Simulation & Timing Analysis, General Interest

MODERATOR:
Kelly Larson - *Paradigm Works, Inc., Austin, TX*

ORGANIZER:
Harry Foster - *Mentor, A Siemens Business, Plano, TX*

Today's SoC verification/validation flow involves multiple verification platforms (or engines)—ranging from virtual prototyping, RTL simulation, emulation, FPGA prototyping, and even into actual post-silicon validation. Yet, historically each of these separate platforms have required their own dedicated flow involving the definition of stimulus, result checking, and coverage metrics. This has resulted in inefficiencies due to duplication. This panel of industry and EDA experts will offer differing opinions on what is needed to achieve portable stimulus and testbenches and debate if it is even possible.

PANELISTS:
Monica Farkash - *NXP Semiconductors, Austin, TX*
Mark Glasser - *NVIDIA Corporation, Santa Clara, CA*
Daniel Schostak - *ARM Ltd., Cambridge, United Kingdom*
Tom Fitzpatrick - *Mentor, A Siemens Business, Boston, MA*
Adnan Hamid - *Breker Verification Systems, Inc., San Jose, CA*

Thank You to Our Sponsor

Mentor® A Siemens Business

16

DESIGNER TRACK: ALL THINGS CLOCKING

Time: 10:30am - 12:00pm || Room: Ballroom F || Event Type: Reviewed Presentations
Track: Design, EDA || Topic Area: Physical Design & DFM, Low-Power & Reliability

CHAIR:
Michael Kazda - *IBM Corp., Poughkeepsie, NY*

This session will discuss many different aspects of clock design methodology. From wire delay estimation and better clock balancing, to OCV reduction and clock scheduling using dynamic voltage drop, clock design and build will be reviewed from many angles. Also discussed will be an air-gap-based design methodology for improved performance and a clock matrix based approach for constraint management.

16.1 Enhanced Wire Delay Estimation for Clock Tree Synthesis in Nanometer Scale Technology (10:30)
Taeil Kim, Sangdo Park - *Samsung Semiconductor, Inc., Gyeonggi-do, Republic of Korea*
Hyung-Ok Kim - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Jung Yun Choi - *Samsung Semiconductor, Inc., Gyunggi-do, Republic of Korea*

16.2 A Method to Derive Optimal Clock Balancing Constraints for Clock Tree Synthesis(10:45)
Atul Garg, Venkatraman Ramakrishnan, Muralimohan Thota - *Texas Instruments India Pvt. Ltd., Bangalore, India*

16.3 Air Gap-Aware Design Optimization for High Performance SOC with Efficient Process Cost (11:00)
Seongmin Ryu - *Samsung Electronics Co., Ltd., & Sungkyunkwan Univ., Hwaseong-si, Republic of Korea*
Hyosig Won - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Tae Hee Han - *Sungkyunkwan Univ., Suwon, Republic of Korea*

16.4 An Effective OCV Reduction Methodology for Top-Level Clock Tree Synthesis (11:15)
Yih-Chih Chou, Cheng-Hong Tsai, Chih-Mou Tseng - *Global Unichip Corp., Hsinchu, Taiwan*

16.5 Practical SDC Promotion Method- A Clock Matrix Based Approach (11:30)
Hiroshi Ishikawa - *Renesas System Design Co., Ltd., Tokyo, Japan*
Himanshu Bhatnagar - *Excellicon Inc., Laguna Hills, CA*

16.6 Clock Scheduling Technique Considering Dynamic Voltage Drop in Multi-Design Modes (11:45)
Sangdo Park, Hyung-Ock Kim - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*
Insub Shin - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

▶ **Q&A Poster Session**
Tuesday, June 20, 5:00 - 6:00pm - Exhibit Floor

Thank You to Our Sponsor

Mentor®
A Siemens Business

17

IP TRACK: UNIQUE REQUIREMENTS FACING IP PROVIDERS FOR THE AUTOMOTIVE MARKET

Time: 10:30am - 12:00pm || Room: Ballroom G || Event Type: Invited Presentations
Track: IP, Automotive || Topic Area: General Interest

CHAIR:
Warren Savage - *Silvaco, Inc., San Jose, CA*

The automotive electronics market has long been a specialized market marked with many stringent environmental and safety requirements that semiconductor companies have become adept at navigating over the years. But today, a combination of the explosion in demand for complex chips in vehicles along with semiconductor companies being increasingly reliant on third-party IP is pushing IP suppliers to become aware of the special needs of the automotive supply chain. In this session we hear from companies involved in the automotive supply chain and how they have navigated these new complexities from an IP point of view.

17.1 Automotive IP Design Challenges in the FinFet Era (10:30)
Anis Jarrar - *NXP Semiconductors, Austin, TX*

17.2 How to Solve the Conundrum of Higher Compute Performance Coupled With Integrated Functional Safety 11:00)
Neil Stroud - *ARM Ltd., Phoenix, AZ*

17.3 Architecting Safety and Performance in Automotive SoCs (11:30)
Rajesh Ramanujam - *NetSpeed Systems, Austin, TX*

Thank You to Our Sponsor

ChipEstimate.com

SKY TALK: EXPLORING THE CONNECTIONS BETWEEN THE DIGITAL WORLD AND PHYSICAL WORLD WITH SIMON SEGARS AND LUCIO LANZA

Time: 1:00 - 1:25pm || Room: DAC Pavilion || Event Type: SKY Talk
Track: IoT, Design || Topic Area: Digital Design, Analog & Mixed-signal Design, Emerging Architectures & Technologies

MODERATOR:
Ed Sperling - *Semiconductor Engineering, San Jose, CA*

DAC attendees are invited to join industry luminaries Simon Segars and Lucio Lanza in a lively, far-reaching conversation about the Internet of Things, and how the digital world will be connected with the physical world. Expect an analysis of the variety of new components required — far more than the industry is accustomed to — to support the emerging analog/mixed-signal phenomenon. They will consider how to meet these challenges, why the design ecosystem needs to be reinvented as well as why design and device costs must be reduced to meet a reasonable target. Attendees can expect to hear about new compute models and architectures, smaller processors and how an IoT infrastructure can be secured. The conversation will conclude with a few intriguing predictions on the biggest trends, along with the dreams of how to shape the IoT wave.

Biography: Simon Segars, CEO, has been at the heart of transformational change in the technology industry for 25 years. He led the development of early ARM processors for the world's first digital mobile phones and now spearheads ARM's vision for smart and connected technologies that create better social, economic, education and health prospects for all. Before being appointed CEO in July 2013, Simon held several leadership positions within ARM's engineering and business development teams. He lives in California's Silicon Valley, but spends much of his time meeting leading influencers in the world's technology hubs in the US, Europe and Asia. He serves on the Boards of the Global Semiconductor Alliance (GSA), the Electronic System Design Alliance (ESD Alliance), and as a non-executive director at Dolby Laboratories, Inc.Simon holds a number of patents in the field of embedded CPU design and earned his BEng in electronic engineering from the University of Sussex as well as an MSc in computer science from the University of Manchester.

Biography: Lucio Lanza is the Managing Director of Lanza techVentures, an early stage venture capital and investment firm, and the 2014 recipient of the Phil Kaufman Award for Distinguished Contributions to Electronic Design Automation (EDA). He currently serves as chairman of the board of PDF Solutions, Inc., a provider of technologies to improve semiconductor manufacturing yields, and is on the board of directors of several private companies. A co-founder of Radnorwood Capital, LLC., an investor in public technology companies, Dr. Lanza serves as its co-general partner and technology strategist. Previously, Dr. Lanza was a non-executive director of ARM, the world's leading semiconductor IP company, and a member of the board of directors of Harris & Harris Group. Dr. Lanza joined the venture capital industry in 1990 after executive positions at Olivetti, Intel, Daisy Systems and Cadence Design Systems. He holds a doctorate in electronic engineering from Politecnico in Milan, Italy.

SPEAKERS:
Simon Segars - *ARM Ltd., Cambridge, United Kingdom*
Lucio Lanza - *Lanza TechVentures, Palo Alto, CA*

18 FROM SMARTER CHIPS TO SMARTER BUILDINGS

Time: 1:30 - 3:00pm || Room: 17AB || Event Type: Reviewed Presentations
Track: Embedded Systems, Design || Topic Area: Low-Power & Reliability, Embedded System Software

CHAIR:
Rajesh Gupta - *Univ. of California, San Diego, CA*

CO-CHAIR:
Ayse Coskun - *Boston Univ., Boston, MA*

This session brings together techniques for optimizing the performance, energy, and reliability for cyber physical systems. The first paper aims to detect and thwart hardware trojans in pipelined MPSoCs. The second leverages optimizing compilers to reduce overhead of runtime fault recovery. The last two papers optimize energy consumption by leveraging heterogeneous multicores and by machine learning for HVAC control.

18.1 TrojanGuard: Simple and Effective Hardware Trojan Mitigation Techniques for Pipelined MPSoCs (1:30)
Amin Malekpour - *Univ. of New South Wales, Sydney, Australia*
Roshan G. Ragel - *Univ. of Peradeniya & Univ. of New South Wales, Peradeniya, Sri Lanka*
Aleksandar Ignjatovic, Sri Parameswaran - *Univ. of New South Wales, Sydney, Australia*

18.2 Leveraging Compiler Optimizations to Reduce Runtime Fault Recovery Overhead (1:45)
Fateme S. Hosseini, Pouya Fotouhi, Chengmo Yang, Guang R. Gao - *Univ. of Delaware, Newark, DE*

18.3 Energy-Aware Standby-Sparing on Heterogeneous Multicore Systems (2:00)
Abhishek Roy, Hakan Aydin - *George Mason Univ., Fairfax, VA*
Dakai Zhu - *Univ. of Texas at San Antonio, TX*

18.4 Deep Reinforcement Learning for Building HVAC Control (2:15)
Tianshu Wei - *Univ. of California, Riverside, CA*
Yanzhi Wang - *Syracuse Univ., Syracuse, NY*
Qi Zhu - *Univ. of California, Riverside, CA*

▶ **A Q&A poster session will immediately follow the presentations from 2:30 - 3:00pm.**

19

CONTROL FREAK

Time: 1:30 - 3:00pm || Room: 18CD || Event Type: Reviewed Presentations
Track: Security, Embedded Systems || Topic Area: SoC & Embedded System Architectures, Codesign & System Design

CHAIR:
Jeyavijayan Rajendran - *Univ. of Texas at Dallas, Richardson, TX*

CO-CHAIR:
Saverio Fazzari - *Booz Allen Hamilton, Inc., Clarksville, MD*

System security requires maintaining control over the execution flow of the processor, and maintaining control over critical data. The first two papers describe techniques to ensure correct control-flow using hardware support. The next paper uses machine learning to detect malware based on control flow and data dependencies at runtime. The final paper protects security-sensitive information from kernel-level drivers by leveraging a feature of the ARM architecture to support data isolation.

*Indicates Best Paper Candidate

***19.1 No-Jump-Into-Basic-Block: Enforce Basic Block CFI on the Fly for Real-World Binaries (1:30)**
Wenjian He - *Hong Kong Univ. of Science and Technology, Hong Kong*
Sanjeev Das - *Nanyang Technological Univ., Singapore*
Wei Zhang - *Hong Kong Univ. of Science and Technology, Hong Kong*
Yang Liu - *Nanyang Technological Univ., Singapore*

19.2 LO-FAT: Low-Overhead Control Flow Attestation in Hardware (1:45)
Ghada Dessouky, Shaza Zeitouni - *Technische Univ. Darmstadt, Germany*
Thomas Nyman, Andrew Paverd - *Aalto Univ., Espoo, Finland*
Lucas V. Davi - *Univ. of Duisburg-Essen, Germany*
Patrick Koeberl - *Intel Corp., Darmstadt, Germany*
N. Asokan - *Aalto Univ. & Univ. of Helsinki, Espoo, Finland*
Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*

19.3 Analyzing Hardware Based Malware Detectors (2:00)
Nisarg Patel, Avesta Sasan, Houman Homayoun - *George Mason Univ., Fairfax, VA*

19.4 Instruction-Level Data Isolation for the Kernel on ARM (2:15)
Yeongpil Cho, Donghyun Kwon, Yunheung Paek - *Seoul National Univ., Seoul, Republic of Korea*

▶ **A Q&A poster session will immediately follow the presentations from 2:30 - 3:00pm.**

20

FPGAS FOR PERFORMANCE, THROUGHPUT AND SCALABILITY

Time: 1:30 - 3:00pm || Room: 19AB || Event Type: Reviewed Presentations
Track: EDA, EDA || Topic Area: FPGA and Reconfigurable Systems

CHAIR:
Mathias Soeken - *École Polytechnique Fédérale de Lausanne, Switzerland*

CO-CHAIR:
Dinesh Bhatia - *Univ. of Texas at Dallas, TX*

FPGAs offer an appealing combination of customizability, reduced design cost and in-field programmability. This session explores advances in FPGA systems, including high-level programming frameworks based on OpenCL, synthesis of deep neural networks to FPGAs, and large-scale clustering for FPGAs.

*Indicates Best Paper Candidate

20.1 FlexCL: An Analytical Performance Model for OpenCL Workloads on Flexible FPGAs (1:30)
Shuo Wang, Yun Liang - *Peking Univ., Beijing, China*
Wei Zhang - *Hong Kong Univ. of Science and Technology, Hong Kong*

20.2 A Comprehensive Framework for Synthesizing Stencil Algorithms on FPGAs using OpenCL Model (1:45)
Shuo Wang, Yun Liang - *Peking Univ., Beijing, China*

***20.3 Automated Systolic Array Architecture Synthesis for High Throughput CNN Inference on FPGAs (2:00)**
Xuechao Wei - *Falcon Computing Solutions, Inc. & Peking Univ., Beijing, China*
Cody Hao Yu - *Falcon Computing Solutions, Inc. & Univ. of California, Los Angeles, CA*
Peng Zhang, Youxiang Chen, Yuxin Wang, Han Hu - *Falcon Computing Solutions, Inc., Los Angeles, CA*
Yun Liang - *Peking Univ., Beijing, China*
Jason Cong - *Falcon Computing Solutions, Inc. & Univ. of California, Los Angeles, CA*

20.4 LSC: A Large-Scale Consensus-Based Clustering Algorithm for High-Performance FPGAs (2:15)
Love Singhal, Mahesh A. Iyer, Saurabh Adya - *Intel Corp., San Jose, CA*

▶ **A Q&A poster session will immediately follow the presentations from 2:30 - 3:00pm.**

21 RADIOS FOR THE NEXT 50 BILLION DEVICES

Time: 1:30 - 3:00pm || Room: 12AB || Event Type: Invited Presentations
Track: Embedded Systems, Design || Topic Area: General Interest, Analog & Mixed-signal Design, SoC & Embedded System Architectures

CHAIR:
Luca Carloni - *Columbia Univ., New York, NY*

Pervasive, high bandwidth, robust wireless connectivity holds the promise of enabling the vision of ubiquitous computing. In this session, three experts in wireless systems design will shed light on the main trends and challenges in connecting the world's next tens of Billions of devices.

21.1 The IoT Node: the Wireless Superhero (1:30)
Alessandro Piovaccari, Ramin Poorfard, Alan Hendrickson - *Silicon Labs, Austin, TX*

21.2 Linear Periodically Time-Varying (LPTV) Circuits Enable New Radio Architectures for Emerging Wireless Communication Paradigms (2:00)
Negar Reiskarimian, Linxiao Zhang, **Harish Krishnaswamy** - *Columbia Univ., New York, NY*

21.3 Zero-Power Radios: Wireless Communication out of Thin Air (2:30)
Shyam Gollakota - *Univ. of Washington, Seattle, WA*

22 MODEL-BASED DESIGN OF MEDICAL DEVICES: YOUR LIFE DEPENDS ON IT!

Time: 1:30 - 3:00pm || Room: 18AB || Event Type: Invited Presentations
Track: Design, Embedded Systems || Topic Area: Test & Verification, Embedded System Software, General Interest

CHAIR:
Prabhat Mishra - *Univ. of Florida, Gainesville, FL*

ORGANIZER:
Rahul Mangharam - *Univ. of Pennsylvania, Philadelphia, PA*

Medical devices are increasingly used for monitoring and therapy of a wide range of health conditions. Designing these safety and life-critical systems is challenging due to rapidly increasing hardware and software complexity, lengthy and costly regulatory approval processes and new challenges such as malicious security attacks. This session explores model-based design as an approach to improving the turn-around time and cost of design, validation and regulatory approval for medical devices.

22.1 Challenges and Potential for Incorporating Model-Based Design in Medical Device Development (1:30)
Louis Lintereur - *Medtronic, Inc., Northridge, CA*

22.2 Model-Based Clinical Trials for Closed-Loop Medical Devices (2:00)
Rahul Mangharam, Houssam Abbas, Zhihao Jiang, Kuk Jang - *Univ. of Pennsylvania, Philadelphia, PA*
Jackson Liang, Sanjay Dixit - *Penn Medicine, Philadelphia, PA*

22.3 Modeling Design and Safety Analysis of Physiological Closed-Loop Systems (2:30)
Stephen Patek - *Univ. of Virginia, Charlottesville, VA*

23 DESIGNER TRACK: RISC-V IMPLEMENTATION CONSIDERATIONS

Time: 1:30 - 3:00pm || Room: Ballroom E || Event Type: Invited Presentations
Track: Embedded Systems, Design || Topic Area: SoC & Embedded System Architectures, Digital Design, Embedded System Software

CHAIR:
Rick O'Connor - *RISC-V Foundation, Ottawa, ON, Canada*

ORGANIZER:
Robert Oshana - *NXP Semiconductors, Austin, TX*

RISC-V (pronounced "risk-five"), an open instruction set architecture (ISA) that was originally designed at UC Berkeley to support computer architecture research and education, is an industry standard open ISA under the governance of the RISC-V Foundation. The RISC-V ISA is finding its way into applications ranging from IoT to high end servers and supercomputing. With the advent of RISC-V, which distills over 30 years of RISC processor research into an extensible instruction set that can be fully customized, hardware implementers are now able to build fully open-source based CPUs.

23.1 RISC-V ISA and Foundation Overview (1:30)
Rick O'Connor - *RISC-V Foundation, Ottawa, ON, Canada*

23.2 RISC-V - A Free and Open ISA Enabling A Diversity of Core and Accelerator Choices (1:40)
Guy Lemieux - *VectorBlox, Vancouver, BC, Canada*

23.3 RISC-V Tool Chain - An Example Implementation (2:00)
Tim Morin - *Microsemi Corp., Dallas, TX*

23.4 RISC-V OS Landscape (2:30)
Aditi Hilbert - *Runtime, Redwood City, CA*

24 DESIGNER TRACK: DESIGN CHALLENGES OF NEW PROCESSOR ARCHITECTURES

Time: 1:30 - 3:00pm || Room: Ballroom F || Event Type: Invited Presentations
Track: Design, IoT || Topic Area: Emerging Architectures & Technologies, Digital Design, SoC & Embedded System Architectures

CHAIR:
Moshe Sananes - *Intel Corp., Austin, TX*

The amount of processing in the datacenter and in mobile and other devices at the edge of the network is growing. Applications such as machine learning and IoT have added new processing requirements. But in all cases the constraints of performance, power and cost remain. In this session we look at how three different processors address these challenges.

24.1 Processor Design for Exascale Computing (1:30)
Sudhanva Gurumurthi - *Advanced Micro Devices, Inc., Austin, TX*

24.2 The Design of the KiloCore Chip (2:00)
Brent Bohnenstiehl, Aaron Stillmaker, Bevan Baas - *Univ. of California, Davis, CA*

24.3 Implementing RISC-V for IoT Applications (2:30)
Dan Ganousis - *Codasip Ltd., Campbell, CA*
Vijay Subramaniam - *Microsemi Corp., Austin, TX*

Thank You to Our Sponsor

Mentor® A Siemens Business

25 IP TRACK: SECURITY AND RELIABILITY OF IP SUBSYSTEM

Time: 1:30 - 3:00pm || Room: Ballroom G || Event Type: Reviewed Presentations
Track: IP, Design || Topic Area: SoC & Embedded System Architectures, Analog & Mixed-signal Design, FPGA and Reconfigurable Systems

CHAIR:
Karamveer Yadav - *Cadence Design Systems, Inc., Austin, TX*

The foundation of developing secure and reliable connected world IoT applications lies in selection of mixture of digital and analog IP components which includes these aspect at lowest level in the system. This session will cover the new architecture and methodologies being adopted for different IoT based IP products development and deployment. We will also explore some of the high-speed backplane communication technologies which form the foundation of connected world.

25.1 Performance Verification of an Digital PLL for use in Multi-Gigabit-Transceivers (1:30)
Tobias Markus, Markus Mueller - *Heidelberg Univ., Mannheim, Germany*
Maximilian Thuermer - *EXTOLL GmbH., Mannheim, Germany*
Stefan Kosnac - *Heidelberg Univ., Mannheim, Germany*
Mondrian Nuessle - *EXTOLL GmbH., Mannheim, Germany*
Ulrich Bruening - *Heidelberg Univ., Mannheim, Germany*

25.2 Intelligent IP - A Solution for Analog Design Automation (1:45)
Torsten Reich, Benjamin Prautsch, Uwe Eichler, Sunil Satish Rao - *Fraunhofer IIS/EAS, Dresden, Germany*

25.3 L-IOT: A Flexible Energy Efficient Platform Targeting Wide Range IoT Applications (2:00)
Edith Beigne, **Ivan Miro-Panades**, Jean-Frederic Christmann, Simone Bacles-Min, Arnaud Verdant, Gilles Sicard, Anca Molnos, Suzanne Lesecq, Damien Couroussé, Carolynn Bernier, Clément Jany, Baudouin Martineau, Dominique Morche, Anthony Quelen, Gael Pillonnet, Franck Badets - *CEA-LETI, Grenoble, France*

25.4 Accelerate IoT Device Deployment with Ready-Made, Secure IoT Subsystems (2:15)
Mike Eftimakis - *ARM Ltd., Cambridge, United Kingdom*

25.5 Redundant Execution for Performant High-Integrity Systems (2:30)
Andrew Hopkins, Chris Turner - *ARM Ltd., Cambridge, United Kingdom*

25.6 Solving the Design Challenges of the JESD204B Transport Layer Using Automation (2:45)
Vijay Nebhrajani, **Sanket S. Naik** - *SilabTech, Banglore, India*

▶ **Q&A Poster Session**
Tuesday, June 20, 5:00 - 6:00pm - Exhibit Floor

Thank You to Our Sponsor

ChipEstimate.com™

26 NEARBY ADVANCES AND FAR FRONTIERS IN VERIFICATION

Time: 3:30 - 5:30pm || Room: 17AB || Event Type: Reviewed Presentations
Track: EDA || Topic Area: Test & Verification, Emerging Architectures & Technologies

CHAIR:
Farhan Rahman - *Advanced Micro Devices, Inc., Austin, TX*

CO-CHAIR:
Shaun Feng - *Oracle Corp., Austin, TX*

This session presents new frontiers and current advances in verification. The first two papers are centered on machine learning aspects, with the first paper addressing the robustness of machine learning hardware systems, and the second leveraging machine learning to learn how engineers compose verification tests. The next two papers focus on system verification, advancing hardware-software co-verification and proposing a more effective use of coverage information. Finally, the last two papers target important aspects of verification, demonstrating advancements on automatic assertion extraction and functional timing verification.

*Indicates Best Paper Candidate

***26.1 Fault-Tolerant Training With On-Line Fault Detection for RRAM-Based Neural Computing Systems (3:30)**
Lixue Xia - *Tsinghua Univ., Beijing, China*
Mengyun Liu - *Duke Univ., Durham, NC*
Xuefei Ning - *Tsinghua Univ., Beijing, China*
Krishnendu Chakrabarty - *Duke Univ., Durham, NC*
Yu Wang - *Tsinghua Univ., Beijing, China*

26.2 Learning to Produce Direct Tests for Security Verification Using Constrained Process Discovery (3:45)
Kuo-Kai Hsieh, Li-C Wang - *Univ. of California, Santa Barbara, CA*
Wen Chen, Jayanta Bhadra - *NXP Semiconductors, Austin, TX*

26.3 Formal Techniques for Effective Co-Verification of Hardware/Software Co-Designs (4:00)
Rajdeep Mukherjee - *Univ. of Oxford, United Kingdom*
Mitra Purandare, Raphael Polig - *IBM Research - Zurich, Switzerland*
Daniel Kroening - *Univ. of Oxford, United Kingdom*

26.4 Template Aware Coverage -Taking Coverage Analysis to the Next Level (4:15)
Raviv Gal, Einat Kermany, Bilal Saleh, **Avi Ziv** - *IBM Research - Haifa, Israel*
Michael Behm, Bryan Hickerson - *IBM Corp., Austin, TX*

26.5 A-TEAM: An Automatic Template-Based Assertion Miner (4:30)
Alessandro Danese, Nicolò Dalla Riva, **Graziano Pravadelli** - *Univ. of Verona, Italy*

26.6 Path-Specific Functional Timing Verification Under Floating and Transition Modes of Operation (4:45)
Chun-Ning Lai, Jie-Hong (Roland) Jiang - *National Taiwan Univ. Taipei, Taiwan*

▶ **A Q&A poster session will immediately follow the presentations from 5:00 to 5:30pm.**

27 AGING, EFFICIENCY, AND AGING EFFICIENTLY

Time: 3:30 - 5:30pm || Room: 18CD || Event Type: Reviewed Presentations
Track: Embedded Systems || Topic Area: SoC & Embedded System Architectures

CHAIR:
Andy Pimentel - *Univ. of Amsterdam, The Netherlands*

CO-CHAIR:
Oliver Bringmann - *Univ. Tübingen, Germany*

Considering the effects of aging is rapidly becoming a primary design concern that often aligns with the need for increased efficiency. This session focuses on research that minimizes aging effects via approximation, in addition to minimizing aging effects for CGRAs via stress-aware loop mapping. The papers also address efficiency using loop extensions in dataflow modeling, approximation in low-latency adders, design-space exploration to more effectively use on-chip memory in HLS and big.LITTLE energy-saving mechanisms.

*Indicates Best Paper Candidate

27.1 Hierarchical Dataflow Modeling of Iterative Applications (3:30)
Hyesun Hong - *Seoul National Univ., Seoul, Republic of Korea*
Hyunok Oh - *Hanyang Univ., Seoul, Republic of Korea*
Soonhoi Ha - *Seoul National Univ., Seoul, Republic of Korea*

27.2 Stress-Aware Loops Mapping on CGRAs with Considering NBTI Aging Effect (3:45)
Jiangyuan Gu - *Tsinghua Univ. & Chinese Academy of Sciences, Beijing, China*
Shouyi Yin, Shaojun Wei - *Tsinghua Univ., Beijing, China*

***27.3 Towards Aging-Induced Approximations (4:00)**
Hussam Amrouch - *Karlsruhe Institute of Technology, Karlsruhe, Germany*
Behnam Khaleghi - *Sharif Univ. of Technology, Tehran, Iran*
Andreas Gerstlauer - *Univ. of Texas at Austin, TX*
Jörg Henkel - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

27.4 QuAd: Design and Analysis of Quality-Area Optimal Low-Latency Approximate Adders (4:15)
Muhammad Abdullah Hanif - *Vienna Univ. of Technology & Information Technology Univ., Wien, Austria*
Rehan Hafiz - *Information Technology Univ., Lahore, Pakistan*
Osman Hasan - *National University of Sciences and Technology, Islamabad, Pakistan*
Muhammad Shafique - *Vienna Univ. of Technology, Vienna, Austria*

27.5 Bandwidth Optimization Through On-Chip Memory Restructuring for HLS (4:30)
Jason Cong, **Peng Wei**, Cody Hao Yu, Peipei Zhou - *Univ. of California, Los Angeles, CA*

27.6 Energy-Efficient Execution for Repetitive App Usage Scenarios on big.LITTLE Architectures (4:45)
Xianfeng Li, Guikang Chen, Wen Wen - *Peking Univ., Shenzhen, China*

▶ **A Q&A poster session will immediately follow the presentations from 5:00 to 5:30pm.**

28

(ADAS)² - AUTOMOTIVE DESIGN AUTOMATION SOLUTIONS FOR AUTONOMY, DIVERSITY, ARCHITECTURE AND SAFETY

Time: 3:30 - 5:30pm || Room: 19AB || Event Type: Reviewed Presentations
Track: Automotive, Embedded Systems || Topic Area: Embedded System Software, Codesign & System Design, SoC & Embedded System Architectures

CHAIR:
Haibo Zeng - *Virginia Polytechnic Institute and State Univ., Blacksburg, VA*

CO-CHAIR:
Chung-Wei Lin - *Toyota InfoTechnology Center, Mountain View, CA*

With the imminent advent of automated and self-driving vehicles, the automotive industry relies on help from the EDA community to make these vehicles as safe and secure as possible while, at the same time, solve these challenges in a resource-efficient way.

This session includes new and exciting papers on topics delivering on this, ranging from chip level techniques over sensor safety and network optimization up to pedestrian detection and intersection management.

*Indicates Best Paper Candidate

28.1 DIMP: A Low-Cost Diversity Metric Based on Circuit Path Analysis (3:30)
Sergi Alcaide - *Barcelona Supercomputing Center & Univ. Politencia de Catalunya, Barcelona, Spain*
Carles Hernandez - *Barcelona Supercomputing Center, Barcelona, Spain*
Antoni Roca - *Univ. Politècnica de Catalunya, Spain*
Jaume Abella - *Barcelona Supercomputing Center, Barcelona, Spain*

28.2 Estimation of Safe Sensor Measurements of Autonomous System Under Attack (3:45)
Raj Gautam Dutta, Xiaolong Guo, Teng Zhang - *Univ. of Central Florida, Orlando, FL*
Kevin Kwiat, Charles Kamhoua - *Air Force Research Lab, Utica, NY*
Laurent L. Njilla - *Air Force Research Lab, Rome, NY*
Yier Jin - *Univ. of Central Florida, Orlando, FL*

28.3 Modeling the Effects of AUTOSAR Overheads on Application Timing and Schedulability (4:00)
Manish Chauhan, **Rodolfo Pellizzoni**, Krzysztof Czarnecki - *Univ. of Waterloo, ON, Canada*

28.4 Optimizing Message Routing and Scheduling in Automotive Mixed-Criticality Time-Triggered Networks (4:15)
Fedor Smirnov - *Friedrich-Alexander-Univ. Erlangen-Nürnberg, Germany*
Michael Glaß - *Univ. of Ulm, Germany*
Felix Reimann - *Audi Electronics Venture GmbH, Gaimersheim, Germany*
Jürgen Teich - *Univ. Erlangen-Nürnberg, Erlangen, Germany*

28.5 Real-Time Multi-Scale Pedestrian Detection for Driver Assistance Systems (4:30)
Maryam Hemmati, **Morteza Biglari-Abhari** - *Univ. of Auckland, New Zealand*
Smail Niar - *Univ. of Valenciennes, France*
Stevan Berber - *Univ. of Auckland, New Zealand*

***28.6 Crossroads - Time-Sensitive Autonomous Intersection Management (4:45)**
Edward P. Andert, Mohammad Khayatian - *Arizona State Univ., Tempe, AZ*
Aviral Shrivastava - *Arizona State Univ., Phoenix, AZ*

▶ **A Q&A poster session will immediately follow the presentations from 5:00 - 5:30pm**

PANEL: FROM HARD DIE TO DIE HARD: ARE HARDWARE SECURITY TECHNOLOGIES HAVING ANY IMPACT?

Time: 3:30 - 4:20pm || Room: 12AB || Event Type: Panel || Track: IoT, Security
Topic Area: SoC & Embedded System Architectures, General Interest, Codesign & System Design

MODERATOR:
Ahmad Sadeghi - *Technische Univ. Darmstadt, Germany*

Hardware security schemes are often treated as an afterthought: an extension of the system but not an inherent design metric for the whole system. This limits their adoption and benefit to real-world architectures. Emerging applications, for instance in IoT area, increasingly involve large numbers of connected and heterogeneous device swarms and pose crucial challenges on the underlying security architectures. In the recent years we have seen hardware security solutions from Trusted Platform Modules (TPM), ARM's TrustZone, to Intel's SGX, to name some have been rolled out. However, these solutions are rarely used by user applications, require strong trust assumptions in manufacturers, are too expensive for small constrained devices, and not scalable. This panel will discuss the real-world impact of currently available security hardware, the related shortcomings as well as new research and development directions in hardware-assisted security and privacy solutions.

PANELISTS:
Jean-Pierre Seifert - *Technische Univ. Berlin, Germany*
Farinaz Koushanfar - *Univ. of California, San Diego, La Jolla, CA*
Vedvyas Shanbhogue - *Intel Corp., Austin, TX*
Yousef Iskander - *Cisco Systems, Inc., Knoxville, TN*
George Kanuck - *Trustonic, San Jose, CA*
Isaac Potoczny-Jones - *Tozny LLC, Portland, OR*

31

PLACEMENT TO THE RESCUE OF EXTREME TECHNOLOGY COMPLEXITIES

Time: 3:30 - 5:30pm || Room: 18AB || Event Type: Reviewed Presentations
Track: EDA || Topic Area: Physical Design & DFM, Digital Design, General Interest

CHAIR:
Martin Wong - *Univ. of Illinois at Urbana-Champaign, IL*

Advances in technology have introduced several new constraints into the old placement problem. The devil is in the details: multiple height cells, M1 routing, fogging, pin access and useful skew have made placement challenging again. In this session, innovative techniques are introduced to solve these specific problems in placement. The session starts with a detailed placement technique for sub-10nm designs, then discusses a legalization technique for designs with multi-height cells. Pin access problem and fogging effect are discussed next. The session ends with discussion on timing driven placement.

*Indicates Best Paper Candidate

31.1 Vertical M1 Routing-Aware Detailed Placement for Congestion and Wirelength Reduction in sub-10nm Nodes (3:30)
Peter Debacker - *IMEC, Heverlee, Belgium*
Kwangsoo Han, Andrew B. Kahng, Hyein Lee - *Univ. of California, San Diego, La Jolla, CA*
Praveen Raghavan - *IMEC, Leuven, Belgium*
Lutong Wang - *Univ. of California, San Diego, La Jolla, CA*

***31.2 Toward Optimal Legalization for Mixed-Cell-Height Circuit Designs (3:45)**
Jianli Chen, Ziran Zhu, Wenxing Zhu - *Fuzhou Univ., Fuzhou, China*
Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

31.3 Fogging Effect Aware Placement in Electron Beam Lithography (4:00)
Yu-Chen Huang, **Yao-Wen Chang** - *National Taiwan Univ., Taipei, Taiwan*

31.4 Pin Accessibility-Driven Cell Layout Redesign and Placement Optimization (4:15)
Jaewoo Seo - *Korea Advanced Institute of Science and Technology & Samsung Electronics Co., Ltd., Hwaseong, Republic of Korea*
Jinwook Jung, Sangmin Kim, Youngsoo Shin - *KAIST, Daejeon, Republic of Korea*

31.5 Fast Predictive Useful Skew Methodology for Timing-Driven Placement Optimization (4:30)
Seungwon Kim, SangGi Do, Seokhyeong Kang - *Ulsan National Institute of Science and Technology (UNIST), Ulsan, Republic of Korea*

31.6 Timing Driven Incremental Multi-Bit Register Composition Using a Placement-Aware ILP Formulation (4:45)
Ioannis Seitanidis, Giorgos Dimitrakopoulos - *Democritus Univ. of Thrace, Xanthi, Greece*
Pavlos Mattheakis - *Mentor, A Siemens Business, Montbonnot-Saint-Martin, France*
Laurent H. Masse-Navette - *Mentor, A Siemens Business, Saint Ismier, France*
David Chinnery - *Mentor, A Siemens Business, Fremont, CA*

▶ **A Q&A poster session will immediately follow the presentations from 5:00 - 5:30pm**

32

DESIGNER TRACK: CHIP SECURITY: THREATS, SOLUTIONS, AND ECONOMICS

Time: 3:30 - 5:00pm || Room: Ballroom E || Event Type: Invited Presentations
Track: IoT, Security || Topic Area: SoC & Embedded System Architectures, General Interest, Codesign & System Design

CHAIR:
Saverio Fazzari - *Booz Allen Hamilton, Inc., Arlington, VA*

Security is quickly becoming a prominent design constraint in all chip segments, leading to much work in developing best practices and new technologies for its enablement. In this session, the implications of design security are explored, including modern threats and state-of-the-art solutions for today's chip designs. Additionally, the business implications of security are explored, both in terms of how new solutions can reduce the cost of implementing security, as well as how security can increase chip value

32.1 Balancing Security, Cost and Scale in IoT Security Solutions (3:30)
Asaf Ashkenazi, **Denis Pochuev** - *Rambus Security Division, San Francisco, CA*

32.2 Leveraging Security to Increase the Value of Your Chips in the Supply Chain and the Field (4:00)
Tom Katsioulas - *Mentor, A Siemens Business, Portland, OR*

32.3 Verifying Security Properties at the Hardware/Software Boundary (4:30)
Jason Oberg - *Tortuga Logic, San Diego, CA*

33 DESIGNER TRACK: PYTHON FOR DESIGN AUTOMATION

Time: 3:30 - 5:00pm || Room: Ballroom F || Event Type: Invited Presentations
Track: EDA || Topic Area: General Interest, Physical Design & DFM, Test & Verification

CHAIR:
Rajesh Gupta - *Samsung Austin R&D Center, TX*

Design methodology complexity continues to increase as design complexity increases. Python is increasingly used as the language of choice for this task as it brings object oriented design to coders while providing a simple, interactive and near-English experience for non-coders.This session will cover how to build reusable fundamental object oriented modules that represent the design structure and design methodology concepts in Python.

33.1 Using Python for Design Automation (3:30)
Tara Clark - *Intel Corp., San Jose, CA*

34 IP TRACK: MONETIZING SOFTWARE IP IN A WORLD OF HARDWARE IP

Time: 3:30 - 5:00pm || Room: Ballroom G || Event Type: Panel
Track: IP || Topic Area: General Interest

MODERATOR:
Ann Steffora Mutschler - *Semiconductor Engineering, San Jose, CA*

ORGANIZER:
Henning Spruth - *NXP Semiconductors, Austin, TX*

Software for embedded IP is often treated as an ancillary deliverable to the hardware content and not monetized on its own. Furthermore, it often is expected to be free. To the hardware IP vendor, this limits the incentives for additional software investment, to 3rd party software providers it raises the bar for entering the market. This panel discusses emerging trends and challenges of business models for embedded software IP.

PANELISTS:
Jean-Christophe Bodet - *NXP Semiconductors, Austin, TX*
Hua Xue - *Lattice Semiconductor Corp., San Jose, CA*
Scot Morrison - *Mentor, A Siemens Business, Fremont, CA*
Alex Sabatier - *NVIDIA Corporation, Austin, TX*
Dan Mender - *Green Hills Software, Inc., Santa Barbara, CA*

PANEL: COWS, COWBIRDS AND THE CONUNDRUM OF EDA RESEARCH FUNDING

Time: 4:30 - 5:20pm || Room: 12AB || Event Type: Panel || Track: EDA, Design
Topic Area: General Interest, Digital Design, Test & Verification

MODERATOR:
Andrew Kahng - *Univ. of California, San Diego, La Jolla, CA*

A perennial lament is that EDA companies don't fund academic EDA research at levels seen in other semiconductor supply chain industries. Perhaps, as the saying goes, "If you get free milk, why buy the cow?" But are EDA cows (research programs and their trained graduates) now scarcer? Starving? Migrating to greener, "DA Futures" fields? Today's graduates in EDA are hired by fewer EDA companies, who serve fewer customers, who have fewer internal EDA organizations. Research activity is a function of the number of faculty in the field, along with the amount of research funding. Research itself is slowed by limited access to tools, data, and problem formulations – while funding is limited by the years (from "DAC paper" to "production tool flow") needed to pay off the underlying investment. This panel brings together senior executives to discuss questions at the heart of these concerns: (1) Can the future bring a renaissance of EDA research funding? (2) For what kinds of research and results? (3) How must attitudes and actions change across researchers, industry, and government / consortia? (4) Who will ultimately contribute to such a renaissance, and how?

PANELISTS:
Andreas Olofsson - *Defense Advanced Research Projects Agency, Arlington, VA*
Tim Cheng - *Hong Kong Univ. of Science and Technology, Hong Kong*
Mamta Bansal - *Qualcomm Technologies, Inc., San Diego, CA*
Leon Stok - *IBM Systems and Technology Group, Yorktown Heights, NY*
Shishpal Rawat - *Council on EDA, Folsom, CA*

DESIGNER/IP TRACK POSTER SESSION

Time: 5:00 - 6:00pm || Room: Exhibit Floor || Event Type: Poster Session || Track: Design, IP || Topic Area: General Interest

During the poster presentation, you will interact directly with poster presenters in a small group setting.

As the limited time available in the Designer/IP Track session program was exceeded by the quantity of great submitted content, we present the following posters in the Design/IP Track Poster Session held Tuesday, June 20 from 5:00 to 6:00pm on the Exhibit Floor.

Thank You to Our Sponsors

Mentor® A Siemens Business

ChipEstimate.com

123.1 Netlist Reduction at Transistor Level
Ning Lu - *IBM Systems and Technology Group, Essex Junction, VT*
Richard Wachnik - *IBM Systems and Technology Group, Poughkeepsie, NY*

123.2 Validating Clamp Logic in Multi-Rail Full Custom Circuits
Jared M. Buckner - *Qualcomm Technologies, Inc., Raleigh, NC*

123.3 Thermal-Aware Statistical Electromigration Budgeting for Advanced FinFET EM Sign-Off
Qiuling Zeng, Qi Chen - *HiSilicon, Shanghai, China*
Chang Zhao - *Apache Design, Inc., A Subsidiary of ANSYS, Inc., Shanghai, China*
Kanishka De - *Apache Design, Inc., A Subsidiary of ANSYS, Inc., San Jose, CA*
Norman Chang - *ANSYS, Inc., San Jose, CA*

123.4 A Thermal-Aware Electromigration and Failure-in-Time Reliability Flow
Nitin Navale, Dawn M. Graves, Jae-Gyung Ahn - *Xilinx Inc., San Jose, CA*
Anusha Prakash - *ANSYS, Inc., San Jose, CA*

123.5 PERC Based Static Circuit Topology Checks for Robust, Reliable Low Power Implementation
Lakshmanan Balasubramanian - *Texas Instruments India Pvt. Ltd. & IEEE, Bangalor, India*
Nadeem Tehsildar - *Texas Instruments India Pvt. Ltd. & Texas Instruments, Inc., Bangalore, India*

123.6 Full Chip ESD Signoff for Multi-Domain Multi-Path Set Top Box SoC Design
Kartik Iyer - *ANSYS, Inc., Austin TX*
Shaotao Liu - *Broadcom Corp., Singapore, Singapore*
Dileesh Jostin - *ANSYS, Inc., Bangalore, India*

123.7 Advanced Power-Integrity & Reliability-Verification Methodology for Cutting-Edge AMS Designs
Ayan Roy Chowdhury, Harikrishnan K. Namboodiri - *Intel Technology India Pvt. Ltd, Bangalore, India*

123.8 Dynamic Voltage Frequency Scaling in Static Timing Analysis
Eric Foreman - *IBM Systems and Technology Group, Essex Jct, VT*
Nathan Buck - *IBM Systems and Technology Group, Underhill, VT*
Peter Elmendorf - *IBM Systems and Technology Group, Poughkeepsie, NY*
Stephen Shuma - *IBM Systems and Technology Group, Essex Jct., VT*
Michael Wood - *IBM Systems and Technology Group, Poughkeepsie, NY*

123.9 ICE-XTime Timing Analysis and SignOff with SPICE
Marc Zheng, Ruiqi Wu - *Spreadtrum, Shanghai, China*
Senhua Dong, XiaoGuang Wang, WeiWei Zhang - *Huada Empyrean Software Co., Ltd, Beijing, China*

123.10 Metal Variation Timing Methodology
Eric Foreman, Jeffrey G. Hemmet, Stephen Shuma - *IBM Systems and Technology Group, Essex Jct., VT*
David Widiger - *IBM Systems and Technology Group, Austin, TX*
Ning Lu - *IBM Systems and Technology Group, Essex Junction, VT*
Michael Wood - *IBM Systems and Technology Group, Poughkeepsie, NY*
Nate Buck - *IBM Corp., Essex Junction, VT*

123.11 Design Convergence Using Combination of VCD and Vectorless Methodologies in Low Power IP of Production SoC
Heerak Bandopadhyay - *Intel Corp., Bangalore, India*
Abhishek Nigam - *HCL Technologies,Noida, India*
Munish Chauhan - *Intel Corp., Bangalore, India*
Bharathwaj Thirumalai Ananthanpillai - *HCL Technologies,Noida, India*
Sunil Muralidharan- *Intel Corp., Bangalore, India*
Prashant Shrivastava, Dr. Satyanarayan - *HCL Technologies,Noida, India*
Subhada Mishra - *Intel Corp., Bangalore, India*

123.12 Using SDC Equivalence Check to Verify that IP Constraints are Correctly Reused in an SoC
Dinesh Kumar Tadepalli, Ming-Shuing Chen - *Intel Corp., San Jose, CA*

123.13 Impact of Dynamic Voltage Drop on Timing
Lily Aggarwal - *Microsoft Corporation, Mountain View, CA*
Anusha T. Prakash, Prabhas Kumar - *ANSYS, Inc., San Jose, CA*

123.14 High Capacity Power Signoff Using Big Data
Emmanuel Chao, Kritika Garg, Bonita Bhaskaran, Santosh Santosh - *NVIDIA Corporation, Santa Clara, CA*
Tom Taylor, Aditya Roshan, Sooyong Kim - *ANSYS, Inc., San Jose, CA*

123.15 Rapid High Coverage Multi-Scenario Flow for Power Integrity Sign-Off
Byunghyun Lee - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Sankar Ramachandran - *ANSYS, Inc. & Apache Design, Inc., A Subsidiary of ANSYS, Inc., Bangalore, India*
Anudeep Surasani - *ANSYS, Inc., Banglore, India*
Yeonsook Kim - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Sooyong Kim - *ANSYS, Inc., San Jose, CA*

123.16 Flexible Methodology Support of Customer Requirements for Timing Sign-off
Tim Helvey - *GLOBALFOUNDRIES, Rochester, MN*
Michael D. Amundson - *GLOBALFOUNDRIES, Oronoco, MN*
Ray Yock - *Cyient, East Hartford, CT*
Joe Wang - *GLOBALFOUNDRIES, Shanghai, China*
Naveen Sampath Krishna - *GLOBALFOUNDRIES, Bangalore, India*
John Dubuque - *Encore Semi Inc., Jericho, VT*

123.17 A High Quality RX SERDES IP via a Combination of Accurate SV Modelling of Analog & use of Digital Verification Flows
Gopalkrishna Nayak, Suyash Uthale, Sharath N, **Ravi Mehta** - *SilabTech, Bangalore, India*

DESIGNER/IP TRACK POSTER SESSION

123.18 Bandwidth vs Power Comsumption Tradeoffs for Coding Strategies on NoC's Links
Erwan Moréac, Pierre Bomel, Johann Laurent, André Rossi - *Univ. of South Brittany & Lab-STICC, Lorient, France*

123.19 Building FPGA's for the Cloud: Microsoft's Build System for Project Catapult
Todd Massengill, **Hari Angepat** - *Microsoft Corporation, Redmond, WA*
Andrew Putnam - *Microsoft Research, Redmond, WA*
Adrian Caulfield, Eric Chung - *Microsoft Corporation, Redmond, WA*

123.20 Application of LSF 10.1 to Improve Microprocessor Design Grid Throughput - User Case Study
David Cadigan - *IBM Corp., Poughkeepsie, NY*
Joshua Hernandez - *IBM Corp., Austin, TX*
Michael Sperling - *IBM Corp., Poughkeepsie, NY*
Andrew Scheib - *IBM Corp., Jefferson City, MO*
Marco Aurelio Stelmar Netto - *IBM Research, Sao Paulo, Brazil*
Rama Gopal Gandham - *IBM Corp., Poughkeepsie, NY*

123.21 Automating Generation of System use Cases Using Model-Based Portable Stimulus Approach
Frederik Kautz, Joerg Simon - *Cadence Design Systems, Inc., Feldkirchen, Germany*
Christian Sauer - *Cadence Design Systems, Inc., Munich / Feldkirchen, Germany*

123.22 Simple Approaches to Create Suitable Size PSTs for Static Low Power Check
JianWei Lin - *MediaTek, Inc., Hsinchu City, Taiwan*

123.23 A Universal, Transparent Connect Module Methodology for DMS and AMS Co-Simulation
Lakshmanan Balasubramanian - *Texas Instruments India Pvt. Ltd. & IEEE, Bangalore, India*
Vijay Kumar Sankaran - *Cadence Design Systems, Inc., Bangalore, India*
Nadeem Tehsildar, Bharath K. Poluri - *Texas Instruments India Pvt. Ltd. & Texas Instruments, Inc., Bangalore, India*
Qingyu Lin - *Cadence Design Systems, Inc., San Jose, CA*
Nan Zhang, Ji Du - *Cadence Design Systems, Inc., Beijing, China*

123.24 Requirement Driven Synthesis of UVM Testbench Components
Muhammad H. Khan - *OneSpin Solutions GmbH, München, Germany*
Goeran Herrmann, Matthias Sauppe - *Technical Univ. of Chemnitz, Germany*

123.25 Automatic Debug with Adaptive Fine Granularity
Daniel Hansson, Patrik Granath - *Verifyter AB, Lund, Sweden*

123.26 Automated Verification for Complex Power Management Protocols for Mixed Signal Automotive SoCs
Kushal Kamal - *GLOBALFOUNDRIES, Bengaluru, India*
Navin Bishnoi - *GLOBALFOUNDRIES, Bangalore, India*

123.27 Customizing a UVM Register Package to Support Atypical Requirements
Nancy Pratt - *INVECAS, Inc., Williston, VT*
Sai Nandikanti, Srihari Gummadilli - *INVECAS, Inc., Hyderabad, India*
Dinesh Pai - *GLOBALFOUNDRIES, Bangalore, India*

WORK-IN-PROGRESS POSTER SESSION

Time: 6:00 - 7:00pm || Room: Trinity St. Foyer
Event Type: Poster Session || Track: || Topic Area: General Interest

120.2 Automatic Fault Injection with Virtual Prototypes for Driver Robustness Testing
Kai Cong, Zhenkun Yang, Li Lei - *Intel Corp., Hillsboro, OR*
Bin Lin - *Portland State Univ., Portland, OR*
Christopher Havlicek - *Intel Corp., Hillsboro, OR*
Fei Xie - *Portland State Univ., Portland, OR*

120.3 Unified nvTCAM and sTCAM Architecture for Improving Packet Matching Performance
Xianzhong Ding, Zhiyong Zhang, Zhiping Jia, Lei Ju, **Mengying Zhao** - *Shandong Univ., Jinan, China*
Huawei Huang - *Univ. of Aizu, Fukushima-ken, Japan*

120.4 A Framework for Deep Neural Networks Exploration, Spike Transcoding and Code Generation for COTS and Dedicated Hardware IPs
Olivier Bichler, Alexandre Carbon, David Briand, Vincent Lorrain, Jean-Marc Philippe - *CEA-LIST, Gif-Sur-Yvette, France*

120.5 A Divide-and-Conquer Factoring Algorithm for Read-Once Functions
Vinicius Callegaro, Felipe S. Marranghello - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*
Mayler Martins - *Carnegie Mellon Univ., Pittsburgh, PA*
Renato P. Ribas, Andre I. Reis - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*
Marek A. Perkowski - *Portland State Univ., Portland, OR*

120.6 Fine-Grained Acceleration Control for Autonomous Intersection Management Using Deep Reinforcement Learning
Hamid Mirzaei Buini, Tony Givargis - *Univ. of California, Irvine, CA*

120.7 GRASP Based Metaheuristics for Layout Pattern Classification
Mingyu Woo, Seungwon Kim, Seokhyeong Kang - *Ulsan National Institute of Science and Technology (UNIST), Ulsan, Republic of Korea*

120.8 An Energy-Efficient Integration Methodology for Multichip Systems: A Low-Latency Wireless Interconnection Approach
Md Shahriar Shamim, Naseef Mansoor, **M Meraj Ahmed**, Mayank Dhull, Amlan Ganguly - *Rochester Institute of Technology, Rochester, NY*

120.9 Robust Area-Constrained and Edge-Constrained Clustering for Layout Pattern Classification
Yu-Min Sung, Yu-Hsiang Cheng, Sheng-Hao Wang, Chao-Yuan Huang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Oscar Chen - *AnaGlobe Technology, Inc., Hsinchu, Taiwan*
Ting-Chi Wang - *National Tsing Hua Univ., Hsinchu, Taiwan*

120.10 SURPRISE: A Probabilistic Metric of Design Space Complexity
Alric Althoff - *Univ. of California, San Diego, CA*
Ilse Tse, Ryan Kastner - *Univ. of California, San Diego, La Jolla, CA*

120.11 IR Drop Prediction of ECO-Revised Circuits Using Machine Learning
Shih-Yao Lin, Yu-Ching Li, Yen-Chun Fang, **Chien-Mo Li** - *National Taiwan Univ., Taipei, Taiwan*

120.12 Flip-Chip Routing With IO Planning Considering Practical Pad Assignment Constraints
Tao-Chun Yu, Shao-Yun Fang - *National Taiwan Univ. of Science and Technology, Taipei, Taiwan*

120.14 Implications of Distributed On-Chip Power Delivery on EM Side-Channel Attacks
Tanya Wanchoo, **Selcuk Kose**, Gokhan Mumcu - *Univ. of South Florida, Tampa, FL*

120.16 Exploiting Transactional Memory for Error Tolerance and Energy Efficiency
Dimitra Papagiannopoulou - *Brown Univ., Providence, RI*
Andrea Marongiu - *Swiss Federal Institute of Technology & Univ. di Bologna, Zurich, Switzerland*
Tali Moreshet - *Boston Univ., Boston, MA*
Maurice Herlihy, Iris Bahar - *Brown Univ., Providence, RI*

120.17 Majority-n Logic Synthesis Using Threshold Functions and LUT Networks
Eleonora Testa, Mathias Soeken - *École Polytechnique Fédérale de Lausanne, Switzerland*
Bharani Chava, Trong Huynh Bao - *IMEC & Katholieke Univ. Leuven, Belgium*
Julien Ryckaert, Kris Croes - *IMEC, Leuven, Belgium*
Francky Catthoor - *IMEC & Katholieke Univ. Leuven, Belgium*
Giovanni De Micheli - *École Polytechnique Fédérale de Lausanne, Switzerland*

120.18 FlowPaP: A Flow Pattern Predictor For STT-MRAM-Based Handheld Devices Under Read Disturbance
Hao Yan - *Univ. of Texas at San Antonio, TX*
Lei Jiang - *Indiana Univ., Bloomington, IN*
Lide Duan - *Univ. of Texas at San Antonio, TX*

120.19 CAD Methodology for Domain Crossing Immune Redundant Soft-Error Mitigated Digital Circuits
Chandarasekaran Ramamurthy, Lawrence T. Clark, Lovish Masand - *Arizona State Univ., Tempe, AZ*

120.21 Simulation Techniques for EMC Compliant Design of Automotive IC Chips and Modules
Akihiro Tsukioka, Makoto Nagata, Kohki Taniguchi, Daisuke Fujimoto - *Kobe Univ., Kobe, Japan*
Rieko Akimoto, Takao Egami - *Toshiba Corp., Kawasaki, Japan*
Kenji Niinomi - *Toshiba Microelectronics Corp., Kawasaki, Japan*
Takeshi Yuhara, Sachio Hayashi - *Toshiba Corp., Kawasaki, Japan*
Rob Mathews, Karthik Srinivasan, Ying-Shiun Li, Norman Chang - *Semiconductor BU, ANSYS Inc., San Jose, CA*

120.22 A Highly Efficient Dataflow for Sparse Convolutional Neural Networks
Bosheng Liu - *Institute of Computing Technology & Chinese Academy of Sciences, Beijing, China*
Ying Wang, Yinhe Han, Shichang Zhang - *Chinese Academy of Sciences, Beijing, China*
Xiaowei Li - *Institute of Computing Technology & Chinese Academy of Sciences, Beijing, China*

120.23 Trace Buffer Reused Based Trigger Design for Post-Silicon Debug
Yun Cheng - *Chinese Academy of Sciences, Beijing, China*
Ying Wang, Huawei Li - *Chinese Academy of Sciences & Institute of Computing Technology, Beijing, China*
Xiaowei Li - *Institute of Computing Technology & Chinese Academy of Sciences, Beijing, China*

WORK-IN-PROGRESS POSTER SESSION

120.24 Observability Probability of Timing Critical Path Aware On-Chip Performance Monitoring Methodology
Byung Su Kim - *Samsung Electronics and Sungkyunkwan Univ., Seoul, Republic of Korea*
Joon-Sung Yang - *Sungkyunkwan Univ., Suwon, Republic of Korea*
Hyo Sig Won - *Samsung Semiconductor, Inc., Yongin, Republic of Korea*

120.26 Energy Efficient Analog IC Design for Data Compression in Spiking Neuromorphic Systems
Chenyuan Zhao, Jialing Li, **Yang Yi** - *Univ. of Kansas, Lawrence, KS*

120.27 Deep Recurrent Neural Network meets MIMO-OFDM: Adaptive Transmit Symbol Detection Through Brain-Inspired Computing Architecture
Yang Yi, Lingjia Liu - *Univ. of Kansas, Lawrence, KS*

120.28 On Minimizing Write Amplification to Enhance Lifetime of Resource-Constrained Flash-Memory Storage Devices
Wei-Lin Wang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Tseng-Yi Chen - *Academia Sinica, Taipei, Taiwan*
Hsin-Wen Wei - *Tamkang Univ., Taipei, Taiwan*
Wei-Kuan Shih - *National Tsing Hua Univ., Hsinchu, Taiwan*

120.29 A Tri-Regional Hybrid Cache for Energy Reduction
Jiacong He, Joseph Callenes-Sloan - *Univ. of Texas at Dallas, Richardson, TX*

120.30 Architecting NVM in Virtualized Memory Systems
Guoliang Zhu, Kai Lu, Pengfei Zhang, Xiaoping Wang - *National Univ. of Defense Technology, ChangSha, China*
Sparsh Mittal - *Indian Institute of Technology, Hyderabad, India*

120.31 Strong PUF-Based Hardware Obfuscation
Soroush Khaleghi, Wenjing Rao - *Univ. of Illinois at Chicago, IL*

120.32 Optimization and Evaluation of Post-Silicon Trace Analysis for System-on-Chip Protocol Debug
Hao Zheng, **Yuting Cao** - *Univ. of South Florida, Tampa, FL*
Sandip Ray - *Qualcomm, Inc., Austin, TX*
Jin Yang - *Intel Corp., Hillsborough, OR*

120.33 Efficient Deployment of Structurally Pruned DNNs on Distributed Mobile Systems
Jiachen Mao, Zhongda Yang, Wei Wen, Chunpeng Wu, Linghao Song, Kent W. Nixon - *Univ. of Pittsburgh, PA*
Xiang Chen - *George Mason Univ., Fairfax, VA*
Yiran Chen - *Univ. of Pittsburgh, PA*

120.34 Detection of Layout-Level Trojans by Injecting Current into Substrate and Digitally Monitoring Built-In Sensors
Leonel Acunha Guimarães, Rodrigo Possamai Bastos, Laurent Fesquet - *TIMA Lab, CNRS/Grenoble INP/UJF, Grenoble, France*

120.35 SCBench: A Benchmark Design Suite for SystemC Verification and Validation
Bin Lin, **Fei Xie** - *Portland State Univ., Portland, OR*

120.36 Adiabatic Computing for Low Power and DPA Resistant Lightweight Cryptography for IoT Applications
Himanshu Thapliyal - *Univ. of Kentucky, Lexington, KY*
T.S.S Varun, S. Dinesh Kumar - *Univ. of Kentucky, Lexington, KY*

120.37 Energy-Efficient Implementation of an Acoustic Modem for Underwater Communication With a Model-Based Design Approach
Marcel W. Rieß, Steffen Moser, Frank Slomka, Timo Feld - *Univ. of Ulm, Germany*

120.38 Generation of Abstract Driver Models for Third-Party IP Integration Testing
Thomas Fehmel, Dominik Stoffel - *Technische Univ. Kaiserslautern, Germany*
Wolfgang Kunz - *Univ. of Kaiserslautern, Germany*

120.39 LeAF: Low-Overhead Asymmetric Frequency Control for On-Chip Interconnects
Nizar S. Dahir, **Pedro B. Campos**, Martin Trefzer, Andy M. Tyrrell, Gianluca Tempesti - *Univ. of York, United Kingdom*

120.40 A Fast and Effective Fractional Search and Lookahead Based List Scheduling Algorithm for High-Level Synthesis
Shantanu Dutt, **Ouwen Shi** - *Univ. of Illinois at Chicago, IL*

120.41 Sequential Engineering Change Order Under Retiming and Resynthesis
Nian-Ze Lee - *National Taiwan Univ., Taipei City, Taiwan*
Victor Kravets - *IBM Corp., Yorktown Heights, NY*
Jie-Hong (Roland) Jiang - *National Taiwan Univ., Taipei, Taiwan*

120.43 A Novel Approximate Ternary Multiplier for Energy-Efficient Arithmetic Designs
Yesung Kang, Jaewoo Kim, Sunmin Kim, Sunhae Shin, E-San Jang, Kyung Rok Kim, Seokhyeong Kang - *Ulsan National Institute of Science and Technology (UNIST), Ulsan, Republic of Korea*

120.44 A Binary Convolutional Neural Network on Digital ReRAM-Crossbar
Leibin Ni, Zichuan Liu, **Hao Yu** - *Nanyang Technological Univ., Singapore*

120.45 A Racetrack Memory Based In-Memory Modular Multiplication for Cryptology Application
Tao Luo - *Nanyang Technological Univ., Singapore*
Wei Zhang - *Hong Kong Univ. of Science and Technology, Hong Kong*
Bingsheng He - *National Univ. of Singapore, Singapore*
Douglas Maskell - *Nanyang Technological Univ., Singapore*

120.46 Bit-Width Reduction Scheme and Customized Register for Low Cost Convolutional Neural Network Accelerator
Kyungrak Choi, Woong Choi, Kyungho Shin, Jongsun Park - *Korea Univ., Seoul, Republic of Korea*

120.47 TACO: Thermally-Aware Chiplet Organization for 2.5D Integrated Manycore Systems
Ayse K. Coskun, Ajay Joshi - *Boston Univ., Boston, MA*
Andrew B. Kahng - *Univ. of California, San Diego, La Jolla, CA*
Yenai Ma, Saiful A. Mojumder, Tiansheng Zhang - *Boston Univ., Boston, MA*

120.48 SAT-Based Optimization for Flash-Based Digital Designs
Monther Abusultan, **Sunil Khatri** - *Texas A&M Univ., College Station, TX*

120.49 Fast Analysis on Circuit Reliability Using Signal Probabilities
Chunhong Chen, Jinchen Cai - *Univ. of Windsor, ON, Canada*

120.50 Domain-Wall Memory-Based Deep Convolutional Neural Network using Stochastic Computing
Xiaolong Ma, Yipeng Zhang, Geng Yuan, Ao Ren, Zhe Li - *Syracuse Univ., Syracuse, NY*
Jie Han - *Univ. of Alberta, Canada*
Jingtong Hu - *Oklahoma State Univ., Stillwater, OK*
Yanzhi Wang - *Syracuse Univ., Syracuse, NY*

120.51 Adaptive Power Management in Solar Energy Harvesting Sensor Node Using Reinforcement Learning
Shaswot Shresthamali, Masaaki Kondo, Hiroshi Nakamura - *Univ. of Tokyo, Japan*

WORK-IN-PROGRESS POSTER SESSION

120.52 An Interactive Framework to Explore Design Space using Human Computation and Automated Algorithms
Satyanarayana Chivukula, Samir Koppikar, Krunalkumar Patel, Alok Pal, Kranti Sattiraju, **Gayatri Mehta** - *Univ. of North Texas, Denton, TX*

120.53 Towards Post-Quantum Secure Encryption in the IoT-World
Daniela Becker, Jorge Guajardo - *Robert Bosch GmbH, Pittsburgh, PA*
Christopher Huth - *Robert Bosch GmbH, Renningen, Germany*
Karl-Heinz Zimmermann - *Technical Univ. of Hamburg, Germany*

120.54 HEMERA: Heterogeneous Architecture for Emerging Robotic Applications
Liu Liu - *Univ. of California, Santa Barbara & PerceptIn, CA*
Shaoshan Liu, Zhe Zhang - *PerceptIn, Santa Clara, CA*
Jie Tang - *South China Univ. of Technology, Guangzhou, China*
Yuan Xie - *Univ. of California, Santa Barbara, CA*

120.55 Thermal Modeling and Design for Heat Pipe in High-End Smartphones
Hong-Wen Chiou - *Industrial Technology Research Institute & National Chiao Tung Univ., Hsinchu, Taiwan*
Yu-Min Lee - *National Chiao Tung Univ., Hsinchu, Taiwan*
Liang-Chia Cheng - *Industrial Technology Research Institute, Chutung, Hsinchu, Taiwan*
Wei-Hung Lee - *Industrial Technology Research Institute, Hsinchu, Taiwan*

120.56 In-Circuit FPGA Debugging using Parameterised Reconfigurations
Alexandra Kourfali, Dirk Stroobandt - *Ghent Univ., Gent, Belgium*

120.57 OpenSoC System Architect: An Open Toolkit for Building High Performance SoC's
David Donofrio, Farzad Fatollahi-Fard - *Lawrence Berkeley National Lab, Berkeley, CA*
John Leidel - *Tactical Computing Laboratories, McKinney, TX*
Xi Wang - *Texas Tech Univ., Lubbock, TX*

120.58 A Fast Model-Based SRAF Insertion Considering Positive and Negative Coherence
Chikaaki Kodama - *Toshiba Memory Corp., Yokohama, Japan*
Hirotaka Ichikawa - *Toshiba Microelectronics Corp., Kawasaki, Japan*
Shigeki Nojima - *Toshiba Corp., Yokohama, Japan*

120.59 Flexible Spare Core Placement for Fault-Tolerant Network-on-Chip Design
Soumya J, Phani Teja Pitchuka - *BITS Pilani, Hyderbad, India*

120.60 Hardware-assisted Efficient Long Branch Tracing for Control Flow Integrity on x86 Processors
Junmo Park, Myunghoon Yang, Yongje Lee, Jangseop Shin, Yunheung Paek - *Seoul National Univ., Seoul, Republic of Korea*

120.61 OR-Gate Based Activity-Driven Clock Tree for Low Power
Shih-Hsu Huang, Jia-Hong Jian, Chen-Hsien Lin, Xin-Jia Chen - *Chung Yuan Christian Univ., Taoyuan, Taiwan*

120.62 An Industrial OCV-Aware Top-Level Clock Tree Synthesis Methodology
Hsu-Yu Kao, Yu Lee, **Shih-Hsu Huang**, Wei-Kai Cheng - *Chung Yuan Christian Univ., Taoyuan, Taiwan*
Yih-Chih Chou - *Global Unichip Corp., Taipei, Taiwan*

120.63 Space Partitioning and 3D DRC for 3D ICs
Stefano Pettazzi - *Silvaco, Inc., St Ives, United Kingdom*
Ahmed Nejim, Andrew Plews - *Silvaco, Inc., Cambridge, United Kingdom*
Anatoli Rudenko, Andrei Karabelnikau, Siarhei Lobach - *Silvaco, Inc., Santa Clara, CA*

See More Great Content in the DAC Pavilion! Complete schedule can be found on Pages 97 - 101, Additional Meetings: See Pages 89 - 95.

KEYNOTE: ACCELERATING THE IOT

TYSON TUTTLE – *Silicon Labs, Austin, TX*

Time: 9:00 – 10:00am || Room: Ballroom A || Track: IoT
Topic Area: Emerging Architectures & Technologies, SoC & Embedded System Architectures, General Interest

The Internet of Things (IoT) has been hailed as the next frontier of innovation in which the everyday "things" in our homes, offices, cars, factories and cities connect to the Internet in ways that improve our lives and transform industries. The IoT market is poised to reach 70 billion connected devices by 2025, but several challenges remain in achieving the market's full potential. Tyson Tuttle, CEO of Silicon Labs, will explore what it will take to accelerate the promise of the IoT. In his keynote, Tyson will consider the market imperatives and engineering challenges of adding connectivity to electronic devices, including cost, ease of use, energy efficiency, interoperability, future extensibility, and security. Addressing these challenges will unleash the limitless possibilities of a more connected world.

Biography: Tyson Tuttle serves as the CEO of Silicon Labs, a leading provider of silicon, software and solutions for a smarter, more connected world. Since joining Silicon Labs in 1997, Tyson has significantly shaped the company's strategic and technological directions. He helped design Silicon Labs' first breakthrough IC product, which achieved market share leadership in PC modems, enabling the company to go public in 2000. After serving as Chief Technology Officer in 2010 and Chief Operating Officer in 2011, he became CEO in 2012. In his C-level roles, Tyson spearheaded the company's focus on the Internet of Things and drove the strategic acquisitions of Ember (the zigbee market leader), Energy Micro (the pioneer of energy-friendly microcontrollers), Bluegiga (a proven provider of Bluetooth modules and software), Micrium (the leading embedded RTOS supplier) and Zentri (a Wi-Fi innovator). Tyson has more than 25 years of semiconductor experience with industry leaders like Broadcom and Crystal Semiconductor/Cirrus Logic, holds 70 patents in RF and mixed-signal IC design, and serves on the board of the Global Semiconductor Alliance (GSA). Tyson holds a B.S. in electrical engineering from Johns Hopkins University and an M.S. in electrical engineering from UCLA.

35

HARDWARE GETS CYBERPHYSICAL

Time: 10:30am - 12:00pm || Room: 17AB || Event Type: Reviewed Presentations
Track: Embedded Systems, Design || Topic Area: Digital Design, SoC & Embedded System Architectures

CHAIR:
Mohammad Al Faruque - *Univ. of California, Irvine, CA*

This session presents four innovative hardware designs for cyber physical systems. The first two are hardware accelerators for face shape recognition and time series data mining. The third presents a novel algorithm for kinematics on GPUs, and the last paper describes hardware for multi-user detector in 5G communication.

*Indicates Best Paper Candidate

***35.1 A 700fps Optimized Coarse-to-Fine Shape Searching Based Hardware Accelerator for Face Alignment (10:30)**
Qiang Wang, Leibo Liu - *Tsinghua Univ. & Institute of Microelectronics, Beijing, China*
Wenping Zhu - *Chinese Academy of Sciences & Univ. of Chinese Academy of Sciences, Beijing, China*
Huiyu Mo, Chenchen Deng, Shaojun Wei - *Tsinghua Univ. & Institute of Microelectronics, Beijing, China*

35.2 An Efficient Memristor-Based Distance Accelerator for Time Series Data Mining on Data Centers (10:45)
Xiaowei Xu, Dewen Zeng - *Huazhong Univ. of Science & Technology, Wuhan, China*
Wenyao Xu - *SUNY Buffalo, NY*
Yiyu Shi - *Univ. of Notre Dame, IN*
Yu Hu - *Huazhong Univ. of Science & Technology, Wuhan, China*

35.3 Dadu: Accelerating Inverse Kinematics for High-DOF Robots (11:00)
Shiqi Lian, Yinhe Han, Ying Wang, Hang Xiao, Xiaowei Li, Yungang Bao, Ninghui Sun - *Institute of Computing Technology & Chinese Academy of Sciences, Beijing, China*

35.4 Towards Design and Automation of Hardware-Friendly NOMA Receiver With Iterative Multi-User Detection (11:15)
Muhammad A. Pasha, Momin A. Uppal, Muhammad Hassan Ahmed, Muhammad Aimal Rehman, Muhammad Awais Bin Altaf - *Lahore Univ. of Management Sciences, Lahore, Pakistan*

▶ **A Q&A poster session will immediately follow the presentations from 11:30am - 12:00pm**

36

LAYOUT: BEGINNING TO SEE A PATTERN HERE

Time: 10:30am - 12:00pm || Room: 18CD || Event Type: Reviewed Presentations
Track: EDA || Topic Area: Physical Design & DFM

CHAIR:
Wai-Kei Mak - *National Tsing Hua Univ., Taipei, Taiwan*

CO-CHAIR:
Haoxing Ren - *NVIDIA Corporation, Austin, TX*

Lithography layout decomposition, hotspot pattern detection are critical and indispensable processes for today's high performance chip design and manufacturing. This session presents four state-of-the-art papers on these topics. The session starts with a powerful fixed parametric tractable algorithm targeting at the layout decomposition problem. The session then presents a specialized deep neural network for hotspot pattern detection. The last part of the session consists of two improved solutions for layout pattern classification problem presented in 2016 ICCAD contest.

36.1 Fixed-Parameter Tractable Algorithms for Optimal Layout Decomposition and Beyond (10:30)
Jian Kuang - *Chinese Univ. of Hong Kong & Cadence Design Systems, Inc., Hong Kong*
Evangeline F. Y. Young - *Chinese Univ. of Hong Kong, Shatin, Hong Kong*

36.2 Layout Hotspot Detection With Feature Tensor Generation and Deep Biased Learning (10:45)
Haoyu Yang - *Chinese Univ. of Hong Kong, Shatin, Hong Kong*
Jing Su, Yi Zou - *ASML, San Jose, CA*
Bei Yu, Evangeline Young - *Chinese Univ. of Hong Kong, Shatin Hong Kong*

36.3 Minimizing Cluster Number With Clip Shifting in Hotspot Pattern Classification (11:00)
Kuan-Jung Chen, **Yu-Kai Chuang**, Bo-Yi Yu, Shao-Yun Fang - *National Taiwan Univ. of Science and Technology, Taipei, Taiwan*

36.4 iClaire: A Fast and General Layout Pattern Classification Algorithm (11:15)
Wei-Chun Chang, Iris Hui-Ru Jiang - *National Chiao Tung Univ., Hsinchu, Taiwan*
Yen-Ting Yu - *Synopsys, Inc., Chupei, Taiwan*
Wei-Fang Liu - *National Chiao Tung Univ., Hsinchu, Taiwan*

▶ **A Q&A poster session will immediately follow the presentations from 11:30am - 12:00pm**

37

GPUS MEET EMBEDDED SOFTWARE!

Time: 10:30am - 12:00pm || Room: 19AB || Event Type: Reviewed Presentations
Track: Embedded Systems || Topic Area: Embedded System Software

CHAIR:

Eugenio Villar - *Univ. of Cantabria, Santander, Spain*

GPUs are powerful computation platforms that are being increasingly used in embedded systems. The embedded context introduces new challenges such as code size and power consumption that must be addressed. This session presents advances in optimizing software for embedded GPUs. Specialized micro-benchmarking enables tuning applications for lower power consumption. Exploiting the high levels of parallelism through redundant multi-threading increases reliability. Optimizing memory efficiency pushes performance to convolutional kernels to new levels for deep learning.

*Indicates Best Paper Candidate

37.1 Compiler Techniques to Reduce the Synchronization Overhead of GPU Redundant Multithreading (10:30)
Manish Gupta - *Univ. of California, San Diego, La Jolla, CA*
Daniel Lowell - *Advanced Micro Devices, Inc., Austin, TX*
John Kalamatianos, Steven Raasch, Vilas Sridharan - *Advanced Micro Devices, Inc., Boxborough, MA*
Dean Tullsen, Rajesh Gupta - *Univ. of California, San Diego, La Jolla, CA*

37.2 Power-Aware Performance Tuning of GPU Applications Through Microbenchmarking (10:45)
Nicola Bombieri, Federico Busato - *Univ. of Verona, Italy*
Franco Fummi - *Univ. of Verona & EDALab s.r.l., Italy*

***37.3 Low-Overhead Aging-Aware Resource Management on Embedded GPUs (11:00)**
Haeseung Lee - *Univ. of California, Irvine, CA*
Muhammad Shafique - *Vienna Univ. of Technology, Vienna, Austria*
Mohammad Abdullah Al Faruque - *Univ. of California, Irvine, CA*

37.4 Optimizing Memory Efficiency for Convolution Kernels on Kepler GPUs (11:15)
Xiaoming Chen, Jianxu Chen, Danny Z. Chen, Xiaobo Sharon Hu - *Univ. of Notre Dame, IN*

▶ **A Q&A poster session will immediately follow the presentations from 11:30am - 12:00pm**

38

MAKING TIME IN CYBER-PHYSICAL SYSTEMS

Time: 10:30am - 12:00pm || Room: 12AB || Event Type: Invited Presentations
Track: IoT, Embedded Systems || Topic Area: Embedded System Software, Codesign & System Design, Test & Verification

CHAIRS:

Aviral Shrivastava - *Arizona State Univ., Phoenix, AZ*
Marc Weiss - *Qulsar Inc., San Jose, CA*

ORGANIZER:

Aviral Shrivastava - *Arizona State Univ., Phoenix, AZ*

Cyber-Physical systems tightly integrate physical and computational systems. A key challenge in distributed cyber-physical systems is establishing a common notion of time between the physical world and the computational system. Fundamental research is needed in synchronizing the clocks of distributed computing systems to a higher degree than currently possible. Even if the clocks are synchronized, designing CPS systems so that they can perform geographically distributed actions in a synchronized manner is challenging. In this special session, we will start with explaining the time-related challenges facing the design of cyber-physical systems. Then, we will go over the state-of-the-art in tools and technology to develop time-sensitive applications, and then discuss where more research is needed.

38.1 Timing Requirements of Large-Scale Distributed Cyber-Physical Systems (10:30)
Edward Griffor, Ya-Shian Li-Baboud - *National Institute of Standards and Technology, Gaithersburg, MD*

38.2 Programming With Time (11:00)
Patricia Derler - *National Instruments Corp., Berkeley, CA*

38.3 Time-Sensitive Networks and Platforms (11:30)
Kevin Stanton - *Intel Corp., Hilsboro, OR*
James Coleman - *Intel Corp., Chandler, AZ*

39

WHEN COGNITIVE SYSTEMS LEARN, WHAT'S ON THEIR FINAL EXAM?

Time: 10:30am - 12:00pm || Room: 18AB || Event Type: Invited Presentations
Track: EDA, Design || Topic Area: Test & Verification, Low-Power & Reliability, General Interest

CHAIR:
Sankar Basu - *National Science Foundation, Arlington, VA*

ORGANIZERS:
Jon Candelaria - *Semiconductor Research Corp., Durham, NC*
David Yeh - *Semiconductor Research Corp., Durham, NC*

There is no question that machine learning is a hot topic with potential to change the way humans interact with the world around them. Digital assistants have become common and applications tout the term as if it conveys magical properties. Underneath all the hype, though, lies a serious problem. With unsupervised learning just around the corner and the next leap forward needed to enable autonomous systems, what will the design community do to handle the verification, validation, and test of such systems? This session will address the current state-of-the-art and formulate the key design issues in charting a path forward towards enabling the next great advances in intelligent systems.

39.1 Engineering the Future of Cognitive Systems (10:30)
Ruchir Puri - *IBM T.J. Watson Research Center, Yorktown, NY*

39.2 Verification and Test Challenges of Unsupervised Learning Systems (10:50)
Li-C Wang - *Univ. of California, Santa Barbara, CA*

39.3 Principles for Verified AI (11:10)
Sanjit Seshia - *Univ. of California, Berkeley, CA*

39.4 Improving Patient Care Through Data -- When Accurate Models are Not Enough (11:30)
Jenna Wiens - *Univ. of Michigan, Ann Arbor, MI*

40

DESIGNER TRACK: NEW FRONTIERS IN FORMAL VERIFICATION

Time: 10:30am - 12:00pm || Room: Ballroom E || Event Type: Reviewed Presentations
Track: Design, EDA || Topic Area: Logic & High-Level Synthesis, Test & Verification, Digital Design

CHAIR:
Miroslav Velev - *Aries Design Automation, LLC, Chicago, IL*

Static and formal methods, which mathematically model and analyze a design for full coverage of the behavior space, have continued to make major leaps in usability and capacity. In this session we explore new ways to effectively leverage these technologies and enable highest quality at the earliest design stages.

40.1 Formal Verification for Analog/Mixed Signal Designs (10:30)
Sudhakar Surendran - *Texas Instruments India Pvt. Ltd. & Texas Instruments, Inc., Bangalore, India*

40.2 IP-XACT Based on Design Automation for Micro Architecture Specification (10:45)
Won-Kyung Lee, Youngsik Kim, Seonil Brian Choi - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

40.3 End-to-End Formal Verification Method for Communication IP Including S/W (11:00)
Fumitaka Fukuzawa, Satoshi Kaneko - *Renesas System Design Co., Ltd., Tokyo, Japan*

40.4 Architectural Formal Verification of Cache Coherent Protocols (11:15)
Kurt Shuler, **Chirag Gandhi** - *Arteris, Inc., Campbell, CA*
HarGovind Singh, **Deepa Sahchari** - *Oski Technology, Inc., Gurgaon, India*
Roger Sabbagh - *Oski Technology, Inc., Ottawa, ON, Canada*

40.5 Conquer Difficult C-RTL Formal Verification Problems Using Recursive Compositional Reasoning (11:30)
Jian(Jeffrey) Wang, Jia Zhu - *Advanced Micro Devices, Inc., Shanghai, China*

40.6 Handling Complexities in End-to-End Formal Verification: A Case Study (11:45)
Vishal Chadha - *Oracle Corp. & NXP Semiconductors, Austin, TX*
Ram Mantha, Ram Narayan, Rishabh Jain - *Oracle Corp. & ARM Ltd., Austin, TX*

▶ **A Q&A Poster Session**
Wednesday, June 21, 5:00 - 6:00pm - Exhibit Floor

41

DESIGNER TRACK: THE ART OF TIMING

Time: 10:30am - 12:00pm || Room: Ballroom F || Event Type: Reviewed Presentations
Track: Design, EDA || Topic Area: Simulation & Timing Analysis, Physical Design & DFM, Digital Design

CHAIR:
Navin Bishnoi - *GLOBALFOUNDRIES, Bangalore, India*

This session will focus on Timing and Timing Closure issues in large scale designs. Hierarchy manipulation for optimal timing closure will be discussed, along with back-end aware synthesis, efficient timing rule generation, and fast timing closure methods on large hierarchical designs.

41.1 SOC Chip Level Aging Timing Sign-Off in Advanced FinFet Technologies (10:30)
Yongsheng Sun - *HiSilicon, Chengdu, China*
Canhui Zhan - *HiSilicon, Shenzhen, China*
Shiva Raja - *ANSYS, Inc., Littleton, MA*
Yiwei Fu - *HiSilicon, Shenzhen, China*
Hongde Xie - *HiSilicon, Chengdu, China*
Waisum Wong - *HiSilicon, Shanghai, China*

41.2 Automated Multi-Voltage High-Speed Mixed-Signal Macro Timing for Statistical Timing Rule Generation (10:45)
Nathan Buck - *IBM Systems and Technology Group, Underhill, VT*
Eric Foreman - *IBM Systems and Technology Group, Essex Jct, VT*
Rob Allen - *IBM Corp., Williston, VT*

41.3 Back End Of Line (BEOL) - Aware Synthesis Methodology (11:00)
Jae Hoon Kim, Hyung-Ok Kim - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*
Naya Ha - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

41.4 A Fast Timing Closure Method for Large Scale Hierarchical SoC Design (11:15)
Xiang Zhu - *Huawei Technologies Co., Ltd. & HiSilicon, Shenzhen, China*
Xiao Yong - *Huada Empyrean Software Co., Ltd, Beijing, China*

41.5 Tiling : An Advanced Approach for Interchanging Hierarchies Between Logical & Physical Design (11:30)
Nikhil Murgai - *Cadence Design Systems, Inc., Bengaluru, India*
Arnab Halder - *Qualcomm India Pvt. Ltd., Bangalore, India*

41.6 Local Layout Effect Aware Implementation and Optimization for Advanced Nodes (11:45)
Naya Ha, Jae Hoon Kim, Ki-Ok Kim - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Jae-Hen Hwang - *Synopsys, Inc., Seongnam-si, Republic of Korea*
Hyung-Ock Kim - *Samsung Electronics Co., Ltd., Yongin, Republic of Korea*
Sunik Heo - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

▶ **A Q&A Poster Session**
Wednesday, June 21, 5:00-6:00pm - Exhibit Floor

Thank You to Our Sponsor

Mentor®
A Siemens Business

42

IP TRACK: SILICON IP ON THE CUTTING EDGE

Time: 10:30am - 12:00pm || Room: Ballroom G || Event Type: Invited Presentations
Track: IP, Design || Topic Area: General Interest, Analog & Mixed-signal Design

CHAIR:
Ty Garibay - *Intel Corp., Austin, TX*

In the most advanced technology nodes, 16nm and below, all designs are becoming more difficult to implement. IP vendors face the added challenge of creating products that are usable by multiple customers, each with their own design methodology, tool flow and floorplanning issues. What techniques and abstractions can help IP vendors address these challenges within a reasonable design resource budget? What role does the soft IP provider play in ensuring the their designs will work well in a customers' application? Also, as customers push harder and harder for first tapeout ramp to production for their designs, what do IP providers have to do to make this type of success more likely? How can close collaboration between Foundries, EDA vendors, IP vendors and customers accelerate the pace of design?

42.1 The Secret to Building IP at the Cutting Edge (10:30)
John Maneatis - *True Circuits, Inc., Los Altos, CA*

42.2 High-Speed Interface IP: 56G SerDes in Advanced FinFet Process Nodes (11:00)
Saman Sadr - *Rambus Inc., Toronto, ON, Canada*

42.3 An Intelligent Interconnect Fabric (11:30)
Anush Mohandass - *NetSpeed Systems, San Jose, CA*

Thank You to Our Sponsor

ChipEstimate.com

SKY TALK: POWER ELECTRONICS WITH VERTICAL GaN DEVICES

Time: 1:00 - 1:25pm || Room: DAC Pavilion || Event Type: SKY Talk
Track: Embedded Systems || Topic Area: Analog & Mixed-signal Design, Low-Power & Reliability, General Interest

ORGANIZER:
Michael 'Mac' McNamara - *Adapt-IP, Palo Alto, CA*

Electronic systems have become an indispensible part of our daily lives. All electronics devices have to convert AC (alternating current) that is available from the wall sockets into DC (direct current) to run the integrated circuits that define their functionality. This conversion is typically done by a switch mode power supply (SMPS) that was a major breakthrough in the 1980s, and has lead to the proliferation of electronics systems.

At the heart of an SMPS is a high voltage silicon power transistor. Unfortunately, silicon is not the best semiconductor for high voltage (HV) devices. Silicon based Super Junction (SJ) MOSFETs achieve up to 600V. Higher voltages in silicon are realized with Insulated Gate Bipolar Transistors (IGBTs). IGBT's switching frequency tops off at 20kHz while HV SJ MOSFETs top off at 200kHz. Switching frequency freezes the efficiency and size of any SMPS.

III-V compound semiconductors such silicon carbide (SiC) or Gallium Nitride (GaN) are much better suited for high voltage power transistors. NexGen Power Systems has demonstrated vertical GaN Junction Field Effect Transistor (JFETs). We have demonstrated vertical JFETs operating at 1200V, passing the JDEC device reliability requirements, and switching at 1MHz. These devices have extremely low Coss and Qrr. We have also demonstrated working converter systems with vertical GaN devices. Further, we have shown the breakdown voltages for these vertical devices can scale up to 4000V and they can sink up to 400A of current.

This talk will compare the NexGen Power Systems vertical GaN devices with other devices in the market and show their impact on power applications such data centers, motor drives and photovoltaic inverters.

Biography: Dinesh Ramanathan is CEO of NexGen Power Systems pioneering vertical GaN devices and their applications in Power Systems. Vertical GaN devices allow the creation of a new class of power circuits that increase efficiency, reduce cost and the size of power systems. Dr. Ramanathan was also the CEO of Avogy that was acquired by NexGen Power Systems.

Prior to Avogy, Dr. Ramanathan, was Executive Vice President of the Data Communications Division and the Programmable Systems Division at Cypress Semiconductor Corp. In these roles, he managed multiple product lines, including USB, Optical Finger Navigation, Communications and Programmable System on Chip. He grew revenue through new product development that included silicon, software and systems.

Dr. Ramanathan holds both Master's and Doctorate degrees in Information and Computer Science from the University of California at Irvine. He also holds a Bachelor's degree in Computer Science and a Master's degree in Mathematics from the Birla Institute of Technology and Science (BITS) at Pilani in India.

Dr. Ramanathan is currently on the advisory council of the School of Information and Computer Science at the University of California at Irvine. He is also on the advisory board of the

SPEAKER:
Dinesh Ramanathan - *NexGen Power Systems, Inc., Cupertino, CA*

43 METRICS MATTER - OPTIMIZING FOR PERFORMANCE

Time: 1:30 - 3:00pm || Room: 17AB || Event Type: Reviewed Presentations
Track: Design, EDA || Topic Area: Digital Design, Simulation & Timing Analysis, 3D and Advanced Packaging

CHAIR:
Zhiyu Zeng - *Cadence Design Systems, Inc., Austin, TX*

CO-CHAIR:
W. Rhett Davis - *North Carolina State Univ., Raleigh, NC*

Engineering is all about optimizing metrics: maximizing performance, minimizing cost and power, and increasing reliability. This session focuses on pushing performance from circuits to architecture: the first paper optimizes the thermal behavior of liquid-cooled 3DICs, the second minimizes the stalls in coarse grained reconfigurable architectures, the third optimizes the clock tree for predictable timing, and the fourth focuses on optimal circuits for bit reversal for FFT.

43.1 Minimizing Thermal Gradient and Pumping Power in 3D IC Liquid Cooling Network Design (1:30)
Gengjie Chen, Jian Kuang, Zhiliang Zeng, Hang Zhang, Evangeline F. Y. Young, Bei Yu - *Chinese Univ. of Hong Kong, Shatin, Hong Kong*

43.2 Minimizing Pipeline Stalls in Distributed-Controlled Coarse-Grained Reconfigurable Arrays With Triggered Instruction Issue and Execution (1:45)
Yanan Lu, Yangdong Deng, Jian Weng, **Zhaoshi Li**, Chenchen Deng - *Tsinghua Univ. & Institute of Microelectronics, Beijing, China*
Leibo Liu, Shaojun Wei - *Tsinghua Univ., Beijing, China*

43.3 A Clock Tree Optimization Framework With Predictable Timing Quality (2:00)
Rickard Ewetz - *Univ. of Central Florida, Orlando, FL*

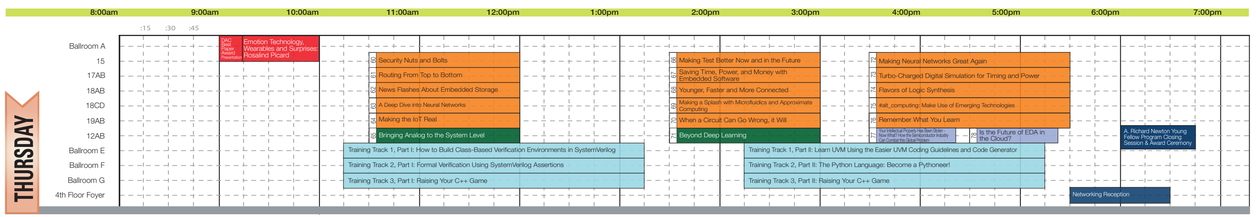
43.4 Optimal Circuits for Parallel Bit Reversal (2:15)
Ren Chen, Viktor K. Prasanna - *Univ. of Southern California, Los Angeles, CA*

▶ **A Q&A poster session will immediately follow the presentations from 2:30 - 3:00pm**

DESIGN AUTOMATION CONFERENCE

THURSDAY

Event Schedule



NETWORKING RECEPTION
Thursday, June 22 | 5:30 - 6:30pm | 4th Floor Foyer

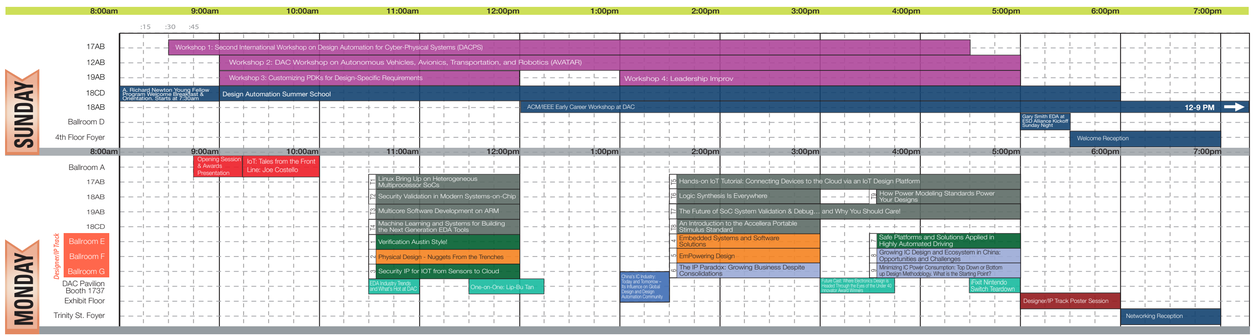
EVENT TYPES LEGEND

- Keynotes
- SKY Talks
- Reviewed Presentations
- Invited Presentations
- Panels
- DAC Pavilion
- Monday Tutorials
- Workshops
- Thursday is Training Day
- Poster Sessions
- Additional Meetings

DESIGN AUTOMATION CONFERENCE

SUNDAY/MONDAY

Event Schedule



WELCOME RECEPTION
Sunday, June 18 | 5:30 - 7:00pm | 4th Floor Foyer

NETWORKING RECEPTION
Monday, June 19 | 6:00 - 7:00pm | Trinity St. Foyer

Thank You to Our Sponsor: AMIQ

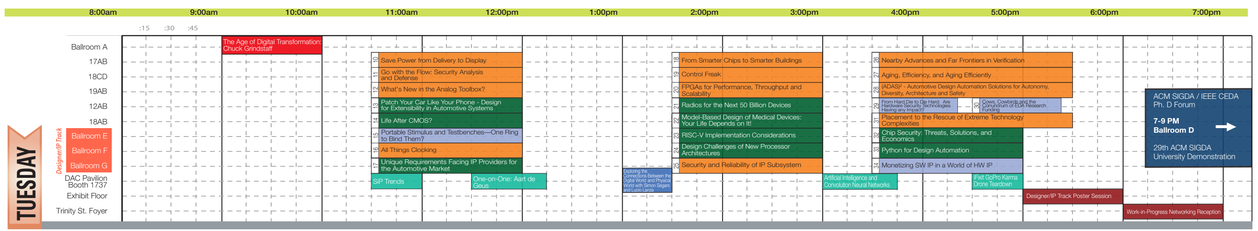
EVENT TYPES LEGEND

- Keynotes
- SKY Talks
- Reviewed Presentations
- Invited Presentations
- Panels
- DAC Pavilion
- Monday Tutorials
- Workshops
- Thursday is Training Day
- Poster Sessions
- Additional Meetings

DESIGN AUTOMATION CONFERENCE

TUESDAY

Event Schedule



WORK-IN-PROGRESS NETWORKING RECEPTION
Tuesday, June 20 | 6:00 - 7:00pm | Trinity St. Foyer

Thank You to Our Sponsor:
AMIQ

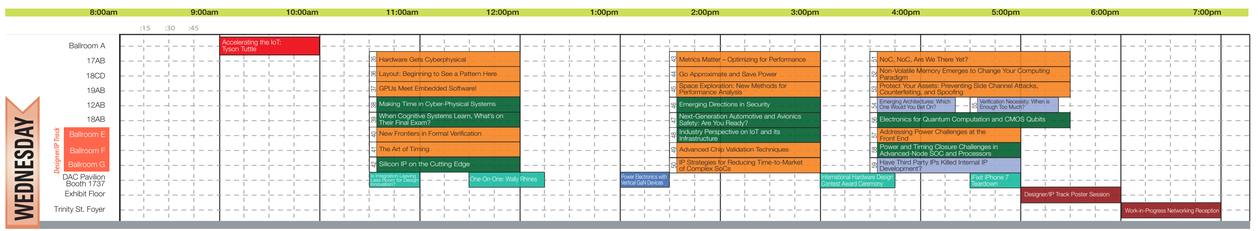
EVENT TYPES LEGEND

- Keynotes
- SKY Talks
- Reviewed Presentations
- Invited Presentations
- Panels
- DAC Pavilion
- Monday Tutorials
- Workshops
- Thursday is Training Day
- Poster Sessions
- Additional Meetings

DESIGN AUTOMATION CONFERENCE

WEDNESDAY

Event Schedule



WORK-IN-PROGRESS NETWORKING RECEPTION
Wednesday, June 21 | 6:00 - 7:00pm | Trinity St. Foyer

EVENT TYPES LEGEND

- Keynotes
- SKY Talks
- Reviewed Presentations
- Invited Presentations
- Panels
- DAC Pavilion
- Monday Tutorials
- Workshops
- Thursday is Training Day
- Poster Sessions
- Additional Meetings

44

GO APPROXIMATE AND SAVE POWER

Time: 1:30 - 3:00pm || Room: 18CD || Event Type: Reviewed Presentations
Track: EDA, Design || Topic Area: Low-Power & Reliability, Codesign & System Design, Digital Design

CHAIR:
Hadi Esmaeilzadeh - *Georgia Institute of Technology, Atlanta, GA*

Approximate computing leads to significant power efficiency at the reasonable cost of accuracy. This session presents novel approximation computing techniques from system level to circuit level. The first paper explores energy-accuracy tradeoffs of a smart camera system across different subsystems. The second paper presents a matrix based recursive approach for error analysis of multi-bit approximate adder. The third paper presents a configurable approximate floating point multiplier design that conditionally avoids parts of multiplication to save energy. The fourth paper identifies approximable and non-approximable circuits of a design.

44.1 Towards Full-System Energy-Accuracy Tradeoffs: A Case Study of An Approximate Smart Camera System (1:30)
Arnab Raha, Vijay Raghunathan - *Purdue Univ., West Lafayette, IN*

44.2 Statistical Error Analysis for Low Power Approximate Adders (1:45)
Muhammad Kamran Ayub, Osman Hasan - *National University of Sciences and Technology, Islamabad, Pakistan*
Muhammad Shafique - *Vienna Univ. of Technology, Vienna, Austria*

44.3 CFPU: Configurable Floating Point Multiplier for Energy-Efficient Computing (2:00)
Mohsen Imani, **Daniel N. Peroni**, Tajana Simunik Rosing - *Univ. of California, San Diego, La Jolla, CA*

44.4 Error Propagation Aware Timing Relaxation For Approximate Near Threshold Computing (2:15)
Anteneh Gebregiorgis, Saman Kiamehr, Mehdi B. Tahoori - *Karlsruhe Institute of Technology, Karlsruhe, Germany*

▶ **A Q&A poster session will immediately follow the presentations from 2:30 - 3:00pm**

45

SPACE EXPLORATION: NEW METHODS FOR PERFORMANCE ANALYSIS

Time: 1:30 - 3:00pm || Room: 19AB || Event Type: Reviewed Presentations
Track: EDA, Embedded Systems || Topic Area: Codesign & System Design, SoC & Embedded System Architectures

CHAIR:
Graziano Pravadelli - *Univ. of Verona, Italy*

CO-CHAIR:
Danella Zhao - *Old Dominion Univ., Norfolk, VA*

Modeling and simulation are a critical part of exploring design space. The first paper of this session improves co-design with polyhedral optimization. The next paper accelerates system simulation by vectorization. The third paper provides regression-based performance estimation, with the final paper abstracting memory accesses for confidentiality and simulation speed.

*Indicates Best Paper Candidate

45.1 Accurate High-Level Modeling and Automated Hardware/ Software Co-Design for Effective SoC Design Space Exploration (1:30)
Wei Zuo - *Univ. of Illinois at Urbana-Champaign, IL*
Louis Noel Pochet - *Colorado State Univ., Fort Collins, CO*
Andrey Ayupov, Taemin Kim - *Intel Corp., Hillsboro, OR*
Chung-Wei Lin - *Toyota InfoTechnology Center, Mountain View, CA*
Shinichi Shiraishi - *Toyota InfoTechnology Center, Minato-ku, Japan*
Deming Chen - *Univ. of Illinois at Urbana-Champaign, IL*

45.2 Exploiting Thread and Data Level Parallelism for Ultimate Parallel SystemC Simulation (1:45)
Tim Schmidt - *Univ. of California, Irvine, CA*
Guantao Liu - *Univ. of California, Irvine & Center for Embedded and Cyber-Physical Systems, CA*
Rainer Doemer - *Univ. of California, Irvine, CA*

45.3 HALWPE: Hardware-Assisted Light Weight Performance Estimation for GPUs (2:00)
Kenneth O'Neal - *Univ. of California, Riverside & Intel Corp., CA*
Emily Shriver, Michael Kishinevsky - *Intel Corp., Hillsboro, OR*
Philip Brisk - *Univ. of California, Riverside, CA*

45.4 Statistical Pattern Based Modeling of GPU Memory Access Streams (2:15)
Reena Panda, Xinnian Zheng, Jiajun Wang, Andreas Gerstlauer, Lizy K. John - *Univ. of Texas at Austin, TX*

▶ **A Q&A poster session will immediately follow the presentations from 2:30 - 3:00pm**

46

EMERGING DIRECTIONS IN SECURITY

Time: 1:30 - 3:00pm || Room: 12AB || Event Type: Invited Presentations
Track: Security, Embedded Systems || Topic Area: General Interest

CHAIR:
Siddharth Garg - *New York Univ., New York, NY*

New trends in hardware bring with them new information security threats, while opening up new avenues to design secure systems. This session explores three emerging directions in security - post-quantum security, nano-enabled security and additive manufacturing supply chain security.

46.1 Sooner Than You Think: Quantum Computing and the Reinvention of Security (1:30)
Mike Brown - *ISARA Inc., Waterloo, ON, Canada*

46.2 Security Primitive by Nanoscale Manipulation of Carbon Nanotubes (2:00)
Shu-Jen Han - *IBM T.J. Watson Research Center, Yorktown Heights, NY*

46.3 ObfusCADe: Obfuscating Additive Manufacturing CAD Models Against Counterfeiting (2:30)
Nikhil Gupta, Fei Chen, Nektarios Georgios Tsoutsos - *New York Univ., Brooklyn, NY*
Michail Maniatakos - *New York Univ., Abu Dhabi, United Arab Emirates*

47

NEXT-GENERATION AUTOMOTIVE AND AVIONICS SAFETY: ARE YOU READY?

Time: 1:30 - 3:00pm || Room: 18AB || Event Type: Invited Presentations
Track: Automotive, Embedded Systems || Topic Area: Embedded System Software, Test & Verification, General Interest

CHAIR:
Qi Zhu - *Univ. of California, Riverside, CA*

ORGANIZERS:
Haibo Zeng - *Virginia Polytechnic Institute and State Univ., Blacksburg, VA*
Huafeng Yu - *Boeing, Huntsville, AL*

Guaranteeing the safety of automotive and avionics systems is challenging. With the wave of autonomous features and rapidly evolving software in such systems (which was considered fictional only a few years ago), the big question is: Are we able to make safe autonomous systems? This special session explores the frontiers of this topic in research and industrial practice.

The first talk from a Technical Fellow at General Motors will discuss a new approach of incremental verification, which can drastically reduce the complexity of verifying evolving automotive software. The second from an industry who extensively worked in both automotive and avionics industries will focus on the safety issues and the new concept of safety guard for autonomous systems. The third will provide the experiences from safety certification in avionics, which can help nurture similar success in automotive.

47.1 Specification, Verification and Design of Evolving Automotive Software (1:30)
Ramesh S - *General Motors Research and Development, Warren, MI*
Birgit Vogel-Heuser - *Technische Univ. München, Germany*
Wanli Chang - *Singapore Institute of Technology, Singapore*
Debayan Roy, Licong Zhang, Samarjit Chakraborty - *Technische Univ. München, Germany*

47.2 Safety Guard: Runtime Enforcement for Safety-Critical Cyber-Physical Systems (2:00)
Meng Wu, Haibo Zeng - *Virginia Polytechnic Institute and State Univ., Blacksburg, VA*
Chao Wang - *Univ. of Southern California, Los Angeles, CA*
Huafeng Yu - *Boeing, Huntsville, AL*

47.3 Advanced Software V&V for Civil Aviation and Autonomy (2:30)
Guillaume Brat - *NASA, Moffett Field, CA*

48

DESIGNER TRACK: INDUSTRY PERSPECTIVE ON IOT AND ITS INFRASTRUCTURE

Time: 1:30 - 3:00pm || Room: Ballroom E || Event Type: Invited Presentations
Track: IoT, Embedded Systems || Topic Area: General Interest

CHAIR:
Jian Li - *Huawei Technologies Co., Ltd., Austin, TX*

ORGANIZER:
Jian Li - *Huawei Technologies Co., Ltd., Austin, TX*

This session covers some industrial perspectives on the infrastructure, architecture and applications of Internet of Things (IoT). Three expert speakers of both technical and business depth are invited to share their views on (1) platforms for Intelligence of Things, (2) IIoT system architecture and efforts from Industrial Internet Consortium, and (3) an all-cloud approach to IoT applications and its network nfrastructure optimization.

48.1 IIoT System Architecture Guidance from the Industrial Internet Consortium (1:30)
Brett Murphy - *RTI, Austin, TX*

48.2 An All-Cloud Approach to IoT Applications and its Network Infrastructure Optimization (2:00)
Tingqiu Tim Yuan, Cong Xu, Tao Huang - *Huawei Technologies Co., Ltd., Beijing, China*
Balint Fleischer - *Huawei Technologies Co., Ltd., Boston, MA*

48.3 Make All the Things Intelligent! (2:30)
Paul Teich - *TIRIAS Research, Austin, TX*

49

DESIGNER TRACK: ADVANCED CHIP VALIDATION TECHNIQUES

Time: 1:30 - 3:00pm || Room: Ballroom F || Event Type: Reviewed Presentations
Track: Design, EDA || Topic Area: Test & Verification, Simulation & Timing Analysis, Digital Design

CHAIR:
Kyungsu Kang - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

The complexity of design validation has continued to grow in recent years, requiring a variety of new techniques and tools. These include testing methodologies like UVM, portable stimulus, and hardware/ software co-verification; use of analytics to improve regression flows; and improvements in understanding and characterizing process-related design criteria. This session will explore several new developments in these areas.

49.1 Effectively Reduced Statistical Characterization Resource (1:30)
EunYeung Yu, Eunbyeol Kim - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

49.2 The Hidden Gems of UVM : UVM Report Catcher, UVM Heartbeat and UVM Events (1:45)
Vikas Billa - *Microsemi Corp., Hyderabad, India*

49.3 A Real Example of Accellera's Portable Stimulus Used to Verify an LTE Switch (2:00)
Adnan Hamid - *Breker Verification Systems, Inc., San Jose, CA*

49.4 Novel Approach to Hardware Software Co-Verification on Emulation (2:15)
Nimalan Siva, Ankit Anand - *Cavium, Inc., San Jose, CA*
Ayub Khan - *Mentor, A Siemens Business, Fremont, CA*

49.5 Design Tracking and Analysis for Improved Design Automation Tools (2:30)
Bill Dougherty - *IBM Corp., Pittsburgh, PA*
Michael Kazda - *IBM Corp., Poughkeepsie, NY*

49.6 Thermal Exploration and Sign-Off Analysis for Advanced 3D Integration (2:45)
Cristiano Santos - *CEA-LETI, Grenoble, France*
Pascal Vivet - *CEA-LETI & Laboratoire d'analyse et d'architecture des systèmes, Grenoble, France*
Lee Wang - *Mentor, A Siemens Business, Fremont, CA*
Alexandre Arriordaz - *Mentor, A Siemens Business, Grenoble, France*

▶ **Q&A Poster Session**
Wednesday, June 21, 5:00-6:00pm - Exhibit Floor

50 IP TRACK: IP STRATEGIES FOR REDUCING TIME-TO-MARKET OF COMPLEX SOCS

Time: 1:30 - 3:00pm || Room: Ballroom G || Event Type: Reviewed Presentations
Track: IP, Design || Topic Area: Test & Verification, Low-Power & Reliability, General Interest

CHAIR:
Paul Stravers - *Synopsys, Inc., Eindhoven, The Netherlands*

Now that the size of systems-on-chip routinely exceeds 1 billion transistors, the implied design complexity forces development teams to rethink their IP and verification strategies. With the increasing use of IP it is becoming ever more challenging to track versions, compatibility and unintended interactions among the internal and third party contributions to the IP pool. Ad-hoc verification strategies are no longer sufficient to guarantee operational silicon and the current lack of a solid methodology to handle the evolution of individual IPs in the context of the complete design only exacerbates the problem. In this session six speakers each present their view on how to solve different aspects of the IP handling and verification challenge.

50.1 "I Thought IP was Supposed to Make My Job Easier?": Adopting a Platform Based Design Methodology to Make IP Reuse and Integration Easier for SoC Design (1:30)
Michael C. Munsey - *Methodics, Inc., San Francisco, CA*
Charles McLouth - *Perforce, Alameda, CA*

50.2 PCIe TripleCheck: Boosting the Design Confidence (1:45)
Devanshu Bajaj - *Cadence Design Systems, Inc., Noida, India*

50.3 An IP Management Strategy for Accessibility, Compliance & Security of Semiconductor IP (2:00)
Dave Noble - *Consensia Inc., Dublin, CA*

50.4 Generic UVM-Based Verification Architecture for Flash Memory Controllers (2:15)
Khaled Mohamed - *Mentor, A Siemens Business, Cairo, Egypt*

50.5 A Compact Flow for Complete Register Verification (2:30)
Rajendra Prasad, Tim Blackmore - *Infineon Technologies UK Ltd., Bristol, United Kingdom*

50.6 Efficient SCE-MI Usage to Accelerate TBA Performance (2:45)
Ponnambalam Lakshmanan - *Analog Devices, Inc., Bangalore, India*

▶ **Q&A Poster Session**
Wednesday, June 21, 5:00-6:00pm - Exhibit Floor

Thank You to Our Sponsor

ChipEstimate.com

51 NOC, NOC, ARE WE THERE YET?

Time: 3:30 - 5:30pm || Room: 17AB || Event Type: Reviewed Presentations
Track: EDA || Topic Area: NoC, Chip & Package Scale Interconnect

CHAIR:
Sudeep Parischa - *Colorado State Univ., Fort Collins, CO*

CO-CHAIR:
Andreas Gerstlauer - *Univ. of Texas at Austin, TX*

This session is composed of six presentations exploring novel network-on-chip architectures, spanning emerging photonic technologies to custom architectures for data-centric applications. The presented solutions address power consumption, network latency, application specific optimizations, and integration challenges with memory hierarchy. The first two papers design low-power and resilient photonic communication fabrics. The next two papers design low-latency distance oblivious NoCs. The last two papers develop big data application-driven network architectures.

*Indicates Best Paper Candidate

51.1 Energy and Performance Trade-off in Nanophotonic Interconnects Using Coding Techniques (3:30)
Cedric Killian, Daniel Chillet - *Univ. of Rennes 1 & INRIA, Lannion, France*
Sebastien Le Beux - *École Centrale de Lyon & Lyon Institute of Nanotechnology, Lyon, France*
Dung V. Pham - *Univ. of Rennes 1 & INRIA, Lannnion, France*
Olivier Sentieys - *Univ. of Rennes 1 & INRIA, Rennes, France*
Ian D. O'Connor - *Lyon Institute of Nanotechnology & École Centrale de Lyon, Ecully, France*

51.2 MOCA: An Inter/Intra-Chip Optical Network for Memory (3:45)
Zhehui Wang - *Hong Kong Univ. of Science and Technology, Hong Kong*
Zhengbin Pang - *National Univ. of Defense Technology, Changsha, Hunan Province, China*
Peng Yang, Jiang Xu, Xuanqi Chen, Rafael K. Vivas Maeda, Zhifei Wang, Luan H.K. Duong, Haoran Li, Zhe Wang - *Hong Kong Univ. of Science and Technology, Hong Kong*

***51.3 Low-Power On-Chip Network Providing Guaranteed Services for Snoopy Coherent and Artificial Neural Network Systems (4:00)**
Bhavya K. Daya - *Massachusetts Institute of Technology & Intel Corp., Hillsboro, OR*
Li-Shiuan Peh - *Massachusetts Institute of Technology & National Univ. of Singapore, Cambridge, MA*
Anantha Chandrakasan - *Massachusetts Institute of Technology, Cambridge, MA*

51.4 Task Mapping on SMART NoC: Contention Matters, Not the Distance (4:15)
Lei Yang, Weichen Liu, Peng Chen - *Chongqing Univ., Chongqing, China*
Nan Guan - *Hong Kong Polytechnic Univ., Hong Kong*
Mengquan Li - *Chongqing Univ., Chongqing, China*

51.5 Accelerating Graph Community Detection With Approximate Updates via an Energy-Efficient NoC (4:30)
Karthi Duraisamy, Hao Lu, Partha P. Pande, Ananth Kalyanaraman - *Washington State Univ., Pullman, WA*

51.6 Network Synthesis for Database Processing Units (4:45)
Andrea Lottarini, Stephen Edwards, Kenneth A. Ross, Martha Kim - *Columbia Univ., New York, NY*

▶ **A Q&A poster session will immediately follow the presentations from 5:00 - 5:30pm**

52

NON-VOLATILE MEMORY EMERGES TO CHANGE YOUR COMPUTING PARADIGM

Time: 3:30 - 5:30pm || Room: 18CD || Event Type: Reviewed Presentations
Track: Embedded Systems || Topic Area: Emerging Architectures & Technologies

CHAIR:
Lei Jiang - *Indiana Univ., Bloomington, IN*

CO-CHAIR:
Jae Lee - *Seoul National Univ., Seoul, Republic of Korea*

Emerging non-volatile memories (NVMs) are transforming computing at all levels, from FPGA, to processors, to processing-in-memory. This session covers a wide range of novel computing paradigms. First, security and persistence issues in NVMs are addressed. Next, unique challenges of using NVMs for implementing FPGAs and processors are tackled. Lastly, efficient parallel NVM-based processing-in-memory for neural nets and data-intensive applications are explored.

*Indicates Best Paper Candidate

***52.1 Age-Aware Logic and Memory Co-Placement for RRAM-FPGAs (3:30)**
Yuan Xue, **Chengmo Yang** - *Univ. of Delaware, Newark, DE*
Jingtong Hu - *Oklahoma State Univ., Stillwater, OK*

52.2 Maximizing Forward Progress With Cache-Aware Backup for Self-powered Non-Volatile Processors (3:45)
Jing Li, **Mengying Zhao**, Lei Ju - *Shandong Univ., Jinan, China*
Chun Jason Xue - *City Univ. of Hong Kong, Hong Kong*
Zhiping Jia - *Shandong Univ., Jinan, China*

52.3 Toss-up Wear Leveling: Protecting Phase-Change Memories From Inconsistent Write Patterns (4:00)
Xian Zhang, Guangyu Sun - *Peking Univ., Beijing, China*

52.4 Exploiting Parallelism for Convolutional Connections in Processing-In-Memory Architecture (4:15)
Yi Wang, Mingxu Zhang - *Shenzhen Univ., Shenzhen, China*
Jing Yang - *Harbin Institute of Technology, Shenzhen, China*

52.5 Leave the Cache Hierarchy Operation as It Is: A New Persistent Memory Accelerating Approach (4:30)
Chun-Hao Lai - *National Taiwan Univ., Taipei, Taiwan*
Jishen Zhao - *Univ. of California, Santa Cruz, CA*
Chia-Lin Yang - *National Taiwan Univ., Taipei, Taiwan*

52.6 Ultra-Efficient Processing In-Memory for Data Intensive Applications (4:45)
Mohsen Imani, Saransh Gupta, Tajana Simunik Rosing - *Univ. of California, San Diego, La Jolla, CA*

▶ **A Q&A poster session will immediately follow the presentations from 5:00 - 5:30pm**

53

PROTECT YOUR ASSETS: PREVENTING SIDE CHANNEL ATTACKS, COUNTERFEITING, AND SPOOFING

Time: 3:30 - 5:30pm || Room: 19AB || Event Type: Reviewed Presentations
Track: Security || Topic Area: Digital Design

CHAIR:
Ujjwal Guin - *Auburn Univ., Auburn, AL*

CO-CHAIR:
Sohrab Aftabjahani - *Intel Corp., Portland, OR*

Today's hardware is subject to a myriad of attacks, ranging from information leakage through side channels, counterfeiting of valuable IP, and identity spoofing. The six papers in this session will cover new and exciting technologies to guard against these threats.

*Indicates Best Paper Candidate

53.1 RIC: Relaxed Inclusion Caches for Mitigating LLC Side-Channel Attacks (3:30)
Mehmet Kayaalp - *IBM Research, Yorktown Heights, NY*
Khaled N. Khasawneh, Hodjat Asghari Esfeden - *Univ. of California, Riverside, CA*
Jesse Elwell - *Vencore Labs, Basking Ridge, NJ*
Nael Abu-Ghazaleh - *Univ. of California, Riverside, CA*
Dmitry Ponomarev - *SUNY Binghamton, NY*
Aamer Jaleel - *NVIDIA Corporation, Westford, MA*

53.2 FFD: A Framework for Fake Flash Detection (3:45)
Zimu Guo, Xiaolin Xu, Mark Tehranipoor, Domenic Forte - *Univ. of Florida, Gainesville, FL*

53.3 Delay Locking: Security Enhancement of Logic Locking Against IC Counterfeiting and Overproduction (4:00)
Yang Xie, Ankur Srivastava - *Univ. of Maryland, College Park, MD*

***53.4 Secure and Reliable XOR Arbiter PUF Design: An Experimental Study Based on 1 Trillion Challenge Response Pair Measurements (4:15)**
Chen Zhou, Keshab K. Parhi, Chris H. Kim - *Univ. of Minnesota, Twin Cities, Minneapolis, MN*

53.5 ASSURE: Authentication Scheme for SecURE Energy Efficient Non-Volatile Memories (4:30)
Joydeep Rakshit, Kartik Mohanram - *Univ. of Pittsburgh, PA*

53.6 On Mitigation of Side-Channel Attacks in 3D ICs: Decorrelating Thermal Patterns From Power and Activity (4:45)
Johann Knechtel, Ozgur Sinanoglu - *New York Univ., Abu Dhabi, United Arab Emirates*

▶ **A Q&A poster session will immediately follow the presentations from 5:00 - 5:30pm**

54

PANEL: EMERGING ARCHITECTURES: WHICH ONE WOULD YOU BET ON?

Time: 3:30 - 4:20pm || Room: 12AB || Event Type: Panel || Track: Design, Embedded Systems || Topic Area: Emerging Architectures & Technologies, General Interest, SoC & Embedded System Architectures

MODERATOR:

An Chen - *Semiconductor Research Corp., Santa Clara, CA*

This panel will explore the following directions in emerging computing architectures.

1. Out of the various emerging architectures, which one would you bet on?
2. What are the advantages and applications of the architecture of your choice?
3. What are the limitations and challenges of the architecture of your choice?
4. Do we need technological breakthroughs to enable the architecture, e.g., new materials or devices? Is the architecture technology-agnostic or does it rely on co-optimization of architecture, devices, and even processing?
5. When do you expect the architecture to be commercialized?

PANELISTS:

Ameen Akel - *Micron Technology, Inc., Folsom, CA*
Kaushik Roy - *Purdue Univ., West Lafayette, IN*
Todd Austin - *Univ. of Michigan, Ann Arbor, MI*
Trung Tran - *Defense Advanced Research Projects Agency, Washington DC,*
Jun Sawada - *IBM Research - Almaden, CA*

56

CMOS QUBITS AND ELECTRONICS FOR QUANTUM COMPUTATION

Time: 3:30 - 5:30pm || Room: 18AB || Event Type: Invited Presentations Track: Design, EDA || Topic Area: Emerging Architectures & Technologies, General Interest, FPGA and Reconfigurable Systems

CHAIR:

Edoardo Charbon - *École Polytechnique Fédérale de Lausanne & Intel Corp., Switzerland*

ORGANIZER:

Edoardo Charbon - *École Polytechnique Fédérale de Lausanne & Intel Corp., Switzerland*

Quantum computers (QCs) hold the promise to change computing as we know it today. What is generally not discussed is the importance of classical electronics to support a QC's computational core: the qubit. In this session we look at the requirements of electronic circuits and systems supporting qubits, with a special interest for scalability issues and CMOS compatibility of quantum-classical computing systems. World experts in the field will present their work and their vision for the possibly integrated QC of the future, often reflecting on architectural and design issues, with a keen interest in the design automation capabilities sought by QC architects.

56.1 Towards Millions of Qubits (3:30)

Hendrik Bluhm - *RWTH Aachen Univ., Aachen, Germany*
Lotte Geck, Andre Kruth, Stefan van Waasen - *Forschungszentrum Jülich, Germany*
Joachim Knoch - *RWTH Aachen Univ., Aachen, Germany*

56.2 SOI Platform for Silicon Quantum Bits and Their Control Hardware (4:00)

Silvano De Franceschi - *CEA, Grenoble, France*

56.3 Cryo-CMOS Electronic Control for Scalable Quantum Computing (4:30)

Fabio Sebastiano, Harald Homulle, Bishnu Patra, Rosario Incandela, Jeroen van Dijk, Lin Song - *Delft Univ. of Technology & Tsinghua Univ., Delft, the Netherlands*
Masoud Babaie - *Delft Univ. of Technology, Delft, The Netherlands*
Andrei Vladimirescu - *Delft Univ. of Technology & Univ. of California, Berkeley, CA*
Edoardo Charbon - *École Polytechnique Fédérale de Lausanne & Intel Corp., Switzerland*

56.4 Quantum Computing: The Industrial Perspective (5:00)

Jeanette Roberts, James Clarke - *Intel Corp., Hillsboro, OR*

57

DESIGNER TRACK: ADDRESSING POWER CHALLENGES AT THE FRONT END

Time: 3:30 - 5:00pm || Room: Ballroom E || Event Type: Reviewed Presentations
Track: Design, EDA || Topic Area: Low-Power & Reliability, Logic & High-Level Synthesis, Digital Design

CHAIR:
Monica Farkash - *NXP Semiconductors, Austin, TX*

In this era of exploding cell phones, it is more critical than ever to consider power issues from the very beginning of the design and validation process. This session will explore a variety of approaches for proactively handling power-related challenges at the front end.

57.1 Methodology for Automatic Extracting Macro I/O Related Power (3:30)
Ya-Chien Ho, Shang-Wei Tu, YuJuei Chen - *MediaTek, Inc., Hsinchu, Taiwan*
Wen-Chi Feng - *Synopsys, Inc., San Jose, CA*

57.2 Application SW Modeling and Simulation Platform for System-Level Power Optimization (3:45)
Eunju Hwang - *Samsung Electronics Co., Ltd., Hwaseong, Republic of Korea*
Wook Kim - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Jung Yun Choi - *Samsung Electronics Co., Ltd., Yong-in, Republic of Korea*
Insub Shin - *Samsung Electronics Co., Ltd., Hwaseong, Republic of Korea*

57.3 Techniques for Efficient RTL Clock and Memory Gating Takedown of Next Generation High-Performance Microprocessor Designs (4:00)
Arun Joseph, Spandana R, Rahul Rao, **Shashidhar Reddy** - *IBM Systems Group, Bangalore, India*

57.4 A Novel ECO Solution for Sequential Clock Gating Based Low Power Design Flow (4:15)
Mahima Jain - *Mentor, A Siemens Business & Calypto Design Systems, Inc., Noida, India*
Jianfeng Liu - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Abhishek Mittal, Mohit Kumar, Divya Parihar - *Mentor, A Siemens Business & Calypto Design Systems, Inc., Noida, India*
Minyoung Mo, Dongkwan Han, Jung Yun Choi - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

57.5 Power Estimation Acceleration Based on Distributed Emulation (4:30)
Hyundon Kim, Seonil Brian Choi - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*
Jay Seo - *Synopsys, Inc., Seongnam-si, Republic of Korea*
Byeong Min - *Synopsys, Inc., SungNamSi, Republic of Korea*
Won-Kyung - *Samsung Electronics Co., Ltd., Hwaseong-si, Republic of Korea*

57.6 Smart Recipe for Quick Bug Hunting: Low Power Assertions (4:45)
Deepmala Sachan, Jeevan Gr - *Intel Technology India Pvt. Ltd, Bangalore, India*
Thameem Syed S - *Intel Technology India Pvt. Ltd & 3Plus1 Technology, Inc., Bangalore, India*
Ganesh B P, Raghu N Chilukuri - *Intel Technology India Pvt. Ltd, Bangalore, India*

▶ **Q&A Poster Session**
Wednesday, June 21, 5:00-6:00pm - Exhibit Hall

Thank You to Our Sponsor

Mentor®
A Siemens Business

58

DESIGNER TRACK: POWER AND TIMING CLOSURE CHALLENGES IN ADVANCED-NODE SOC AND PROCESSORS

Time: 3:30 - 5:00pm || Room: Ballroom F || Event Type: Invited Presentations
Track: EDA, Design || Topic Area: Physical Design & DFM, Low-Power & Reliability, Digital Design

CHAIR:
Shane Stelmach - *Texas Instruments, Inc., Dallas, TX*

With increasing complexity of electrical (timing and power) signoff for sub-10nm nodes, final electrical closure has become increasingly arduous and occupies significant portion of the total design cycle. Designers are addressing these challenges with more complex analysis techniques to reduce design margins, and highly tuned implementation and ECO methodologies to ensure design convergence and last-mile closure. The speakers in this session are analysis and closure experts in leading-edge SOC and processor design team. They will describe approaches for margin reduction in power and timing signoff, and best practices in implementation and ECO to ensure smooth design convergence.

58.1 The Last Mile of SOC Timing Closure (3:30)
Wei Shi - *Qualcomm, Inc., San Diego, CA*

58.2 How to Remove the Pessimistic Margin for Power Signoff (4:00)
Xuewei Huang - *HiSilicon, Shanghai, China*

58.3 Power Integrity Signoff & Mitigation for High Speed Multi-Cores Processor (4:30)
Lee-Kee Yong - *MediaTek, Inc., Austin, TX*

Thank You to Our Sponsor

Mentor®
A Siemens Business

59

IP TRACK: HAVE THIRD PARTY IPS KILLED INTERNAL IP DEVELOPMENT?

Time: 3:30 - 5:00pm || Room: Ballroom G || Event Type: Panel
Track: IP, Design || Topic Area: SoC & Embedded System Architectures, FPGA and Reconfigurable Systems, General Interest

MODERATOR:

Ann Steffora Mutschler - *Semiconductor Engineering, San Jose, CA*

ORGANIZER:

Simon Rance - *ARM Ltd., Dallas, TX*

This panel will discuss the pros and cons of using third party IPs and their impact on the development of internal IPs. It will aim to address questions such as the following. If silicon proven third party IPs are available at a reasonable cost, does it make economic sense for semiconductor companies to create and manage their own IPs? Will the complex licensing schemes of third party IPs prove to be an increased liability for design companies? Will internal IP development be restricted to only non-standard custom IPs specific to their own internal needs?

PANELISTS:

Rich Wawrzyniak - *Semico Research Corp., Green Bay, WI*
Philippe Quinio - *STMicroelectronics, Geneva, Switzerland*
Ranjit Adhikary - *ClioSoft, Inc., Fremont, CA*
Daniel Cooley - *Silicon Labs, Austin, TX*
Andy Hawkins - *Cypress Semiconductor Corporation, CA*

Thank You to Our Sponsor

ChipEstimate.com

PANEL: VERIFICATION NECESSITY: WHEN IS ENOUGH TOO MUCH?

Time: 4:30 - 5:20pm || Room: 12AB || Event Type: Panel || Track: EDA, Embedded Systems || Topic Area: Test & Verification, General Interest, SoC & Embedded System Architectures

MODERATOR:

Brian Bailey - *Semiconductor Engineering, Oceanside, OR*

ORGANIZER:

Nanette Collins - *Nanette V. Collins Marketing & PR, Boston, MA*
Harry Foster - *Mentor, A Siemens Company, Plano, TX*

One contributing factor to growing verification complexity is the emergence of new layers of verification requirements that did not exist years ago that are driving the need for new solutions and expertise. Given a complex SoC project's constraints (i.e., finite resources, finite time, and finite budget) the question remains: How do you construct an efficient, effective, and productive verification flow? When is a proposed verification solution a necessity or nicety?

PANELISTS:

David Lacey - *Hewlett Packard Enterprise, Fort Collins, CO*
Ashish Darbari - *OneSpin Solutions GmbH, Munich, Germany*
Lauro Rizzatti - *Rizzatti LLC, Portland, OR*
Mike Bartley - *Test and Verification Solutions, Bristol, United Kingdom*
Amol Bhinge - *NXP Semiconductors, Austin, TX*

DESIGNER/IP TRACK POSTER SESSION

Time: 5:00 - 6:00pm || Room: Exhibit Floor || Event Type: Poster Session
Track: Design, IP || Topic Area: General Interest

During the poster presentation, you will interact directly with poster presenters in a small group setting.

As the limited time available in the Designer/IP Track session program was exceeded by the quantity of great submitted content, we present the following posters in the Design/IP Track Poster Session held Wednesday, June 21 from 5:00 to 6:00pm on the Exhibit Floor.

Thank You to Our Sponsors

Mentor® A Siemens Business

ChipEstimate.com™

124.1 SW-HW Visual Analysis
Monica Farkash - *NXP Semiconductors, Austin, TX*
Kuo-Kai Hsieh - *Univ. of California, Santa Barbara, CA*
Wen Chen - *NXP Semiconductors, Austin, TX*

124.2 Simulator Agnostic Techniques to Overcome Eternal Conflict of Simulation Speed Against Accuracy in System Level AMS Co-Simulation
Lakshmanan Balasubramanian - *Texas Instruments India Pvt. Ltd. & IEEE, Bangalore, India*
Nadeem Tehsildar - *Texas Instruments India Pvt. Ltd. & Texas Instruments, Inc., Bangalore, India*
Ramu Narthu - *Mirafra Technologies, Bengaluru, India*
Arnab Das - *Univ. of Utah, Salt Lake City, UT*
Venkatseema Das - *Texas Instruments India Pvt. Ltd., Bengaluru, India*
Zoran Koprivica, Srdjan Pjano - *Elsys Eastern Europe d.o.o. & Texas Instruments, Inc., Belgrade, Serbia*
Bharath K. Poluri - *Texas Instruments India Pvt. Ltd. & Texas Instruments, Inc., Bangalore, India*
Ramakrishna K. Reddy - *Texas Instruments India Pvt. Ltd. & Texas Instruments, Inc., Bengaluru, India*
Vijay Kumar Sankaran - *Cadence Design Systems, Inc., Bangalore, India*
Prashant M. Admane - *Tessolve Semiconductor Pvt. Ltd., Bengaluru, India*

124.3 Using Portable Stimulus to Verify a Low Power SoC Design
Kathy Zhang - *Avago Technologies, San Jose, CA*

124.4 SoC Netlist Clock Domain Crossing Verification with Abstract Model Approach
Siva K. Pinjala, Abhijeet Kumar - *Broadcom Corp., Bengaluru, India*
Anup Kumar Gupta - *Synopsys India Pvt. Ltd., Bengaluru, India*
Kaustubh K. Joshi - *Broadcom Corp. & I2R-BYD Joint Lab, Bengaluru, India*
Jay Dutt - *Synopsys, Inc., Plano, TX*

124.5 GPU Data-Path Formal Verification Using Hector
Puneet Anand, Rushi Mehta - *Qualcomm Technologies, Inc., San Diego, CA*

124.6 Formal Connectivity Checking Coverage Metrics
Anders Nordstrom - *Synopsys, Inc., Ottawa, ON, Canada*

124.7 Achieving ROI Through an Automated Hybrid Approach to Timing Exception Verification
Kaowen Liu - *MediaTek, Inc., San Jose, CA*
Ajay Daga - *FishTail Design Automation, Lake Oswego, OR*

124.8 Comprehensive I/O Library Quality Sign-Off Flow
Jason Chen - *Semiconductor Manufacturing International Corp., Shanghai, China*
Allen Mo - *Semiconductor Manufacturing International Corp. & Micron Technology, Inc., Shanghai, China*
Xiao Yong - *Huada Empyrean Software Co., Ltd, Beijing, China*

124.9 An Innovative IoT Platform Realizable by SD Card Slot Utilization with FlashAir
Kuniaki Ito, Keisuke Minami - *Toshiba Memory Corp., Kawasaki, Japan*
Sayako Kasahara - *Toshiba Memory Corp., Tokyo, Japan*
Masaomi Teranishi, Ryo Yonezawa - *Toshiba Memory Corp., Yokohama, Japan*
Daisuke Ajitomi - *Toshiba Memory Corp., Kawasaki, Japan*
Chikaaki Kodama, Mari Takada - *Toshiba Memory Corp., Yokohama, Japan*

124.10 Custom and Secure IoT Systems Built Easily
Simon Rance - *ARM, Inc., Richardson, TX*

124.11 Methodology for Seamless Integration of Double Patterned Metals
Samichi S - *Intel Corp. & Intel Technology India Pvt. Ltd, Varthu Hobli, Bellandur Post, Bangalore, Karnataka, India*
Madan Lal, Hassaly Mohamed M - *Intel Technology India Pvt. Ltd & Intel Corp., Bangalore, Karnataka, India*

124.12 Enhanced Yield Learning and Reduced Power for High Performance Industrial Designs
Sridhar Rangarajan, Ankit Kagliwal - *IBM Corp., Bangalore, India*
Mary Kusko - *IBM Corp., Poughkeepsie, NY*
Robert C. Redburn - *IBM Corp., Essex Junction, VT*
Bill Huott - *IBM Corp., Poughkeepsie, NY*

124.13 Metal Migration and Layout Porting Challenges
Joshua Paik, Tom Williams - *Qualcomm Technologies, Inc., Irvine, CA*

124.14 Mixed Signal SOC Physical Design Methodology
Gaurav K. Varshney, Penchalkumar Gajula - *Texas Instruments India Pvt. Ltd., Bangalore, India*

124.15 Automated Standard Cell Layout Generation For 7nm with SiliSire
Ramesh Koppadi, Bala Venkata Naga Durga Prasad Soutani, Aditya Siripragada, **Siva Krishna Potta**, Bipin B. Malhan - *INVECAS, Inc., Hyderabad, India*

124.16 Graphically Intensive EDA Tools on Integrated Web Platforms: An Experimental Evaluation
Arun Joseph, Sampath G. Baddam - *IBM Systems and Technology Group, Bangalore, India*
Shashidhar Reddy - *IBM Corp., Bangalore, India*
Wolfgang Roesner - *IBM Systems and Technology Group, Austin, TX*

124.17 Concurrent 3DIC Power Analysis for Xilinx SSIT Serdes Interface
Ling Yang, KangWei Lai - *Xilinx Inc., San Jose, CA*
Anusha Prakash - *ANSYS, Inc., San Jose, CA*

124.18 Environment for Heterogeneous Multi-Die System-Level Design and Physical Verification
Jami Al-Mahmood, **Sarojini Rajachidambaram**, Karthik Chandrasekar - *Intel Programmable Solutions Group, San Jose, CA*

DESIGNER/IP TRACK POSTER SESSION

124.19 A Fast GDS Merge and Layout Server Flow for Ultra Large-Scale SoC Design
Xiaochen Zhang - *HiSilicon, Chengdu, China*
Jing Lu - *Huada Empyrean Software Co., Ltd, Beijing, China*

124.20 An Efficient and Automatic Memory Compiler Quality Assurance Flow
Michael Yuan - *HiSilicon, Shenzhen, China*

124.21 Graphical Flow Management
Mukesh Bagul - *GLOBALFOUNDRIES, Bengaluru, India*
Greg Ford - *GLOBALFOUNDRIES, Santa Clara, CA*
Ananya Joisa - *GLOBALFOUNDRIES, Bangalore, India*

124.22 Improving Tool Console Management
Greg Ford - *GLOBALFOUNDRIES, Santa Clara, CA*

124.23 IBM 14nm Microprocessor Flow: RLM Construction
Gregory Schaeffer - *IBM Corp., Poughkeepsie, NY*
Joel Earl - *IBM Corp., Rochester, MN*
Harald Folberth - *IBM Corp., Boeblingen, Germany*
Veit Gernhoefer - *IBM Deutschland Research & Development GmbH, Boeblingen, Germany*
Edward Hughes - *IBM Corp., Wayne, PA*
John Schreck - *IBM Corp., Poughkeepsie, NY*

124.24 Fast Identification of Power-Critical Windows for Multi-Million Instance High-Speed Networking Design
Boris Hristov - *Ciena Corp., Ottawa, ON, Canada*
Preeti Gupta - *ANSYS, Inc., San Jose, CA*

124.25 Novel Connectivity Checking Approach for Advanced IC Packaging
Magesh Govindarajan - *Qualcomm, Inc. & Mentor, A Siemens Business, San Diego, CA*
Tarek Ramadan - *Mentor, A Siemens Business & NA, Cairo, Egypt*
John Ferguson - *Mentor, A Siemens Business, Wilsonville, OR*
Anup Keval, Lisk Durodami - *Qualcomm Technologies, Inc., San Diego, CA*

WORK-IN-PROGRESS POSTER SESSION

Time: 6:00 - 7:00pm || Room: Trinity Street Foyer
Event Type: Poster Session || Track: || Topic Area: General Interest

121.1 ApproxLUT: An Adaptive Lookup Table-Based Accelerator for Approximate Computing
Ye Tian, Qian Zhang, Ting Wang - *Chinese Univ. of Hong Kong, Hong Kong*
Qiang Xu - *Chinese Univ. of Hong Kong, Shatin, Hong Kong*

121.2 SAMG: Sparsified Algebraic Multigrid for Solving Large Symmetric Diagonally Dominant (SDD) Matrices
Zhiqiang Zhao, Yongyu Wang, Zhuo Feng - *Michigan Technological Univ., Houghton, MI*

121.3 Ir-Drop Aware Design & Technology Co-Optimization For N5 Node With Different Device And Cell Height Options
Luca Mattii - *Cadence Design Systems, Inc. & Technische Univ. Braunschweig, Leuven, Belgium*
Dragomir Milojevic - *IMEC & Univ. Lebre de Bruxelles, Heverlee, Belgium*
Peter Debacker - *IMEC, Heverlee, Belgium*
Vassilios Gerousis - *Cadence Design Systems, Inc., San Jose, CA*
Praveen Raghavan - *IMEC, Heverlee, Belgium*
Yasser Sherazi - *IMEC, Leuven, Belgium*
Mladen Berekovic - *Technische Univ. Braunschweig, Germany*

121.4 Accelerating Convolutional Neural Networks in Resource-Bound, Real-Time Embedded Systems
Adam Page, **Tinoosh Mohsenin** - *Univ. of Maryland, Baltimore, MD*

121.5 Field of Groves: An Energy-Efficient Random Forest
Zafar Takhirov, Joseph Wang, Marcia Sahaya Louis, Venkatesh Saligrama, Ajay Joshi - *Boston Univ., Boston, MA*

121.6 CORAL: Coarse-Grained Reconfigurable Architecture for ConvoLutional Neural Networks
Zhe Yuan, **Yongpan Liu**, Jinshan Yue, Jinyang Li, Huazhong Yang - *Tsinghua Univ., Beijing, China*

121.7 NVM-Based FPGA Block RAM With Adaptive SLC-MLC Conversion
Xiaojin Sui, **Lei Ju**, Mengying Zhao - *Shandong Univ., Jinan, China*
Chun Jason Xue - *City Univ. of Hong Kong, Hong Kong*
Jingtong Hu - *Oklahoma State Univ., Stillwater, OK*
Zhiping Jia - *Shandong Univ., Jinan, China*

121.8 A LEGO-Like Architecture for Scalable Deep Learning Accelerator
Yilei Li - *Univ. of California, Los Angeles & Kneron, Los Angeles, CA*
Chien-Heng Wong - *Univ. of California, Los Angeles, CA*
Chun-Chen Liu - *Kneron, San Diego, CA*
Yuan Du, Li Du - *Univ. of California, Los Angeles & Kneron, Los Angeles, CA*
Xiao Wang - *Cornell Univ., Ithaca, NY*
Mau-Chung Chang - *Univ. of California, Los Angeles & National Chiao Tung Univ., Los Angeles, CA*

121.9 Physics-Based Compact TDDB Models for Low-k BEOL Copper Interconnects with Time-Varying Voltage Stressing
Shaoyi Peng, Han Zhou, Taeyoung Kim - *Univ. of California, Riverside, CA*
Hai-Bao Chen - *Shanghai Jiao Tong Univ., Shanghai, China*
Sheldon Tan - *Univ. of California, Riverside, CA*

121.10 An SDN-Based Network Architecture for Internet of Things
Zhiyong Zhang, Zhiwei Zhang, Xiaojun Cai, Zhiping Jia - *Shandong Univ., Jinan, China*

121.11 Die-to-Package RCLM Extraction and Signal Integrity Co-Analysis for Fan-out Wafer-Level-Packaging
Yarui Peng - *Georgia Institute of Technology, Atlanta, GA*
Dusan Petranovic - *Mentor, A Siemens Business, Fremont, CA*
Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*

121.12 Characterization and Scheduling of Multithreaded Applications on Composite Cores Architectures
Hossein Sayadi, Avetsa Sasan - *George Mason Univ., Fairfax, VA*
Houman Homayoun - *George Mason Univ., Vienna, VA*

121.14 Parallel Order ATPG for Test Compaction
Yu-Wei Chen - *National Taiwan Univ., Taipei, Taiwan*
James C-M Li , Yu-Hao Ho, Chih-Ming Chang, Kai-Chieh Yang - *National Taiwan Univ., Taipei, Taiwan*

121.15 TaintHLS: Enabling Dynamic Information Flow Tracking in Hardware Accelerators
Christian Pilato - *Univ, of Lugano, Advanced Learning and Research Institute, Lugano, Switzerland*
Kaijie Wu - *Chongqing Univ. & Univ. of Illinois, Shapingba, China*
Siddharth Garg - *New York Univ., New York, NY*
Francesco Regazzoni - *Univ, of Lugano, Advanced Learning and Research Institute, Lugano, Switzerland*
Ramesh Karri - *New York Univ., Brooklyn, NY*

121.16 RIMPA: A New Reconfigurable In-Memory Processing Architecture With Spin Hall Effect-Driven Domain Wall Motion Device
Shaahin Angizi, Zhezhi He, **Deliang Fan** - *Univ. of Central Florida, Orlando, FL*

121.18 High Speed and Power Efficient Hierarchical SEC-DAEC-DEC code for Reliable Memory
Yonghae Kim - *Samsung Electronics Co., Ltd., Gyeonggi-do, Republic of Korea*
Joon-Sung Yang - *Sungkyunkwan Univ., Suwon, Republic of Korea*

121.19 Physics-Based Compact Electromigration Models Considering Wide Range of Current Stressing Conditions
Zeyu Sun, Chase W. Cook, Taeyoung Kim, Hengyang Zhao, Sheldon Tan - *Univ. of California, Riverside, CA*

121.20 Enabling Post-Silicon Hold Time Closure by Tunable-Buffer Insertion
Divya Akella Kamakshi, Xinfei Guo, Mircea Stan, Benton H. Calhoun - *Univ. of Virginia, Charlottesville, VA*

121.21 High Density, Low Power Cache Design With Magnetic Skyrmions Racetrack Memory
Fan Chen, Zheng Li - *Univ. of Pittsburgh, PA*
Wang Kang, Weisheng Zhao - *Beihang Univ., Beijing, China*
Helen Li - *Univ. of Pittsburgh, PA*

121.22 Scalable Signal Selection for Post-Silicon Debug
Kamran Rahmani - *Univ. of Florida, Sunnyvale, California*
Prabhat Mishra - *Univ. of Florida, Gainesville, FL*

121.23 Temporal Redundancy Latch-Based Architecture for Soft Error Mitigation
Robert Schmidt - *German Aerospace Center, Bremen, Germany*
Alberto García-Ortiz - *Univ. of Bremen, Germany*
Goerschwin Fey - *German Aerospace Center & Univ. of Bremen, Bremen, Germany*

121.24 Front-End-of-Line Attacks in Split Manufacturing
Minh-Tri Cao - *Univ. of Texas at Dallas, Richardson, TX*
Yujie Wang - *Nankai Univ., Nankai Qu, China*
Jiang Hu - *Texas A&M Univ., College Station, TX*
Jeyavijayan Rajendran - *Univ. of Texas at Dallas, Richardson, TX*

WORK-IN-PROGRESS POSTER SESSION

121.25 Physics-Based Analytical Modeling of Electromigration Reliability for Multi-Branch Interconnect Trees
Jiang-Tao Peng, Hai-Bao Chen - *Shanghai Jiao Tong Univ., Shanghai, China*
Taeyoung Kim, Hengyang Zhao, **Sheldon Tan** - *Univ. of California, Riverside, CA*

121.26 CAL: A Compiler-Assisted Lookahead Frontend Architecture for Mobile MPSoCs
Kyu Jung, Paul Jung - *Adaptmicrosys LLC, Erie, PA*

121.27 PT-Spike: A Flexible Precise-Time-Dependent Spiking Neuromorphic Architecture with Efficient Supervised Learning
Tao Liu, Wujie Wen - *Florida International Univ., Miami, FL*
Fuhong Lin - *Univ. of Science & Technology Beijing, China*
Lei Jiang - *Indiana Univ., Bloomington, IN*
Gang Quan - *Florida International Univ., Miami, FL*

121.28 Stabilizing Controller Design for On-Chip Power Delivery Networks
Joseph S. Riad, Peng Li, Edgar Sánchez-Sinencio - *Texas A&M Univ., College Station, TX*

121.29 Hybrid Polymorphic Logic Gate with 5-Terminal Magnetic Domain Wall Motion Device for Hardware Security.
Deliang Fan, Farhana Parveen - *Univ. of Central Florida, Orlando, FL*

121.30 Automated Methodology for Efficient Hardware Accelerator Design
Jeff Setter - *Standford Univ. & Advanced Micro Devices, Inc., Stanford, CA*
Jing Pu - *Stanford Univ., Stanford, CA*
Ravinder R. Rachala - *Advanced Micro Devices, Inc., Austin, TX*
Stuart Clubb - *Mentor, A Siemens Business, Wilsonville, OR*
Mark Horowitz - *Stanford Univ., Stanford, CA*
Stephen Kosonocky - *Advanced Micro Devices, Inc., Fort Collins, CO*

121.31 Support-Aware KL-Cuts
Jody Maick Matos, Vinicius N. Possani, Augusto Neutzling, Renato P. Ribas, Andre I. Reis - *Univ. Federal do Rio Grande do Sul, Porto Alegre, Brazil*

121.32 Towards Budget-Driven Hardware Optimization for Deep Convolutional Neural Networks Using Stochastic Computing
Zhe Li - *Syracuse Univ., Syracuse, NY*
Ji Li - *Univ. of Southern California, Los Angeles, CA*
Ao Ren - *Syracuse Univ., Syracuse, NY*
Jeffrey Draper - *Univ. of Southern California, Marina del Rey, CA*
Bo Yuan - *City Univ. of New York, NY*
Yang (Cindy) Yi - *Univ. of Kansas, Lawrence, KS*
Qinru Qiu, Yanzhi Wang - *Syracuse Univ., Syracuse, NY*

121.33 Acceleration Architecture for Decision Tree Classification Algorithm
Vahideh Akhlaghi, Mohsen Imani, Tajana Simunik Rosing, Rajesh K. Gupta - *Univ. of California, San Diego, La Jolla, CA*

121.34 A Quantization-Aware Regularized Learning Method in Multi-Level Memristor-Based Neuromorphic Computing System
Chang Song, Beiye Liu, Wei Wen - *Univ. of Pittsburgh, PA*
Hai Li - *Duke Univ., Durham, NC*
Yandan Wang - *Univ. of Pittsburgh, PA*

121.35 Communication-Aware Pipelined Instruction Set Architecture for AUTOSAR-Based Automotive ECUs
Ahmed Hamed - *Mentor, A Siemens Business, Cairo, Egypt*
Mona Safar, M. Watheq A. El-Kharashi - *Ain Shams Univ., Cairo, Egypt*
Ashraf Salem - *Mentor, A Siemens Business, Cairo, Egypt*

121.36 SPADES: Share Pattern Aware Hybrid Directory and Snoopy Coherence for Many Core Architectures
Sri Harsha Gade - *Indraprastha Institute of Information Technology, Delhi, India*
Antara Ganguly - *Indraprastha Institute of Information Technology, Delhi & Indian Institute of Technology, India*
Sujay Deb - *Indraprastha Institute of Information Technology, Delhi, India*

121.37 Diagonal Component Expansion for Flow-Layer Placement of Flow-Based Microfluidic Biochips
Brian Crites, Karen Kong, Philip Brisk - *Univ. of California, Riverside, CA*

121.38 Dendroplex: A Synthesis, Simulation, and Validation Flow for Hierarchical Temporal Memory on the Automata Processor
Mateja Putic, Mircea Stan - *Univ. of Virginia, Charlottesville, VA*

121.39 Dionysus: CPUs as Accelerators for FPGAs
Rashid Kaleem - *Univ. of Texas at Austin, TX*
Rajit Manohar - *Yale Univ., New Haven, CT*
Keshav Pingali - *Univ. of Texas at Austin, TX*

121.40 POLE: Probabilistic Online Learning Encoding to Reduce Data Transmission Energy in Off-Chip Interconnects
Seyed Mohammad Seyedzadeh, Helen Li, Alex K. Jones, Rami Melhem - *Univ. of Pittsburgh, PA*

121.41 Towards Reliability-Aware Circuit Design in Nanoscale FinFET Technology— New-Generation Aging Model and Circuit Reliability Simulator
Shaofeng Guo, Runsheng Wang, Zhuoqing Yu, Peng Hao, Pengpeng Ren, Yangyuan Wang - *Peking Univ., Beijing, China*
Siyu Liao, Chunyi Huang, Tianlei Guo, Alvin Chen, **Jushan Xie** - *Cadence Design Systems, Inc., San Jose, CA*
Ru Huang - *Peking Univ., Beijing, China*

121.42 Frequency Computing: An Approach for Emerging Energy-Efficient Systems
Matthew L. Joslin - *Univ. of Texas at Dallas, TX*
Joseph Callenes-Sloan - *Univ. of Texas at Dallas, Richardson, TX*

121.43 Effects of Clustering on Automatic Minimal Selection of Process Corner Simulations for Design Verification
Oleg Oleynikov, Bruce Cockburn, Jie Han, Witold Pedrycz - *Univ. of Alberta, AB, Canada*

121.44 Low-Cost High-Accuracy Variation Characterization for Nanoscale IC Technologies via Novel Learning-Based Techniques
Zhijian Pan - *Tsinghua Univ., Beijing, China*
Miao Li, **Jian Yao**, Hong Lu - *Platform Design Automation, Inc., Beijing, China*
Zuochang Ye - *Tsinghua Univ., Beijing, China*
Yanfeng Li - *Platform Design Automation, Inc., Beijing, China*
Yan Wang - *Tsinghua Univ., Beijing, China*

121.45 Reconfigurable Thermoelectric Generators for Vehicle Radiators
Caiwen Ding - *Syracuse Univ., Syracuse, NY*
Donkyu Baek - *Korea Advanced Institute of Science and Technology, Daejeon, Republic of Korea*
Sheng Lin - *Syracuse Univ., Syracuse, NY*
Donghwa Shin - *Yeungnam Univ., Gyeongsan, Republic of Korea*
Jaemin Kim - *Seoul National Univ., Seoul, Republic of Korea*
Xue Lin - *Northeastern Univ., Boston, MA*
Yanzhi Wang - *Syracuse Univ., Syracuse, NY*
Naehyuck Chang - *Korea Advanced Institute of Science and Technology, Daejeon, Republic of Korea*

121.46 RRAM-Based Reconfigurable In-Memory Computing Architecture With Hybrid Routing
Yue Zha, Jing Li - *Univ. of Wisconsin–Madison, WI*

WORK-IN-PROGRESS POSTER SESSION

121.47 Chip-Package-System Design Targeting Low IR-Drop in a Massively Parallel Compute Architecture
Love M. Cederström, Stefan Schiefer - *Technische Univ. Dresden & RacyICs GmbH, Dresden, Germany*
Sebastian Dietel - *RacyICs GmbH, Dresden, Germany*
Stefan Scholze, Dennis Walter, Stephan Henker, Jörg Schreiter, Sebastian Höppner - *Technische Univ. Dresden & RacyICs GmbH, Dresden, Germany*
Christian G. Mayr - *Technische Univ. Dresden, Germany*
Holger Eisenreich - *Technische Univ. Dresden & RacyICs GmbH, Dresden, Germany*

121.48 A Deep Reinforcement Learning-Based Framework for Cloud Resource Allocation
Jielong Xu, **Ning Liu**, Yanzhi Wang, Jian Tang - *Syracuse Univ., Syracuse, NY*

121.49 Networks-on-Chip Cortex Inspired Communication To Reduce Energy Consumption
Erwan Moréac, Johann Laurent, Pierre Bomel - *Univ. of South Brittany & Lab-STICC, Lorient, France*
André Rossi - *Univ. of Angers, France*
Emmanuel Boutillon - *Univ. of South Brittany & Lab-STICC, Lorient, France*
Andrea Mineo, Maurizio Palesi - *Univ. degli Studi di Catania, Italy*

121.50 Resource Efficient Design of Quantum Circuits for GaloisField Squaring and Exponentiation
Edgard Munoz-Coreas, **Himanshu Thapliyal** - *Univ. of Kentucky, Lexington, KY*

121.51 Look Before You Leap: A Secured Construction Of Branch Predictors
Sarani Bhattacharya, Debdeep Mukhopadhyay - *Indian Institute of Technology, Kharagpur, India*
Biswabandan Panda - *Indian Institute of Technology Madras, Chennai, India*

121.52 Concolic Testing of SystemC Designs
Bin Lin - *Portland State Univ., Portland, OR*
Kai Cong, Zhenkun Yang - *Intel Corp., Hillsboro, OR*
Zhigang Liao - *Virtual Device Technologies LLC, Portland, OR*
Tao Zhan - *Northwestern Polytechnical Univ., Xi'an, China*
Christopher Havlicek, **Fei Xie** - *Portland State Univ., Portland, OR*

121.53 IoT Network Intrusion Detection by Online Sequential Machine Learning Accelerator
Hantao Huang, Suleman K. Rai, **Hao Yu** - *Nanyang Technological Univ., Singapore*
Fengbo Ren - *Arizona State Univ., Tempe, Arizona*

121.54 On Accelerating Pair-HMM Computations in Programmable Hardware
Subho S. Banerjee - *Univ. of Illinois at Urbana-Champaign, IL*
Mohamed El-Hadedy - *Univ. of Virginia, Chartlottesville, VA*
Ching Yang Tan, Zbigniew T. Kalbarczyk, Steven S. Lumetta, Ravishankar K. Iyer - *Univ. of Illinois at Urbana-Champaign, IL*

121.55 CHASE: Contract-Based Requirement Engineering for Cyber-Physical System Design
Pierluigi Nuzzo - *Univ. of Southern California, Los Angeles, CA*
Michele Lora - *Univ. of Verona, Italy*
Yishai A. Feldman - *IBM Research - Haifa, Israel*
Alberto L. Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

121.56 A Programmable Event-Driven Architecture for Spiking Neural Network Evaluation
Arnab Roy - *Indian Institute of Technology Madras, Chennai, India*
Swagath Venkataramani - *Purdue Univ., West Lafayette, IN*
Neel T. Gala - *Indian Institute of Technology Madras, Chennai, India*
Sanchari Sen - *Purdue Univ., West Lafayette, IN*
Veezhinathan Kamakoti - *Indian Institute of Technology Madras, Chennai, India*
Anand Raghunathan - *Purdue Univ., West Lafayette, IN*

121.57 An RRAM-Based Hybrid Neural Network Computing System-on-Chip Design
Tianqi Tang, Lixue Xia - *Tsinghua Univ., Beijing, China*
Chen Weihao - *National Tsing Hua Univ., Hsinchu, Taiwan*
Fang Su - *Tsinghua Univ., Beijing, China*
Hsiao-Yun Chiu - *National Tsing Hua Univ., Hsinchu, Taiwan*
Zhibo Wang - *Tsinghua Univ., Beijing, China*
Kuo-Hsiang Hsu - *National Tsing Hua Univ., Hsinchu, Taiwan*
Ming Cheng, Boxun Li - *Tsinghua Univ., Beijing, China*
Chieh-Pu Lo, Meng-Fan Chang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Yongpan Liu, Yu Wang, Huazhong Yang - *Tsinghua Univ., Beijing, China*

121.58 Optimism-Controllable Pre-simulation-based Synchronization in Distributed Mixed-Signal Co-simulation
Moon Gi Seok - *Korea Advanced Institute of Science and Technology, Daejeon, Republic of Korea*
Tag Gon Kim - *KAIST, Daejeon, Republic of Korea*
Daejin Park - *Kyungpook National Univ., Daegu, Republic of Korea*

121.59 Design of a Multi-station Real-time Simulation Platform for Rapid Modeling/Prototyping of Cyber-physical Systems
Yong-Kyu Jung - *Gannon Univ., Erie, PA*

121.60 A Power Delivery Network and Cell Placement Aware Dynamic IR-Drop Mitigation Technique: Harvesting Unused Timing Slacks to Schedule Useful Skews
Lakshmi Bhamidipati, Bhoopal Gunna - *George Mason Univ., Fairfax, VA*
Houman Homayoun - *George Mason Univ., Vienna, VA*
Avesta Sasan - *George Mason Univ., Fairfax, VA*

121.61 NNgine: Ultra-Efficient Nearest Neighbor Accelerator Based on Near Data Computing
Mohsen Imani, **Yeseong Kim**, Tajana Simunik Rosing - *Univ. of California, San Diego, La Jolla, CA*

I LOVE DAC

WEAR YOUR I LOVE DAC BUTTON

Thank You to Our Sponsors:

CLIO SOFT

Booth 613

onespin

Booth 1547

Truechip
The Verification IP Specialist

Booth 741

Additional Meetings: See Pages 89 - 95.

DAC BEST PAPER AWARD PRESENTATION

Time: 9:00 - 9:10am || Room: Ballroom A || Track: EDA
Topic Area: General Interest

DAC will present the Research Best Paper Award and Best Poster as well as the Designer/IP Track Best Presentation Awards.

KEYNOTE: EMOTION TECHNOLOGY, WEARABLES, AND SURPRISES

ROSALIND PICARD – *Massachusetts Institute of Technology, Cambridge, MA*

Time: 9:10 – 10:00am || Room: Ballroom A || Track: IoT
Topic Area: General Interest

Years ago, I set out to create technology with emotional intelligence, demonstrating the ability to sense, recognize, and respond intelligently to human emotion. At MIT, we designed studies and developed signal processing and machine learning techniques to see what affective insights could be reliably obtained. In this talk I will highlight the most surprising findings during this adventure. These include new insights about the "true smile of happiness," discovering new ways cameras (and your smartphone, even in your handbag) can compute your bio-signals without using any new sensors, finding electrical signals on the wrist that reveal insight into deep brain activity, and learning surprising implications of wearable sensing for autism, anxiety, sleep, memory, epilepsy, and more. What is the grand challenge we aim to solve next?

Biography: Rosalind Picard, ScD, FIEEE is founder and director of the Affective Computing Research Group at the MIT Media Laboratory, co-founder of Affectiva, providing emotional intelligence technology used by 1/3 of the Global Fortune 100, and co-founder and Chief Scientist of Empatica, improving lives with clinical-quality wearable sensors and analytics. Picard is the author of over 250 articles in computer vision, pattern recognition, machine learning, signal processing, affective computing, and human-computer interaction. She is known internationally for her book, Affective Computing, which helped launch the field by that name. Picard holds bachelors in Electrical Engineering (EE) from Georgia Tech and Masters and Doctorate degrees in EE and CS from MIT. Picard's inventions have been twice named to "top ten" lists, including the New York Times Magazine's Best Ideas of 2006 for the Social Cue Reader, and 2011's Popular Science Top Ten Inventions for a Mirror that Monitors Vital Signs. CNN named her in 2015 one of seven "Tech Superheroes to Watch." Picard's lab at MIT develops technologies to better understand, predict, and regulate emotion, with applications aimed at helping people with autism, epilepsy, depression/anxiety, addiction, and chronic pain.

60

SECURITY NUTS AND BOLTS

Time: 10:30am - 12:00pm || Room: 15 || Event Type: Reviewed Presentations
Track: Security, Design || Topic Area: Digital Design

CHAIR:
Yier Jin - *Univ. of Central Florida, Orlando, FL*

CO-CHAIR:
Elena Dubrova - *Royal Institute of Technology, Kista, Sweden*

Designers need a wide range of building blocks and tools to support secure implementation of embedded systems. This session adds four novel and invaluable tools to the existing toolset. The first paper uses 'garbled circuits' to resist side-channel attacks.

The next paper proposes on-the-fly hardware support for statistical testing of random number generators. The third paper presents a high-performance hardware implementation of a new elliptic curve. The final paper offers a dedicated framework to test for fault attacks.

60.1 PriSearch: Efficient Search on Private Data (10:30)
M. Sadegh Riazi - *Univ. of California, San Diego, La Jolla, CA*
Ebrahim M. Songhori - *Rice Univ., Houston, TX*
Farinaz Koushanfar - *Univ. of California, San Diego, La Jolla, CA*

60.2 An Architecture for Learning Stream Distributions with Application to RNG Testing (10:45)
Alric Althoff - *Univ. of California, San Diego, CA*
Ryan Kastner - *Univ. of California, San Diego, La Jolla, CA*

60.3 Cryptography for Next Generation TLS: Implementing the RFC 7748 Elliptic Curve448 Cryptosystem in Hardware (11:00)
Pascal Sasdrich - *Ruhr Univ. Bochum, Germany*
Tim Güneysu - *Univ. of Bremen & DFKI GmbH, Germany*

60.4 Cross-Level Monte Carlo Framework for System Vulnerability Evaluation Against Fault Attack (11:15)
Meng Li - *Univ. of Texas at Austin, TX*
Liangzhen Lai, Vikas Chandra - *ARM Research & ARM, Inc., San Jose, CA*
David Z. Pan - *Univ. of Texas at Austin, TX*

▶ **A Q&A poster session will immediately follow the presentations from 11:30am - 12:00pm**

61

ROUTING FROM TOP TO BOTTOM

Time: 10:30am - 12:00pm || Room: 17AB || Event Type: Reviewed Presentations
Track: EDA || Topic Area: Physical Design & DFM, NoC, Chip & Package Scale Interconnect, Digital Design

CHAIR:
Yi-Xiao Ding - *Cadence Design Systems, Inc., Austin, TX*

CO-CHAIR:
Amin Farshidi - *Cadence Design Systems, Inc., Austin, TX*

This session covers all aspects of routing, starting from bus routing, through global routing, pin accessibility, all the way down to via arrays in latest technology node. The session starts with a bus routing algorithm that combines topology generation and wire synthesis. It is followed by a fast track assignment algorithm to estimate routability, and an ILP-based algorithm to select pin access location for better routability. The session ends with a study on EM impact to via arrays to improve the reliability of the designs.

61.1 Streak: Synergistic Topology Generation and Route Synthesis for On-Chip Performance-Critical Signal Groups (10:30)
Derong Liu - *Univ. of Texas at Austin, TX*
Vinicius Livramento - *Federal Univ.of Santa Catarina, Brazil*
Salim Chowdhury, Duo Ding, Huy Vo, Akshay Sharma - *Oracle Corp., Austin, TX*
David Z. Pan - *Univ. of Texas at Austin, TX*

61.2 TraPL: Track Planning of Local Congestion for Global Routing (10:45)
Daohang Shi, Azadeh Davoodi - *Univ. of Wisconsin, Madison, WI*

61.3 Concurrent Pin Access Optimization for Unidirectional Routing (11:00)
Xiaoqing Xu - *Univ. of Texas at Austin & ARM, Inc., Austin, TX*
Yibo Lin - *Univ. of Texas at Austin, TX*
Vinicius Livramento - *Federal Univ.of Santa Catarina, Brazil*
David Z. Pan - *Univ. of Texas at Austin, TX*

61.4 Incorporating the Role of Stress on Electromigration in Power Grids With Via Arrays (11:15)
Vivek Mishra - *Univ. of Minnesota, Twin Cities & Synopsys, Inc., Mountain View, CA*
Palkesh Jain - *Qualcomm India Pvt. Ltd., Bangalore, India*
Sravan K. Marella - *Univ. of Minnesota, Twin Cities & Intel Corp., Santa Clara, CA*
Sachin S. Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

▶ **A Q&A poster session will immediately follow the presentations from 11:30am - 12:00pm**

62

NEWS FLASHES ABOUT EMBEDDED STORAGE

Time: 10:30am - 12:00pm || Room: 18AB || Event Type: Reviewed Presentations
Track: Embedded Systems || Topic Area: Embedded System Software

CHAIR:
Jingtong Hu - *Oklahoma State Univ., Stillwater, OK*

CO-CHAIR:
Guangyu Sun - *Peking Univ., Beijing, China*

Reducing storage cost while maintaining efficiency is a recurring theme throughout the storage market, from the device level to the system level. The session begins with a discussion on a user-friendly method of swapping pages between main memory and storage in mobile platforms. Next is a smart data refresh scheme to resolve the latency issue of LDPC soft-sensing in flash storage devices. The final two papers show how to improve the usability and performance of Flash through erase-free programming and garbage collection.

62.1 SmartSwap: High-Performance and User Experience Friendly Swapping in Mobile Systems (10:30)
Xiao Zhu, Duo Liu, **Kan Zhong**, Jinting Ren - *Chongqing Univ., Chongqing, China*
Tao Li - *Univ. of Florida, Gainesville, FL*

62.2 Reducing LDPC Soft-Sensing Latency by Lightweight Data Refresh for Flash Read Performance Improvement (10:45)
Yajuan Du - *Huazhong Univ. of Science & Technology & City Univ. of Hong Kong, Wuhan, China*
Qiao Li, Liang Shi - *Chongqing Univ., Chongqing, China*
Deqing Zou, Hai Jin - *Huazhong Univ. of Science & Technology, Wuhan, China*
Chun Jason Xue - *City Univ. of Hong Kong, Hong Kong*

62.3 Improving Performance and Lifetime of Large-Page NAND Storages Using Erase-Free Subpage Programming (11:00)
Myungsuk Kim, Jaehoon Lee - *Seoul National Univ., Seoul, Republic of Korea*
Sungjin Lee - *Inha Univ., Incheon, Republic of Korea*
Jisung Park, Jihong Kim - *Seoul National Univ., Seoul, Republic of Korea*

62.4 VirtualGC: Enabling Erase-Free Garbage Collection to Upgrade the Performance of Rewritable SLC NAND Flash Memory (11:15)
Tseng-Yi Chen, Yuan-Hao Chang, Yuan-Hung Kuan, Yu-Ming Chang - *Academia Sinica, Taipei, Taiwan*

▶ **A Q&A poster session will immediately follow the presentations from 11:30am - 12:00pm**

63

A DEEP DIVE INTO NEURAL NETWORKS

Time: 10:30am - 12:00pm || Room: 18CD || Event Type: Reviewed Presentations
Track: Design || Topic Area: Emerging Architectures & Technologies

CHAIR:
Wei Zhang - *Hong Kong Univ. of Science and Technology, Hong Kong*

Efficient computation hardware is essential to stretch the full potential of deep neural networks. The first paper presents an architecture to enable training of neural networks in RRAM while maximizing the reuse of peripheral circuits. The second paper proposes a scaleable, reconfigurable, and energy efficient architecture built-on Memristive Crossbar Arrays (MCA) for deep Spiking Neural Networks (SNNs). The third paper proposes hardware-software codesign of highly-accurate and multiplier-free deep neural network by mapping floating-point based DNNs to dynamic fixed-point networks. The last paper proposes utilizing stochastic multipliers for deep convolutional neural networks to achieve high accuracy with optimized energy and area.

63.1 TIME: A Training-in-Memory Architecture for Memristor-Based Deep Neural Networks (10:30)
Ming Cheng, Lixue Xia, Zhenhua Zhu, Yi Cai - *Tsinghua Univ., Beijing, China*
Yuan Xie - *Univ. of California, Santa Barbara, CA*
Yu Wang - *Tsinghua Univ. & Electric Power Research Institute, Beijing, China*
Huazhong Yang - *Tsinghua Univ., Beijing, China*

63.2 RESPARC: A Reconfigurable and Energy-Efficient Architecture With Memristive Crossbars for Deep Spiking Neural Networks (10:45)
Aayush Ankit, Abhronil Sengupta, Priyadarshini Panda, Kaushik Roy - *Purdue Univ., West Lafayette, IN*

63.3 Hardware-Software Codesign of Accurate, Multiplier-Free Deep Neural Networks (11:00)
Hokchhay Tann, Soheil Hashemi, Iris Bahar, Sherief Reda - *Brown Univ., Providence, RI*

63.4 New Stochastic Computing Multiplier and Its Application to Deep Neural Networks (11:15)
Hyeonuk Sim, **Jongeun Lee** - *Ulsan National Institute of Science and Technology (UNIST), Ulsan, Republic of Korea*

▶ **A Q&A poster session will immediately follow the presentations from 11:30am - 12:00pm**

64

MAKING THE IOT REAL

Time: 10:30am - 12:00pm || Room: 19AB || Event Type: Reviewed Presentations
Track: Embedded Systems || Topic Area: SoC & Embedded System Architectures

CHAIR:
Aviral Shrivastava - *Arizona State Univ., Phoenix, AZ*

CO-CHAIR:
Kiyoung Choi - *Seoul National Univ., Seoul, Republic of Korea*

The Internet of Things promises to transform our lives in the coming decade. Achieving this vision will require the enabling technologies described in this session. The papers address a range of IoT systems, from on-body networks to large-scale distributed IoT systems. The first three papers develop methods for design space exploration, and the last paper explores the use of accelerators for deep learning in IoT.

64.1 Optimized Design of a Human Intranet Network (10:30)
Ali Moin - *Univ. of California, Berkeley, CA*
Pierluigi Nuzzo - *Univ. of Southern California, Los Angeles, CA*
Alberto L. Sangiovanni-Vincentelli, Jan M. Rabaey - *Univ. of California, Berkeley, CA*

64.2 ArchEx: An Extensible Framework for the Exploration of Cyber-Physical System Architectures (10:45)
Dmitrii Kirov - *Univ. of Trento, Italy*
Pierluigi Nuzzo - *Univ. of Southern California, Los Angeles, CA*
Roberto Passerone - *Univ. of Trento, Italy*
Alberto L. Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

64.3 EDiFy: An Execution Time Distribution Finder (11:00)
Boudewijn Braams, Sebastian J. Altmeyer, Andy D. Pimentel - *Univ. of Amsterdam, The Netherlands*

64.4 Real-Time Meets Approximate Computing: An Elastic CNN Inference Accelerator With Adaptive Trade-off Between QoS and QoR (11:15)
Ying Wang, Huawei Li, Xiaowei Li - *Chinese Academy of Sciences, Beijing, China*

▶ **A Q&A poster session will immediately follow the presentations from 11:30am - 12:00pm**

65

BRINGING ANALOG TO THE SYSTEM LEVEL

Time: 10:30am - 12:00pm || Room: 12AB || Event Type: Invited Presentations
Track: EDA || Topic Area: Analog & Mixed-signal Design, Test & Verification

CHAIR:
Carna Radojicic - *Technische Univ. Kaiserslautern, Germany*

ORGANIZER:
Carna Radojicic - *Technische Univ. Kaiserslautern, Germany*

The number of SoCs containing analog/mixed-signal blocks increases dramatically. These blocks are inevitable parts of today's SoCs for mobile communication, smart power, automotive, internet of things. Such SoCs require coupling of analog/mixed-signal components with digital and software parts that calibrate, configure, and control the analog parts. With increasing integration, the interaction between different parts gets more complex.

This brings new challenges in the design of such systems:

- How can we deal with "analog" issues such as process, voltage, temperature variations, and cross-talk?
- How can we bring analog/mixed-signal behavior into system-level, and how much?
- How can we increase verification coverage?

This session presents state-of-the-art from the industry and academic research to address these challenges.

65.1 ESL Design with SystemC-AMS (10:30)
Martin Barnasconi - *NXP Semiconductors, Eindhoven, The Netherlands*
Sumit Adhikari - *NXP Semiconductors, Hamburg, Germany*

65.2 Dealing with Uncertainties in Analog/Mixed-Signal Systems (11:00)
Christoph Grimm - *Univ. of Kaiserslautern, Germany*
Michael Rathmair - *Vienna Univ. of Technology, Vienna, Austria*

65.3 Advances in Formal Methods for the Design of Analog/Mixed-Signal Systems (11:30)
Vladimir Dubikhin - *Newcastle Univ., Newcastle upon Tyne, United Kingdom*
Chris Myers - *Univ. of Utah, Salt Lake City, UT*
Danil Sokolov - *Newcastle Univ., Newcastle upon Tyne, United Kingdom*
Ioannis Syranidis - *Cadence Design Systems GmbH, Munich, Germany*
Alex Yakovlev - *Newcastle Univ., Newcastle upon Tyne, United Kingdom*

66

MAKING TEST BETTER NOW AND IN THE FUTURE

Time: 1:30 - 3:00pm || Room: 15 || Event Type: Reviewed Presentations
Track: EDA || Topic Area: Test & Verification

CHAIR:
Rob Aitken - *ARM, Inc., San Jose, CA*

Emerging technologies and new design techniques pose new challenges for test methods. Additionally, current test technologies continue to be stressed by the growing complexity of silicon systems. This sessions covers advances in test technologies to address the emerging needs of memristor-based storage systems and asynchronous circuits. The continued increase of test data volume requires new solutions for test compression, while software solutions offer new alternatives for soft-error tolerance.

66.1 Test Methodology for Dual-Rail Asynchronous Circuits (1:30)
Kuan Yen Huang, Ting-Yu Shen, **Chien Mo Li** - *National Taiwan Univ., Taipei, Taiwan*

66.2 Sneak-Path Based Test and Diagnosis for 1R RRAM Crossbar Using Voltage Bias Technique (1:45)
Tianjian Li, Xiangyu Bi, Naifeng Jing, Xiaoyao Liang, **Li Jiang** - *Shanghai Jiao Tong Univ., Shanghai, China*

66.3 A New Paradigm for Synthesis of Linear Decompressors (2:00)
Emil Gizdarski, Peter Wohl, John Waicukauski - *Synopsys, Inc., Sunnyvale, CA*

66.4 InCheck: An In-Application Recovery Scheme for Soft-Errors (2:15)
Moslem Didehban - *Arizona State Univ., Tempe, AZ*
Sai Ram Dheeraj Lokam - *Arizona State Univ. & Intel Corp., Chandler, AZ*
Aviral Shrivastava - *Arizona State Univ., Tempe, AZ*

▶ **A Q&A poster session will immediately follow the presentations from 2:30 - 3:00pm**

67

SAVING TIME, POWER, AND MONEY WITH EMBEDDED SOFTWARE

Time: 1:30 - 3:00pm || Room: 17AB || Event Type: Reviewed Presentations
Track: Embedded Systems || Topic Area: Embedded System Software

CHAIR:
Vijay Raghunathan - *Purdue Univ., West Lafayette, IN*

Embedded platforms require clever programming strategies to make the most of the hardware. This session features four innovative software approaches that exploit special architectural features. The first two papers exploit heterogeneous CPU-GPU architectures for high-performance networking and energy efficient video decoding. The third paper proposes a technique to enable high-quality filtering for CD-quality music on tiny micro-controllers. The fourth paper presents a new file system for non-volatile memory that maximizes storage lifetime.

67.1 Latency-Aware Packet Processing on CPU-GPU Heterogeneous Systems (1:30)
Arian Maghazeh - *Linköping Univ., Linköping, Sweden*
Unmesh Dutta Bordoloi - *General Motors Research and Development, Warren, MI*
Usman Dastgeer, Alexandru Andrei - *Ericsson, Linkoping, Sweden*
Petru Eles, Zebo Peng - *Linköping Univ., Linköping, Sweden*

67.2 Cooperative DVFS for Energy-Efficient HEVC Decoding on Embedded CPU-GPU Architecture (1:45)
Fan Gong, **Lei Ju** - *Shandong Univ., Jinan, China*
Deshan Zhang - *Inspur Technologies Co., Ltd., Jinan, China*
Mengying Zhao, Zhiping Jia - *Shandong Univ., Jinan, China*

67.3 Fast and Energy-Efficient Digital Filters for Signal Conditioning in Low-Power Microcontrollers (2:00)
Carlos Moreno, Sebastian Fischmeister - *Univ. of Waterloo, ON, Canada*

67.4 Enabling Write-Reduction Strategy for Journaling File Systems Over Byte-Addressable NVRAM (2:15)
Tseng-Yi Chen, Yuan-Hao Chang - *Academia Sinica, Taipei, Taiwan*
Shuo-Han Chen, Chih-Ching Kuo - *National Tsing Hua Univ., Hsinchu, Taiwan*
Ming-Chang Yang - *Academia Sinica and National Taiwan Univ., Taipei, Taiwan*
Hsin-Wen Wei - *Tamkang Univ., Taipei, Taiwan*
Wei-Kuan Shih - *National Tsing Hua Univ., Hsinchu, Taiwan*

▶ **A Q&A poster session will immediately follow the presentations from 2:30 - 3:00pm**

68

YOUNGER, FASTER AND MORE CONNECTED

Time: 1:30 - 3:00pm || Room: 18AB || Event Type: Reviewed Presentations
Track: EDA, Embedded Systems || Topic Area: SoC & Embedded System Architectures, FPGA and Reconfigurable Systems

CHAIR:
Philip Brisk - *Univ. of California, Riverside, CA*

CO-CHAIR:
Gunar Schirner - *Northeastern Univ., Boston, MA*

We will explore how we can use application context to mitigate the effects of aging in microprocessors and to increase system performance. We will also look at the importance of staying connected, whether it is fully interconnecting your coarse grained compute array or hexagonally connecting your software defined radio.

68.1 HyCUBE: A CGRA With Reconfigurable Single-Cycle Multi-hop Interconnect (1:30)
Manupa Karunaratne, Aditi Kulkarni Mohite, Tulika Mitra, Li-Shiuan Peh - *National Univ. of Singapore, Singapore*

68.2 Phase-Driven Learning-Based Dynamic Reliability Management For Multi-Core Processors (1:45)
Zhiyuan Yang - *Univ. of Maryland, Greenbelt, MD*
Caleb Serafy - *Oracle Corp., Santa Clara, CA*
Tiantao Lu - *Cadence Design Systems, Inc., San Jose, CA*
Ankur Srivastava - *Univ. of Maryland, College Park, MD*

68.3 A Heterogeneous SDR MPSoC in 28 nm CMOS for Low-Latency Wireless Applications (2:00)
Sebastian Haas, Tobias Seifert, Benedikt Nöthen, Stefan Scholze, Sebastian Höppner, Andreas Dixius, Esther Perez Adeva, Thomas Augustin, Friedrich Pauls, Sadia Moriam, **Mattis Hasler**, Erik Fischer, Yong Chen, Emil Matus, Georg Ellguth, Stephan Hartmann, Stefan Schiefer, Love M. Cederström, Dennis Walter, Stephan Henker, Stefan Hänzsche, Johannes Uhlig - *Technische Univ. Dresden & RacylCs GmbH, Germany*
Holger Eisenreich - *RacylCs GmbH, Dresden, Germany*
Stefan Weithoffer, Norbert Wehn - *Technische Univ. Kaiserslautern, Germany*
René Schüffny, Christian Mayr, Gerhard Fettweis - *Technische Univ. Dresden, Germany*

68.4 Greybox Design Methodology: A Program Driven Hardware Co-Optimization With Ultra-Dynamic Clock Management (2:15)
Tianyu Jia, Russ Joseph, Jie Gu - *Northwestern Univ., Evanston, IL*

▶ **A Q&A poster session will immediately follow the presentations from 2:30 - 3:00pm**

69

MAKING A SPLASH WITH MICROFLUIDICS AND APPROXIMATE COMPUTING

Time: 1:30 - 3:00pm || Room: 18CD || Event Type: Reviewed Presentations
Track: Design || Topic Area: Emerging Architectures & Technologies

CHAIR:
Ahmed Hemani - *KTH Royal Institute of Technology, Stockholm, Sweden*

Microfluidics has emerged as a key technology for biochips, while approximate computing is an important paradigm for bio-inspired chips. The first paper in this session presents a distributed storage technique for microfluidic chips, enabling higher execution efficiency with fewer resources. The second paper presents a discrete model for networked labs-on-a-chip, enabling desingers and tools to efficiently determine droplet paths and positions. The third paper proposes a component-oriented general device concept for continuous-flow microfluidic devices. The final paper proposes an optimization framework for the approximate training of neural networks, consisting of iterative training with a judicious selection of training data.

69.1 Transport or Store? Synthesizing Flow-Based Microfluidic Biochipsusing Distributed Channel Storage (1:30)
Chunfeng Liu, Bing Li - *Technical University of Munich, Munich, Germany*
Hailong Yao - *Tsinghua Univ., Beijing, China*
Paul Pop - *Technical Univ. of Denmark, Kgs. Lyngby, Denmark*
Tsung-Yi Ho - *National Tsing Hua Univ., Hsinchu, Taiwan*
Ulf Schlichtmann - *Technical University of Munich, Germany*

69.2 A Discrete Model for Networked Labs-on-Chips: Linking the Physical World to Design Automation (1:45)
Andreas Grimmer, Werner Haselmayr, Andreas Springer, Robert Wille - *Johannes Kepler Univ. Linz, Austria*

69.3 Component-Oriented High-Level Synthesis for Continuous-Flow Microfluidics Considering Hybrid-Scheduling (2:00)
Mengchu Li - *Technische Univ. Munchen & Ludwig Maximilian Univ. of Munich, Germany*
Tsun-Ming Tseng, Bing Li - *Technische Univ. München, Germany*
Tsung-Yi Ho - *National Tsing Hua Univ., Hsinchu, Taiwan*
Ulf Schlichtmann - *Technische Univ. München, Germany*

69.4 On Quality Trade-off Control for Approximate Computing Using Iterative Training (2:15)
Chengwen Xu, Xiangyu Wu, Wenqi Yin - *Shanghai Jiao Tong Univ., Shanghai, China*
Qiang Xu - *Chinese Univ. of Hong Kong, Shatin, Hong Kong*
Naifeng Jing, Xiaoyao Liang, **Li Jiang** - *Shanghai Jiao Tong Univ., Shanghai, China*

▶ **A Q&A poster session will immediately follow the presentations from 2:30 - 3:00pm**

70

WHEN A CIRCUIT CAN GO WRONG, IT WILL

Time: 1:30 - 3:00pm || Room: 19AB || Event Type: Reviewed Presentations
Track: Design, EDA || Topic Area: Low-Power & Reliability, FPGA and Reconfigurable Systems, Digital Design

CHAIR:
Xuan 'Silvia' Zhang - *Washington Univ., Saint Louis, MO*

CO-CHAIR:
Jiang Hu - *Texas A&M Univ., College Station, TX*

Increasingly complex circuits mean there are increasingly more ways for them to break. This session presents efforts to characterize, predict, avoid, and debug failures in memory and gate-array circuits. The first paper in the session presents valuable measurements of errors in a 14nm FinFET technology The second paper presents a new model for system-level failures, while the third gives a novel architecture to prevent malicious attacks in DRAM. The final paper introduces an open framework for debugging parallel architectures with high-level synthesis.

70.1 On Characterizing Near-Threshold SRAM Failures in FinFET Technology (1:30)
Shrikanth Ganapathy, John Kalamatianos, Keith Kasprak - *Advanced Micro Devices, Inc., Sunnyvale, CA*
Steven Raasch - *Advanced Micro Devices, Inc., Boxborough, MA*

70.2 Correlated Rare Failure Analysis via Asymptotic Probability Evaluation (1:45)
Jun Tao, Handi Yu - *Fudan Univ., Shanghai, China*
Dian Zhou - *Univ. of Texas at Dallas, TX*
Yangfeng Su, Xuan Zeng - *Fudan Univ., Shanghai, China*
Xin Li - *Duke Kunshan University, Kunshan, Jiangsu & Duke Univ., Durham, NC*

70.3 Making DRAM Stronger Against Row Hammering (2:00)
Mungyu Son, Hyunsun Park - *Pohang Univ. of Science and Technology, Pohang, Republic of Korea*
Junwhan Ahn, Sungjoo Yoo - *Seoul National Univ., Seoul, Republic of Korea*

70.4 Developing Dynamic Profiling and Debugging Support in OpenCL for FPGAs (2:15)
Anshuman Verma - *Virginia Polytechnic Institute and State Univ., Blacksburg, VA*
Huiyang Zhou - *North Carolina State Univ., Raleigh, NC*
Skip Booth - *Cisco Systems, Inc., Raleigh, NC*
Robbie King, James Coole, John Marshall, Andy Keep - *Cisco Systems, Inc. & NA, Raleigh, NC*
Wu-chun Feng - *Virginia Polytechnic Institute and State Univ. & NA, Blacksburg, VA*

▶ **A Q&A poster session will immediately follow the presentations from 2:30 - 3:00pm**

71

BEYOND DEEP LEARNING

Time: 1:30 - 3:00pm || Room: 12AB || Event Type: Invited Presentations
Track: Embedded Systems, IoT || Topic Area: Emerging Architectures & Technologies, SoC & Embedded System Architectures, General Interest

CHAIR:
Muhammad Shafique - *Vienna Univ. of Technology, Vienna, Austria*

ORGANIZERS:
Sai Manoj Pudukotai Dinakarrao - *Vienna Univ. of Technology, Vienna, Austria*
Muhammad Shafique - *Vienna Univ. of Technology, Vienna, Austria*
Faisal Shafait - *National University of Sciences and Technology, Islamabad, Pakistan*

Machine learning techniques such as deep neural networks (DNNs) are employed in a wide range of applications. Advances in machine learning systems, with inspiration from the human brain, have the potential to fundamentally transform computing. This special session brings leading experts from the industry to explore advances for the next generation of intelligent systems, including brain-inspired algorithms, the design of deep learning accelerators, and neuromorphic computing.

71.1 Accelerator Design for Deep Learning Training (1:30)
Kailash Gopalakrishnan, Ankur Agrawal, Chia-Yu Chen, Jungwook Choi, Jinwook Oh, Sunil Shukla, Viji Srinivasan, Wei Zhang - *IBM T.J. Watson Research Center, Yorktown Heights, NY*

71.2 Designing Efficient & Scalable Neuromorphic Systems (2:00)
Vivek De - *Intel Corp., Portland, OR*

71.3 The Importance of Brain Theory in Creating Intelligent Systems (2:30)
Austin Marshall - *Numenta, Inc., Redwood City, CA*

72

MAKING NEURAL NETWORKS GREAT AGAIN

Time: 3:30 - 5:30pm || Room: 15 || Event Type: Reviewed Presentations
Track: Design || Topic Area: Emerging Architectures & Technologies

CHAIR:
Tulika Mitra - *National Univ. of Singapore, Singapore*

Reducing overheads and increasing performance are important in neural networks. In the first paper, a case study is performed to map the feature extraction stage of pedestrian detection onto a neuromophic platform. In the second paper convolutions are replaced with point-wise multiplication. In the third paper all kernels are decomposed into sub-kernels with common parts. In the fourth paper an automated deep learning framework proposed. In the fifth paper Winograd's minimal filtering theory is used for CNN implementation. In the last paper a semantic correlation based data prefetch method is proposed to achieve parallel processing.

72.1 Co-Training of Feature Extraction and Classification Using Partitioned Convolutional Neural Networks (3:30)
Wei-Yu Tsai, Jinhang Choi, Tulika Parija, Priyanka Gomatam, Chita R. Das, John Sampson, Vijaykrishnan Narayanan - *Pennsylvania State Univ., University Park, PA*

72.2 Design of an Energy-Efficient Accelerator for Training of Convolutional Neural Networks Using Frequency-Domain Computation (3:45)
Jong Hwan Ko, Burhan A. Mudassar, Taesik Na, Saibal Mukhopadhyay - *Georgia Institute of Technology, Atlanta, GA*

72.3 A Kernel Decomposition Architecture for Binary-Weight Convolutional Neural Networks (4:00)
Hyeonuk Kim, Jaehyeong Sim, Yeongjae Choi, Lee-Sup Kim - *KAIST, Daejeon, Republic of Korea*

72.4 Deep^3: Leveraging Three Levels of Parallelism for Efficient Deep Learning (4:15)
Bita Darvish Rouhani - *Univ. of California, San Diego, La Jolla, CA*
Azalia Mirhoseini - *Rice Univ., Houston, TX*
Farinaz Koushanfar - *Univ. of California, San Diego, La Jolla, CA*

72.5 Exploring Heterogeneous Algorithms for Accelerating Deep Convolutional Neural Networks on FPGAs (4:30)
Qingcheng Xiao, Yun Liang, Liqiang Lu - *Peking Univ., Beijing, China*
Shengen Yan - *SenseTime Group Limited & Chinese Univ. of Hong Kong, Beijing, China*
Yu-Wing Tai - *SenseTime Group Limited, Beijing, China*

72.6 A Fast and Power Efficient Architecture to Parallelize LSTM Based RNN for Cognitive Intelligence Applications (4:45)
Peng Ouyang, Shouyi Yin, Shaojun Wei - *Tsinghua Univ., Beijing, China*

▶ **A Q&A poster session will immediately follow the presentations from 5:00 - 5:30pm**

73

TURBO-CHARGED DIGITAL SIMULATION FOR TIMING AND POWER

Time: 3:30 - 5:30pm || Room: 17AB || Event Type: Reviewed Presentations
Track: EDA, Design || Topic Area: Simulation & Timing Analysis, Digital Design

CHAIR:
Frank Liu - *IBM Research - Austin, TX*

CO-CHAIR:
Pingqiang Zhou - *ShanghaiTech Univ., Shanghai, China*

Simulation efficiency is a critical requirement for digital analysis tools, especially when the design scale dramatically increases. This session addresses such needs in chip timing, clocking and power networks. Learn about exploiting metal segments for hold time optimization from the first paper. The next two papers teaches us how to improve the accuracy of timing analysis. The fourth paper shows how to reduce power through a new clocking strategy. The session ends with two graph-based approaches for efficient power grid analysis. Please visit this exciting session that brings you to the frontier of digital simulation.

73.1 Power and Area Efficient Hold Time Fixing by Free Metal Segment Allocation (3:30)
Wei-Lun Chiu, Iris Hui-Ru Jiang - *National Chiao Tung Univ., Hsinchu, Taiwan*
Chien-Pang Lu, Yu-Tung Chang - *MediaTek, Inc., Hsinchu, Taiwan*

73.2 LibAbs: An Efficient and Accurate Timing Macro-Modeling Algorithm for Large Hierarchical Designs (3:45)
Tin-Yin Lai, Tsung-Wei Huang, Martin D.F. Wong - *Univ. of Illinois at Urbana-Champaign, IL*

73.3 LSTA: Learning-Based Static Timing Analysis for High-Dimensional Correlated On-Chip Variations (4:00)
Song Bian, Michihiro Shintani, Masayuki Hiromoto, Takashi Sato - *Kyoto Univ., Kyoto, Japan*

73.4 A Clock Skewing Strategy to Reduce Power and Area of ASIC Circuits (4:15)
Niranjan Kulkarni - *Arizona State Univ. & Cadence Design Systems, Inc., Tempe, AZ*
Aykut Dengi, **Sarma Vrudhula** - *Arizona State Univ., Tempe, AZ*

73.5 A Spectral Graph Sparsification Approach to Scalable Vectorless Power Grid Integrity Verification (4:30)
Zhiqiang Zhao, Zhuo Feng - *Michigan Technological Univ., Houghton, MI*

73.6 Convergence-Boosted Graph Partitioning Using Maximum Spanning Trees for Iterative Solution of Large Linear Circuits (4:45)
Ya Wang, Wenrui Zhang, Peng Li - *Texas A&M Univ., College Station, TX*
Jian Gong - *Intel Corp., Hillsboro, OR*

▶ **A Q&A poster session will immediately follow the presentations from 5:00 - 5:30pm**

74

FLAVORS OF LOGIC SYNTHESIS

Time: 3:30 - 5:30pm || Room: 18AB || Event Type: Reviewed Presentations
Track: EDA || Topic Area: Logic & High-Level Synthesis, Low-Power & Reliability

CHAIR:
Zhiru Zhang - *Cornell Univ., Ithaca, NY*

Synthesis continues to be a fertile ground for innovation in design automation algorithms and improvements in IC quality. This session features advances in synthesis including retiming latch-based designs, slicing datapath designs for better placement, error-tolerant circuit synthesis, interactive synthesis, performance analysis for asynchronous circuits, and low-power sensor interfaces.

74.1 Retiming of Two-Phase Latch-Based Resilient Circuits (3:30)
Hsiao-Lun Wang - *Univ. of Southern California, LA, CA*
Minghe Zhang - *Tsinghua Univ., Beijing Shi, China*
Peter A. Beerel - *Univ. of Southern California, Los Angeles, CA*

74.2 Graph-Based Logic Bit Slicing for Datapath-Aware Placement (3:45)
Chau-Chin Huang, Bo-Qiao Lin, Hsin-Ying Lee, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*
Kuo-Sheng Wu, Jun-Zhi Yang - *MediaTek, Inc., Hsinchu, Taiwan*

74.3 SABER: Selection of Approximate Bits for the Design of Error Tolerant Circuits (4:00)
Deepashree Sengupta, Farhana Sharmin Snigdha - *Univ. of Minnesota, Twin Cities, Minneapolis, MN*
Jiang Hu - *Texas A&M Univ., College Station, TX*
Sachin S. Sapatnekar - *Univ. of Minnesota, Twin Cities, Minneapolis, MN*

74.4 Closing the Accuracy Gap of Static Performance Analysis of Asynchronous Circuits (4:15)
Cheng-Yu Shih, Chun-Hong Shih, Jie-Hong (Roland) Jiang - *National Taiwan Univ., Taipei, Taiwan*

74.5 LiveSynth: Towards an Interactive Synthesis Flow (4:30)
Rafael Trapani Possignolo, Jose Renau - *Univ. of California, Santa Cruz, CA*

74.6 An Ultra-Low Power Address-Event Sensor Interface for Energy-Proportional Time-to-Information Extraction (4:45)
Alfio Di Mauro - *Swiss Federal Institute of Technology, Zurich, Switzerland*
Francesco Conti, Luca Benini - *Swiss Federal Institute of Technology & Univ. di Bologna, Zurich, Switzerland*

▶ **A Q&A poster session will immediately follow the presentations from 5:00 - 5:30pm**

75

#ALT_COMPUTING: MAKE USE OF EMERGING TECHNOLOGIES

Time: 3:30 - 5:30pm || Room: 18CD || Event Type: Reviewed Presentations
Track: EDA || Topic Area: Emerging Architectures & Technologies

CHAIR:
Luca Amaru - *Synopsys, Inc., Mountain View, CA*

This session showcases 6 papers covering quantum computing and other emerging technologies. The first 3 papers present different solutions to challenges in quantum computing. In particular, the papers propose a Pauli frame module, an embedding technique for solving the constrained satisfaction problem using a D-Wave quantum annealer, and a synthesis algorithm based on k-LUT networks. The second group of papers present different synthesis approaches for emerging technologies and paradigms, including a placement algorithm for 2D directed self-assembly, a wire routing methodology for logic arrays based on pseudo-CMOS logic, and a stochastic ODE solver.

75.1 Pauli Frames for Quantum Computer Architectures (3:30)
Leon Riesebos, Xiang Fu, Savvas Varsamopoulos, Carmen G. Almudever, Koen Bertels - *Delft Univ. of Technology, Delft, The Netherlands*

75.2 Fast Embedding of Constrained Satisfaction Problem to Quantum Annealer With Minimizing Chain Length (3:45)
Juexiao Su, Lei He - *Univ. of California, Los Angeles, CA*

75.3 Hierarchical Reversible Logic Synthesis Using LUTs (4:00)
Mathias Soeken - *École Polytechnique Fédérale de Lausanne, Switzerland*
Martin Roetteler, Nathan Wiebe - *Microsoft Research, Redmond, WA*
Giovanni De Micheli - *École Polytechnique Fédérale de Lausanne, Switzerland*

75.4 Detailed Placement for Two-Dimensional Directed Self-Assembly Technology (4:15)
Zhi-Wen Lin, Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*

75.5 Design Methodology for Thin-Film Transistor Based Pseudo-CMOS Logic Array With Multi-Layer Interconnect Architecture (4:30)
Qinghang Zhao, Yongpan Liu, Wenyu Sun - *Tsinghua Univ., Beijing, China*
Jiaqing Zhao - *Shanghai Jiao Tong Univ., Shanghai, China*
Hailong Yao - *Tsinghua Univ., Beijing, China*
Xiaojun Guo - *Shanghai Jiao Tong Univ., Shanghai, China*
Huazhong Yang - *Tsinghua Univ., Beijing, China*

75.6 Hardware ODE Solvers Using Stochastic Circuits (4:45)
Siting Liu, Jie Han - *Univ. of Alberta, Edmonton, AB, Canada*

▶ **A Q&A poster session will immediately follow the presentations from 5:00 - 5:30pm**

76

REMEMBER WHAT YOU LEARN

Time: 3:30 - 5:30pm || Room: 19AB || Event Type: Reviewed Presentations
Track: EDA || Topic Area: Emerging Architectures & Technologies

CHAIR:
Deliang Fan - *Univ. of Central Florida, Orlando, FL*

CO-CHAIR:
Anup Kumar Das - *IMEC, Eindhoven, The Netherlands*

Memory is an inherent part of any computational system, and efficient optimization is required to maximize application-level performance. The first three papers consider fundamental emerging memory limitations such as non-uniform access latency and read disturbances by proposing novel virtual address re-mapping or partitioning techniques. Interest in neuromorphic computing platforms continues to grow, and researchers continue to look for new ways to create compact and efficient networks and novel hardware platforms. The remaining three papers discuss techniques to reduce network size, reduce the impact of hardware defects on computational accuracy, and exploit existing hardware for efficient links between neurons and synapses.

76.1 A Novel ReRAM-Based Main Memory Structure for Optimizing Access Latency and Reliability
Yang Zhang, Dan Feng, JingNing Liu, Wei Tong, Bing Wu, Caihua Fang - *Huazhong Univ. of Science & Technology, Wuhan, China*

76.2 Boosting the Performance of 3D Charge Trap NAND Flash With Asymmetric Feature Process Size Characteristic
Shuo-Han Chen - *National Tsing Hua Univ., Hsinchu, Taiwan*
Yen-Ting Chen - *National Tsing Hua Univ., New Taipei, Taiwan*
Hsin-Wen Wei - *Tamkang Univ., Taipei, Taiwan*
Wei-Kuan Shih - *National Tsing Hua Univ., Hsinchu, Taiwan*

76.3 Disturbance Aware Memory Partitioning for Parallel Data Access in STT-RAM
Shouyi Yin, **Zhicong Xie**, Shaojun Wei - *Tsinghua Univ., Beijing, China*

76.4 Group Scissor: Scaling Neuromorphic Computing Design to Large Neural Networks
Yandan Wang, Wei Wen, Beiye Liu, Donald Chiarulli, Helen Li - *Univ. of Pittsburgh, PA*

76.5 Adaptation of Enhanced TSV Capacitance as Membrane Property in 3D Brain-Inspired Computing System
Md Amimul Ehsan, Hongyu An - *Univ. of Kansas, Lawrence, KS*
Zhen Zhou - *Intel Corp., Santa Clara, CA*
Yang Yi - *Univ. of Kansas, Lawrence, KS*

76.6 Rescuing Memristor-Based Neuromorphic Design With High Defects
Chenchen Liu - *Univ. of Pittsburgh, PA*
Miao Hu, John Paul Strachan - *Hewlett-Packard Labs., Palo Alto, CA*
Helen Li - *Univ. of Pittsburgh, PA*

77

PANEL: YOUR INTELLECTUAL PROPERTY HAS BEEN STOLEN - NOW WHAT? HOW THE SEMICONDUCTOR INDUSTRY CAN COMBAT THIS GLOBAL PROBLEM

Time: 3:30 - 4:20pm || Room: 12AB || Event Type: Panel || Track: Security, EDA
Topic Area: General Interest

MODERATOR:
Ted Miracco - *SmartFlow Compliance Solutions, San Jose, CA*

ORGANIZER:
Ted Miracco - *SmartFlow Compliance Solutions, San Jose, CA*

This panel will explore IP theft and how the Semiconductor and EDA industries can come together and move forward to combat this growing problem. Highly technical intellectual property (IP), including everything from soft and hard IP cores to electronic design automation (EDA) software used in military and defense applications, is being stolen. Ted Miracco is the co-founder of SmartFlow Compliance Solutions, a leading cyber-security and anti-piracy company he started after a long battle against copyright and IP theft of EDA tools. Ted, Warren Savage, Kurt Shuler, Rob Ballow and Liz Ruetsch bring a wealth of experience in dealing with the misappropriation of semiconductor IP and use of counterfeit licenses to EDA software. David Locke Hall brings a government perspective on what the government is, or is not, doing to help companies combat software piracy. The panel will also discuss the damage that is being done by this sustained threat to fair market competition, the U.S. and world economies, and private and public security.

PANELISTS:
Warren Savage - *Silvaco, Inc., Santa Clara, CA*
Kurt Shuler - *Arteris, Inc., Campbell, CA*
Liz Ruetsch - *Keysight Technologies, Santa Rosa, CA*
David Locke Hall - *Wiggin and Dana LLP, Philadelphia, PA*
Rob Ballow - *KPMG LLC, Santa Clara, CA*

78

PANEL: IS THE FUTURE OF EDA IN THE CLOUD?

Time: 4:30 - 5:20pm || Room: 12AB || Event Type: Panel || Track: EDA
Topic Area: General Interest

MODERATOR:

Mojy Chian - *ON Semiconductor, Phoenix, AZ*

Migration to the cloud is inevitable for scientific and engineering applications, but security has been an ever-increasing concern. In particular, the IC design environment is a multi-organizational platform (EDA companies, foundries, IP providers, and design companies) and hence is more prone to security concerns. EDA companies have also been concerned about loss of revenue because of the increased efficiency of using EDA tools in the cloud.

Recent technology advances have been addressing many of the security concerns, but the impediments in the business model for using EDA tools in the cloud remain.

In this panel of experts, we will directly address the technical and business challenges for IC design in cloud. Will the enablers of the cloud be the last community to use it?

PANELISTS:

Wilbur Luo - *Cadence Design Systems, Inc., San Jose, CA*
W. Rhett Davis - *North Carolina State Univ., Raleigh, NC*
Marc Edwards - *Silicon Cloud International Pte Ltd, Cary, NC*

THURSDAY IS TRAINING DAY

TRACK 1, PART I: HOW TO BUILD CLASS-BASED VERIFICATION ENVIRONMENTS IN SYSTEMVERILOG

Time: 10:15am - 1:15pm || Room: Ballroom E || Track: EDA || Topic Area: Test & Verification
Event Type: Thursday is Training Day

This session will teach the key SystemVerilog language skills needed to understand and build class-based constrained random verification environments, as used by UVM. The emphasis will be on learning to apply the concepts of object-oriented programming to the creation of a re-usable test bench infrastructure. Language features will be taught using working code examples, which delegates can run immediately on the EDA Playground website and will be available to use and share after the class.

Topics to be taught include the object-oriented and constrained random language features of SystemVerilog, and more particularly how to use these language features to build a verification environment that includes a component hierarchy and transaction-level communication.

The knowledge taught in this session is an essential prerequisite to the afternoon session on UVM.

This track is taught by David C. Black, Doulos Senior Member Technical Staff, who is co-author of the book, “SystemC: From the Ground Up.”

SPEAKER:
David Black - *Doulos Ltd., Austin, TX*

Thank You to Our Sponsor

DOULOS

TRACK 2, PART I: FORMAL VERIFICATION USING SYSTEMVERILOG ASSERTIONS

Time: 10:15am - 1:15pm || Room: Ballroom F || Track: EDA || Topic Area: Test & Verification
Event Type: Thursday is Training Day

This session will teach attendees how to use formal verification to verify RTL code by writing SystemVerilog Assertions (SVA). The emphasis will be on the practicalities of running today’s formal verification tools: how to write SVA, how to run the tools, how to get results from the tools, and what to do when formal proofs don’t finish. The session will cover all the main concepts and the pitfalls likely to be encountered when someone runs formal verification for the first time.

This session is aimed at RTL design and verification engineers who want to become familiar with the practical application of formal verification. Prior knowledge of SVA would be an advantage but is not required.

This track is taught by Doulos CTO John Aynsley, winner of the Accellera Systems Initiative 2012 Technical Excellence Award for his contribution to the development of language standards.Speaker:

SPEAKER:
John Aynsley - *Doulos Ltd., Ringwood, United Kingdom*

Thank You to Our Sponsor

DOULOS

THURSDAY IS TRAINING DAY

TRACK 3, PART I: RAISING YOUR C++ GAME

Time: 10:15am - 1:15pm || Room: Ballroom F || Track: EDA, IOT
Topic Area: General Interest || Event Type: Thursday is Training Day

ORGANIZER:
John Croix - *Cadence Design Systems, Inc., Austin, TX*

C++ was already a large and complex language prior to the changes introduced in C++11/14 — changes that almost doubled the size of the standard to over 1300 pages in length. Additionally there are also many different software packages and libraries, like STL and Boost, that leverage C++ features to provide abstract classes, concepts, and algorithms to improve programmer productivity and program reliability. Unfortunately, while abstraction can yield many benefits, it can also make it harder to debug a C++ program through many layers of code that are often in the form of templates. Thus, to be a good C++ programmer, an individual needs to understand the language, be aware of libraries that they can leverage, and know how to effectively and efficiently debug complex C++ code.

This DAC tutorial will focus on specific aspects of application development in C++, with presentations by C++ experts from Cadence Design Systems, Samsung, and Trull Consulting. The session will cover serialization methodologies, the application of modern C++ techniques to engineering software, and C++ optimization identification and implementation strategies.

About the Speakers:
Jeff Trull, owner of Trull Consulting, began his career as a VLSI circuit designer and graduated to CAD scripter and eventually, manager. He subsequently transitioned to EDA software engineer, and then full-time C++ consultant. He remembers well the problems he faced trying to tape out chips and is excited to apply some of what he's learned in the meantime.

Aditya Kumar works at Samsung (SARC) as a Senior Compiler Engineer. Previously he worked at Qualcomm (Austin) also as a compiler engineer. He received his masters in Computer Science from Texas A&M University. His interests include C++ programming, compiler design, static analysis, software engineering, and artificial intelligence.

Ningyu Shi, Senior Principle Software Engineer at Cadence Design Systems in Austin, started his career in Magma Design Automation as a C/C++ developer in their Fast-SPICE simulation group. He is interested in designing complex high performance systems, and C++ naturally became his goto language for the work. He now works in the Voltus power signoff group in Cadence, focusing on domain-specific distributed system development.

SPEAKERS:
Jeff Trull - *Trull Consulting, San Francisco , CA*
Aditya Kumar - *Samsung Electronics Co., Ltd., Austin, TX*
Ningyu Shi - *Cadence Design Systems, Inc., Austin, TX*

TRACK 1, PART II: PART II: LEARN UVM USING THE EASIER UVM CODING GUIDELINES AND CODE GENERATOR

Time: 2:15 - 5:15pm || Room: Ballroom E || Track: EDA || Topic Area: Test & Verification
Event Type: Thursday is Training Day

This session will teach the basics of UVM, the Universal Verification Methodology for SystemVerilog, by taking advantage of Doulos' Easier™ UVM Coding Guidelines and Code Generator. All the main concepts of UVM will be taught using working code examples. By running the Easier™ UVM Code Generator on the EDA Playground website, delegates will be able to run UVM examples immediately, experiment with what they have learned, and share their examples with others after the class.

The session is aimed at hands-on engineers who want to start writing UVM code themselves and are looking for some specific advice on the best place to start, the right UVM features and coding idiom to use, and the pitfalls to avoid.

This track is taught by David C. Black, Doulos Senior Member Technical Staff, who is co-author of the book, "SystemC: From the Ground Up."

SPEAKER:
David Black - *Doulos Ltd., Austin, TX*

Thank You to Our Sponsor

DOULOS

THURSDAY IS TRAINING DAY

TRACK 2, PART II: THE PYTHON LANGUAGE: BECOME A PYTHONEER!

Time: 2:15 - 5:15pm || Room: Ballroom F || Track: EDA || Topic Area: Test & Verification
Event Type: Thursday is Training Day

This session will teach attendees the basics of the Python programming language. Python has become enormously popular as a programming language because it is compact, elegant, productive, readable, and extensible. People often remark that a Python program looks like pseudo-code, an English language description of what the code is meant to do. These attributes have led Python to be widely used as a general purpose scripting language in EDA tool flows, for scientific computing and machine learning, for embedded software test, and even for digital hardware verification and system modeling.

People sometimes become very enthusiastic about Python because of its elegance as a programming language – so-called Pythoneers. This session is your chance to become a Pythoneer, and to learn about some of the cool things you can do with Python right out-of-the-box!

This track is taught by Doulos CTO John Aynsley, winner of the Accellera Systems Initiative 2012 Technical Excellence Award for his contribution to the development of language standards.

SPEAKER:
John Aynsley - *Doulos Ltd., Ringwood, United Kingdom*

Thank You to Our Sponsor

DOULOS

TRACK 3, PART II: RAISING YOUR C++ GAME

Time: 2:15 - 5:15pm || Room: Ballroom F || Track: EDA, IOT
Topic Area: General Interest || Event Type: Thursday is Training Day

ORGANIZER:
John Croix - *Cadence Design Systems, Inc., Austin, TX*

C++ was already a large and complex language prior to the changes introduced in C++11/14 — changes that almost doubled the size of the standard to over 1300 pages in length. Additionally there are also many different software packages and libraries, like STL and Boost, that leverage C++ features to provide abstract classes, concepts, and algorithms to improve programmer productivity and program reliability. Unfortunately, while abstraction can yield many benefits, it can also make it harder to debug a C++ program through many layers of code that are often in the form of templates. Thus, to be a good C++ programmer, an individual needs to understand the language, be aware of libraries that they can leverage, and know how to effectively and efficiently debug complex C++ code.

This DAC tutorial will focus on specific aspects of application development in C++, with presentations by C++ experts from Cadence Design Systems and Undo Software. The session will cover template metaprogramming, event-driven programming, and advanced C++ debugging.

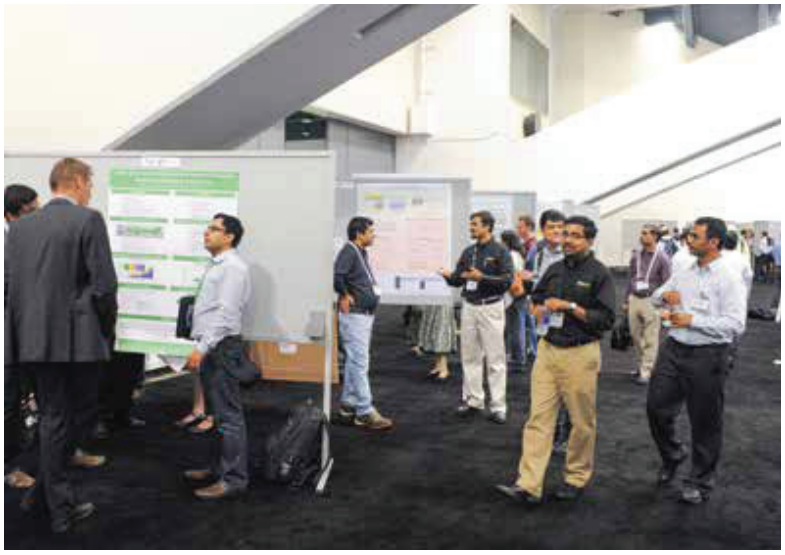
About the Speakers:
Tim Edwards, Software Director at Cadence Design Systems in Austin, has been developing software professionally since the early 90's. His early exposure to Tcl introduced him to the power of the event loop and the color bisque. He now focuses on distributed systems development at Cadence.

Finn Grimwood is a Senior Software Engineer at Undo Software. Having graduated with a MSci in Physical Natural Sciences from Cambridge University in 2011, Finn spent two years at Solarflare Communications working on high performance computer networking equipment.

John Croix, Senior Software Architect at Cadence Design Systems, has been writing C++ code since 1989, when C++ was translated into C and then compiled. He holds a PhD in Electrical and Computer Engineering from the University of Texas at Austin and MS in Computer Science from SMU.

SPEAKERS:
Tim Edwards - *Cadence Design Systems, Inc., Austin, TX*
Finn Grimwood - *Undo Software, Cambridge, United Kingdom*
John Croix - *Cadence Design Systems, Inc., Austin, TX*

DAC IS BACK IN SAN FRANCISCO FOR 2018!



JUNE 24-28, 2018
MOSCONE CENTER
SAN FRANCISCO, CA
DAC.COM

Visit us at booth #1528

EDACAFÉ

Visit EDACAFÉ at DAC 2017 in booth #1528, and be entered to win an Amazon Echo!

NEWS & TRENDS

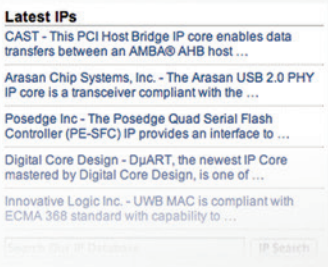
Latest news and industry trends.
Insightful editorial and blogs.

VIDEOS & TUTORIALS

Video interviews with key industry players.
Valuable video tutorials to help you learn.

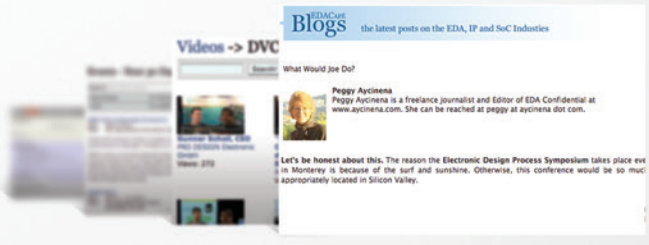
EDA & IP CATALOGS

Detailed information about thousands of commercially available IP blocks.



#1 EDA NEWSLETTER

EDACafe.com is the #1 web portal for Electronic Design Professionals. Visit our website today!



CONTACT US TO FIND OUT MORE

Address: 595 Millich Dr., Suite 216 , Campbell, CA 95008 Office: 1 (408) 337-6870 // www.EDACAFÉ.com

INTERNATIONAL WORKSHOP ON LOGIC & SYNTHESIS (IWLS)

Date: Saturday, June 17 || Time: 8:00am - 9:00pm || Room: Thompson Center
Event Type: Colocated Conference || Track: EDA, Design || Topic Area: Logic & High-Level Synthesis, Emerging Architectures & Technologies, Test & Verification

ORGANIZER:

Jie-Hong (Roland) Jiang - *National Taiwan Univ., Taipei, Taiwan*

The International Workshop on Logic & Synthesis (IWLS) is the premier forum for research in synthesis, optimization, and verification of integrated circuits and systems. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged. The workshop encourages early dissemination of ideas and results. The workshop accepts complete papers highlighting important new problems in the early stages of development, without providing complete solutions. The emphasis is on novelty and intellectual rigor

Topics of interest include, but are not limited to: hardware synthesis and optimization; software synthesis; hardware/software co-synthesis; power and timing analysis; testing, validation and verification; synthesis for reconfigurable architectures; hardware compilation for domain-specific languages; design experiences. Submissions on modeling, analysis and synthesis for emerging technologies and platforms are also encouraged.

The workshop format includes paper presentations, posters, invited talks, social lunch and dinner gatherings, and recreational activities. Accepted papers are distributed exclusively to IWLS participants.

ACM/IEEE SYSTEM LEVEL INTERCONNECT PREDICTION WORKSHOP (SLIP) 2017

Date: Saturday, June 17 || Time: 9:30am - 5:30pm || Room: 17AB
Event Type: Colocated Conference || Track: EDA, IoT || Topic Area: Simulation & Timing Analysis, Emerging Architectures & Technologies, NoC, Chip & Package Scale Interconnect

ORGANIZER:

Tsung-Yi Ho - *National Tsing Hua Univ., Hsinchu, Taiwan*

The general technical scope of the workshop is the design, analysis, prediction, and optimization of interconnect and communication fabrics in electronic systems.

CELUG/ESD ALLIANCE ENTERPRISE LICENSING CONFERENCE

Date: Tuesday, June 20 - Thursday, June 22 || Time: 8:00am - 5:00pm || Room: 9AB
Event Type: Colocated Conference || Track: EDA || Topic Area: General Interest

ORGANIZER:

Derek Magill - *Qualcomm, Inc., Austin, TX*

Tuesday, June 20 - 8:00am - 5:00pm
Wednesday, June 21 - 8:00am - 5:00pm
Thursday, June 22 - 8:00am - 12:00pm

EDA Licensing providers, ISVs, and Enterprise Customers will come together at an event colocated with the 54th ACM/ESD Alliance/IEEE Design Automation Conference (DAC), June 18-22, 2017, at the Austin Convention Center in Austin, Texas.

CELUG (Centralized Enterprise Licensing Users Group) and the Electronic System Design (ESD) Alliance are co-hosting this three-day event colocated at DAC 2017.

This interactive event will focus on Enterprise Licensing, with presentations and panels addressing current and future challenges to making high technology tools and users more productive. This colocated event will bring Licensing Solution Providers and Independent Software Vendors together with Enterprise Customers from key industries for interactive, face-to-face meetings.

CELUG Centralized Enterprise Licensing User Group

ADVANCED TECHNIQUES FOR MANAGING EDA WORKLOADS

Date: Wednesday, June 21 || Time: 9:30am - 5:00pm || Room: 10AB
Event Type: Colocated Conference || Track: EDA, Design || Topic Area: General Interest, Emerging Architectures & Technologies

ORGANIZER:

Peter Basmajian - *IBM Systems and Technology Group, Foster City, CA*
Gabor Samu - *IBM Systems Group, Markham, ON, Canada*

EDA data growth is challenging both traditional storage and data management solutions. Balancing workloads and data types puts pressure on administrators to deliver application performance and reduce bottlenecks.

Please join IBM at this complimentary annual workshop and learn how to bring EDA designs to market faster with improved performance, manageability and ease of use. Our technical experts will show you how to improve delivery schedules, increase EDA application performance and reduce bottlenecks that waste expensive resources.

You will hear directly from our developers about the latest features in IBM Spectrum™ LSF®, IBM Spectrum Scale™ and IBM® Aspera® Sync, while we demonstrate how you can improve operational efficiency.

Attend and you will learn how to:

- Optimize all resources including compute utilization and license management
- Maximize I/O and share data globally
- Reduce bottlenecks and maximize data transfer
- Synchronize big data globally over WANs
- Gain a competitive advantage through case studies from your peers

We will cover the following technologies in this free seminar:

IBM Spectrum LSF is a powerful workload management platform for demanding, distributed HPC environments. Join us for an update on the latest release of IBM Spectrum LSF family, including new capabilities improving usability, and support for new workloads including deep learning frameworks, and containers.

IBM Spectrum Scale simplifies data management by providing a single namespace that can grow quickly and infinitely by adding more scale-out resources – eliminating “filer sprawl”, single filer choke points, and enabling global collaboration and speeding data access.

IBM Aspera Sync quickly replicates and synchronizes big data globally over WANs—even if the data consists of millions of individual files or the largest size files. The software achieves maximum transfer speed regardless of file size, transfer distance and network conditions.

Agenda:

9:30-10:00am:	Registration
10:00-10:30am:	Welcome & Strategy Bill McMillan, Global Offering Manager, IBM Spectrum LSF Family
10:30-11:00am:	Driving Operational Efficiencies with IBM Spectrum LSF Family including Case Study: LSF & Ellexus Mistral @ ASML Larry Adams, Solution Architect, Auto/Aero/EDA, IBM Cognitive Systems
11:00-11:30am	Case Study: Using IBM Spectrum LSF Arthur Tseng, MediaTek
11:30am-12:00pm	Client Case Study: Cypress Semiconductor Addresses Filer Bottlenecks in HPC Infrastructure with IBM Spectrum Scale Dragomir Nikolic, CAD Director, Cypress Semiconductor Ken Halbrecht, CTO for HPC Platforms, Sycomp, Inc.
12:00-1:00pm:	Lunch and Networking
1:00-1:30pm:	Choosing a High Performance Parallel File Systems for EDA Workloads including Case Study at Cypress Semiconductor Chandra Mukhyala, Offering Manager, IBM File and Object Storage Stieg Klein, Systems Engineer, IBM Spectrum Storage
1:30-2:00pm:	Client Case Study: IBM Spectrum LSF & Jenkins Enables Rapid Delivery of Device Driver Software Brian Vandegriend, Product Verification Manager, Microsemi
2:00-2:30pm:	Using IBM Aspera Sync for Fast, Scalable, Multidirectional File Replication and Synchronization Jim Gallagher, Aspera Sales Engineer, IBM Hybrid Cloud
2:30-3:00pm:	Case Study: Using IBM Spectrum LSF to Efficiently Design Power and Z Microprocessors Leon Stok, Vice President, Electronic Design Automation, IBM Systems Michael Kazda, Software Architect, Electronic Design Automation, IBM Systems
3:00-3:15pm:	Break
3:15-5:00pm:	Round Table: What’s Next for IBM Spectrum LSF? Bill McMillan, Global Offering Manager, IBM Spectrum LSF Family & MPI

SPEAKER:

Bill McMillan - *IBM Corp., Hursely, United Kingdom*

A. RICHARD NEWTON YOUNG FELLOW PROGRAM WELCOME BREAKFAST & ORIENTATION

Date: Sunday, June 18 || Time: 7:30 - 9:00am || Room: 18CD
Event Type: Additional Meeting || Track: EDA || Topic Area: General Interest

The Newton Young Fellow Program is designed to assist young students at the beginning of a career in Electronic Design Automation and Embedded Systems. Each Newton Young Fellow will actively engage in DAC through a number of events including meetings with design automation luminaries, attendance at technical sessions and exhibits, participation in student-related events at DAC.

In addition, Newton Young Fellows will participate in a welcome orientation breakfast on Sunday morning, attend the Design Automation Summer School program, present posters of their academic/research work on Tuesday evening (colocated with the SIGDA Ph.D. Forum), and participate in a closing award ceremony for Young Fellows on Thursday evening.

Following a 50-year tradition, DAC strives to foster a vibrant and worldwide community of electronic design and embedded systems professionals; the fellowship actively supports and attempts to build an active cohort of the next generation of EDA and Embedded Systems professionals.

Welcome Breakfast and Orientation

Sunday, June 18
7:30 - 9:00am
Room: 18CD

Poster Presentation (colocated with the Ph.D. Forum)
Tuesday, June 20
7:00 - 9:00pm
Ballroom D

Closing Session and Award Ceremony
Thursday, June 22
6:00 - 6:45pm
Room: 12AB

Thank You to Our Sponsors

cadence® ACADEMIC NETWORK SYNOPSYS® Silicon to Software™

DESIGN AUTOMATION SUMMER SCHOOL

Date: Sunday, June 18 || Time: 9:00am - 6:00pm || Room: 18CD
Event Type: Additional Meeting || Track: IoT, Security || Topic Area: Codesign & System Design, Emerging Architectures & Technologies, Physical Design & DFM

ORGANIZERS:

Helen Li - *Duke Univ., Durnham, NC*
Yier Jin - *Univ. of Central Florida, Orlando, FL*
Muhammad Shafique - *Vienna Univ. of Technology, Vienna, Austria*

The Design Automation Summer School (DASS) is a one-day intensive course on research and development in design automation (DA). Each topic in this course will be covered by a distinguished speaker who will define the topic, describe recent accomplishments, and indicate remaining challenges. This program is intended to introduce and outline emerging challenges, and to foster creative thinking in the next generation of EDA engineers.

The 2017 SIGDA Design Automation Summer School is co-hosted by A. Richard Newton Young Fellowship Program at DAC. All the students receiving the fellowship (excluding the mentors) are required to attend DASS event.

For additional details go to: http://www.sigda.org/dass

Thank You to Our Sponsors

cadence® ACADEMIC NETWORK SIGDA SYNOPSYS® Silicon to Software™

ACM/IEEE EARLY CAREER WORKSHOP AT DAC

Date: Sunday, June 18 || Time: 12:00 - 9:00pm || Room: 18AB
Event Type: Additional Meeting || Track: Design, EDA || Topic Area: General Interest

ORGANIZERS:

Aviral Shrivastava - *Arizona State Univ., Tempe, AZ*
Andreas Gerstlauer - *Univ. of Texas at Austin, TX*
Rasit O. Topaloglu - *IBM Systems and Technology Group, Hopewell Junction, NY*
Elaheh Bozorgzadeh - *Univ. of California, Irvine, CA*
Peng Li - *Texas A&M Univ., College Station, TX*

This workshop is for young and mid-career faculty, and professionals in the field of electronic design automation (EDA). The workshop will be organized as presentations and panel discussions by EDA professionals, with additional opportunities to network with some of the established academicians, and professionals, and funding officers in the field of EDA. The themes this year include: Succeeding in Academic Job, thriving in industry, engaging in meaningful and impactful research, effective networking, and admirable teaching.

Thank You to Our Sponsors

GARY SMITH EDA AT ESD ALLIANCE KICKOFF SUNDAY NIGHT

Date: Sunday, June 18 || Time: 5:00 - 5:30pm || Room: Ballroom D
Event Type: Additional Meeting || Track: EDA || Topic Area: General Interest

Laurie Balch kicks off the annual ESD Alliance presentation.

Come hear the 28th annual update on the state of EDA by Laurie of Gary Smith EDA.

"EDA in the Age of the System"

This year's talk will discuss the challenges and opportunities facing EDA vendors as we enter an era increasingly focused on overall system design. How will the industry need to adjust and how can it best address the needs of electronic product developers? Where will EDA find its role in the broadening design landscape? What are the growth prospects for EDA vendors, including a view of the annual EDA forecast?

DAC reception immediately follows.

SPEAKER:
Laurie Balch - *Gary Smith EDA, Santa Clara, CA*

SYNOPSYS/ARM/TSMC BREAKFAST

Date: Monday, June 19 || Time: 7:15 - 8:45am || Room: Hilton Hotel, 6th Floor, Austin Grand Ballroom || Event Type: Additional Meeting || Track: EDA, Design
Topic Area: Physical Design & DFM

IEEE CEDA AUTHOR EDUCATION TALK "PUBLISHING WITHOUT PERISHING: A PERSPECTIVE"

Date: Monday, June 19 || Time: 10:00am - 12:00pm || Room: 12AB
Event Type: Additional Meeting || Track: EDA || Topic Area: General Interest

ORGANIZERS:

Yao-Wen Chang - *National Taiwan Univ., Taipei, Taiwan*
Helmut Graeb - *Technische Univ. München, Germany*

Most authors will agree that the process of publishing research can be beautiful and enriching as well as frustrating and annoying, sometimes simultaneously. So - what's an author to do?

Fortunately, we can use our technical skills to navigate this landscape. We will formulate the Promising Author Problem into an optimization framework that maximizes the joy while minimizing the agony. We will attempt to identify the optimization variables and classify them into deterministic and random components, and also into controllable and uncontrollable sets. We then model the cost function and constraints (graduation/tenure constraints, ethical issues, etc.) in terms of these variables and attempt to determine a trajectory that could maximize the probability of acceptance of your next paper. We have no theorems, no proofs of NP-hardness, no guarantees on feasibility, and no significant experimental results... but we hope this talk throws up some insights that might help you as you write your next paper.

SPEAKER:
Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

EDA POWERED BY MACHINE LEARNING

Date: Monday, June 19 || Time: 10:30 - 11:30am || Room: 10AB
Event Type: Additional Meeting || Track: EDA, Design || Topic Area: Low-Power & Reliability, Simulation & Timing Analysis

MODERATOR:

Amit Gupta - *Solido Design Automation, Inc., San Jose, Canada*

Machine Learning is making an enormous impact in a variety of fields, but how about EDA? Fast growing semiconductor market segments, including high-performance computing, automotive, mobile, and internet of things (IoT), are driving the need for electronic design automation (EDA) software tools to advance even more quickly in addressing increased complexity. Machine Learning has already started to play a major role in EDA, and has further opportunities to provide disruptive technology breakthroughs to address semiconductor challenges.

This panel discussion will focus on technologies and opportunities to address semiconductor challenges using machine learning. Examples will be covered on how machine learning technologies are already delivering disruptive runtime, resource, and productivity benefits, including areas such as variation-aware design and characterization.

PANELISTS:

Ting Ku - *NVIDIA Corporation, Santa Clara, CA*
Sorin Dobre - *Qualcomm, Inc., San Diego, CA*
Eric Hall - *Broadcom Corp., Bellevue, WA*
Jeff Dyck - *Solido Design Automation, Inc., Saskatoon, Canada*

SYNOPSYS AMS LUNCH: ACCELERATING ROBUST AMS DESIGN AT ADVANCED NODES

Date: Monday, June 19 || Time: 11:30am - 1:30pm || Room: Hilton Hotel, 6th Floor, Austin Grand Ballroom || Event Type: Additional Meeting || Track: EDA
Topic Area: Analog & Mixed-signal Design

The transition to advanced nodes has led to a significant increase in analog/mixed-signal (AMS) design size and complexity, exacerbated by worsening design conditions and stringent reliability requirements driven by emerging applications. These challenges translate to more exacting requirements for circuit simulators. At this lunch, designers will share their perspectives on the growing challenges at advanced nodes and discuss how they leverage Synopsys circuit simulation solutions to address these challenges to deliver robust AMS designs.

CADENCE LUNCHEON: TOWARDS SMARTER VERIFICATION

Date: Monday, June 19, 2017 || Time: 12:00pm - 1:30pm || Location: Ballroom BC
Event Type: Additional Meeting || Track: EDA || Topic Area: EMbedded System Software, Test & Verification, SoC & Embedded Systems Architectures

Formal verification, simulation, emulation, and FPGA-based prototyping are the core anchors to deliver verification productivity. While they continue to evolve and differentiate on parameters like performance, capacity, and memory footprint, the next leaps in productivity will be added in the fabric that binds them together with advanced analytics of the data created by the core engines. Smart switching between the engines to capitalize on their individual advantages, smart combination of engines to reap individual benefits, and advanced use models, flows, and methodologies combining the engines will provide the next step function in productivity. Learn more and register here.

SYNOPSYS IC COMPILER II LUNCH: ACHIEVING INDUSTRY-BEST QOR ON ADVANCED DESIGNS

Date: Monday, June 19 || Time: 11:30am - 1:30pm || Room: Hilton Hotel, 6th Floor, Austin Grand Ballroom || Event Type: Additional Meeting || Track: EDA, Design
Topic Area: Physical Design & DFM

Hear how industry leaders are achieving success in their advanced designs using IC Compiler II. Leading customers will share their experiences using IC Compiler II technology to address physical design challenges and accelerate products to market.

COOLEY'S DAC TROUBLEMAKER PANEL

Date: Monday, June 19 || Time: 3:00 - 4:00pm || Room: 10AB
Event Type: Additional Meeting || Track: EDA || Topic Area: General Interest

MODERATOR:

John Cooley - *Deepchip, Holliston, MA*
Come watch the EDA troublemakers answer the edgy, user-submitted questions about this year's most controversial issues! It's an old style open Q&A from the days before corporate marketing took over every aspect of EDA company images.

PANELISTS:

Joe Sawicki - *Mentor, A Siemens Business, Wilsonville, OR*
Anirudh Devgan - *Cadence Design Systems, Inc., Austin, TX*
Dean Drako - *IC Manage, Inc., Campbell, CA*
Amit Gupta - *Solido Design Automation, Inc., San Jose, Canada*
Prakash Narain - *Real Intent, Inc., Sunnyvale, CA*
Jim Hogan - *Vista Ventures, Louisville, CO*

SYNOPSYS/SAMSUNG FOUNDRY BREAKFAST

Date: Tuesday, June 20 || Time: 7:15 - 8:45am || Room: Hilton Hotel, 6th Floor, Austin Grand Ballroom || Event Type: Additional Meeting || Track: EDA, Design
Topic Area: Physical Design & DFM

Attend this breakfast presentation to learn how Samsung Foundry and Synopsys are enabling mutual customers to meet advanced SoC designs needs.

SYNOPSYS CUSTOM COMPILER LUNCH: CUTTING FINFET LAYOUT TASKS FROM DAYS TO HOURS

Date: Tuesday, June 20 || Time: 11:30am - 1:30pm || Room: Hilton Hotel, 6th Floor, Austin Grand Ballroom || Event Type: Additional Meeting || Track: EDA, Design
Topic Area: SoC & Embedded System Architectures, Analog & Mixed-signal Design

FinFET devices have added significant complexity to the design flow, and many companies are seeking new solutions for custom design. During this lunch, customers will present their experiences with the challenges of FinFET custom design, and will discuss how they have deployed Synopsys Custom Compiler to improve their custom design productivity for FinFET.

SYNOPSYS VERIFICATION LUNCH: SOC LEADERS VERIFY WITH SYNOPSYS

Date: Tuesday, June 20 || Time: 11:30am - 1:30pm || Room: Hilton Hotel, 6th Floor, Austin Grand Ballroom || Event Type: Additional Meeting || Track: EDA
Topic Area: Test & Verification

Synopsys will highlight next-generation verification technologies as well as discussions about the latest developments in the verification landscape and advanced technology trends. In addition, a panel of industry experts will share their viewpoints on what is driving SoC complexity, how their teams have achieved success and how you can apply their insights on your next project.

ACM TODAES EDITORIAL BOARD MEETING

Date: Tuesday, June 20 || Time: 12:00 - 2:00pm || Room: 10C || Event Type: Additional Meeting || Track: Design, Embedded Systems || Topic Area: Low-Power & Reliability, Test & Verification

ORGANIZER:

Annie Yu - *Univ. of Southern California, Los Angeles, CA*

Annual meeting of the ACM TODAES Editorial Board

IEEE CEDA DISTINGUISHED SPEAKER LUNCHEON: COMPUTER ARCHITECTURE AND DESIGN: LOOKING BACK, PROJECTING FORWARD

Date: Tuesday, June 20 || Time: 12:00 to 1:30pm || Room: Ballroom D
Event Type: Additional Meeting || Track: Design, EDA
Topic Area: Test & Verification, Logic & High-Level Synthesis

To begin the talk I will tell the story of a hardware prototype we implemented early in my career when CMOS was the new technology and Moore's Law was full steam ahead. The prototype was an application specific signal processor we named the Arithmetic Cube, which took place in the mid 1980's to the early 1990's, and which required the design and implementation of a number of design tools. This was my first, but not last, foray into the EDA world. I will briefly describe both the architecture of the Arithmetic Cube and the EDA tools we developed for it. Among the lessons learned during this period was "Let the needs of the design drive the design tool development," something that those in the EDA industry innately understand as driven by their customers' needs but something that can be a challenge for academics since it means that one must juggle two research thrusts at the same time. The second portion of the talk will project forward into several new technology spaces beyond Moore's Law to see how the lessons learned during the design of the Arithmetic Cube in the early days of CMOS can help guide architecture design and design tools research and development in the future.

Biography: Mary Jane Irwin has been on the faculty at Penn State since 1977 where she currently holds the title of Evan Pugh Professor and A. Robert Noll Chair in Engineering in the Department of Computer Science and Engineering. Her research and teaching interests include computer architecture, embedded and high performance computing systems design, power and reliability aware design, and emerging technologies in computing systems. Dr. Irwin received her Ph.D. from the University of Illinois in 1977 and an Honorary Doctorate from Chalmers University, Sweden, in 1997. She was named a Fellow of The Institute of Electrical and Electronic Engineers (IEEE) in 1995, a Fellow of The Association for Computing Machinery (ACM) in 1996, and was elected to the National Academy of Engineering in 2003 and to the American Academy of Arts and Sciences in 2009.

SPEAKER:

Mary Jane Irwin - *Pennsylvania State Univ., State College, PA*

CEDA
IEEE Council on Electronic Design Automation

CADENCE LUNCHEON: HIGH-PERFORMANCE DIGITAL DESIGN AT 7N

Date: Tuesday, June 20, 2017 || Time: 12:00pm to 1:30pm || Location: Ballroom BC
Event Type: Additional Meeting || Registration Type: Designer/IP Special, One Day Only Available, I Love DAC, Conference || Track: EDA || Topic Area: Digital Design, Simulation & Timing Analysis

Designing at 7nm while simultaneously pushing power, performance, and area (PPA) requirements for new high-performance computing (HPC) and mobile platforms requires extensive industry collaboration. Experts from TSMC, Cadence and SoC design teams will discuss how to successfully take on these new requirements and benefit from the performance and efficiency improvements that 7nm offers. The panel will discuss the readiness of the process node, IP ecosystem, and Cadence digital flow for confidently supporting advanced 7nm design starts.

SIGDA BOARD MEETING

Date: Tuesday, June 20 || Time: 2:00 - 4:00pm || Room: 10C
Event Type: Additional Meeting || Track: EDA || Topic Area: General Interest

The SIGDA Board Meeting is open to SIGDA Executive Committee members and event organizers only. Past activities and future directions will be discussed for SIGDA at this meeting.

SYNOPSYS/GLOBAL FOUNDRIES DINNER: ADVANCED DESIGN ENABLEMENT AND ECOSYSTEM READINESS OF GLOBALFOUNDRIES DUAL ROADMAP TECHNOLOGIES, USING THE SYNOPSYS DESIGN PLATFORM

Date: Tuesday, June 20 || Time: 6:15 - 8:15pm || Room: Hilton Hotel, 6th Floor, Austin Grand Ballroom || Event Type: Additional Meeting || Track: EDA, IoT Topic Area: Physical Design & DFM, Emerging Architectures & Technologies

GLOBALFOUNDRIES and Synopsys share details of their collaboration on enablement and ecosystem readiness, using the Synopsys Design Platform to achieve optimal results on GLOBALFOUNDRIES' leading edge dual roadmap process technologies.

BIRDS-OF-A-FEATHER MEETINGS

Date: Tuesday, June 20 || Time: 7:00 - 8:30pm || Room: Various
Event Type: Additional Meeting || Track: EDA || Topic Area: General Interest

DAC will provide conference rooms for informal groups to discuss items of common technical interest. These very informal, non-commercial meetings, held after hours, are referred to as "Birds-Of-A-Feather" (BOF).

All BOF meetings are held at the Austin Convention Center, Tuesday, June 20 from 7:00 - 8:30pm.

To arrange a BOF Meeting, please click here to fill out the form. Please send the completed form to Corinne Nichols at corinne@dac.com.

ACM SIGDA AND IEEE CEDA PH.D. FORUM

Date: Tuesday, June 20 || Time: 7:00 - 9:00pm || Room: Ballroom D
Event Type: Additional Meeting || Track: EDA || Topic Area: General Interest

ORGANIZER:

Yiyu Shi - *Univ. of Notre Dame, IN*

The Ph.D. Forum at the Design Automation Conference is a poster session hosted by ACM SIGDA and IEEE CEDA for senior Ph.D. students to present and discuss their dissertation research with people in the EDA community. Participation in the forum is highly competitive with acceptance rate of around 30%. The forum is open to all members of the design automation community and is free-of-charge.

For more information, please visit ACM/IEEE SIGDA Ph.D. Forum website.

29TH ACM SIGDA UNIVERSITY DEMONSTRATION

Date: Tuesday, June 20 || Time: 7:00 - 9:00pm || Room: Ballroom D
Event Type: Additional Meeting || Track: EDA || Topic Area: General Interest

This year marks the 29th University Demonstration at the Design Automation Conference. UD is an opportunity for university researchers to display their results and to interact with participants at DAC. Presenters and attendees at DAC are especially encouraged to participate, but participation is open to all members of the university community. The demonstrations include new EDA tools, EDA tool applications, design projects, and instructional materials.

For decades, DAC has encouraged the contributions and participation of graduate and undergraduate students globally. For further details please visit the Students & Scholarships page.

Booth Coordinators

Chair: Sudeep Pasricha - *Colorado State Univ., Fort Collins, CO*
Vice Chair: Qi Zhu - *Univ. of California, Riverside, CA*
Publicity Chair: Anup Kumar Das - *IMEC, Peoria, IL*

SYNOPSYS/INTEL CUSTOM FOUNDRY BREAKFAST

Date: Wednesday, June 21 || Time: 7:15 - 8:45am || Room: Hilton Hotel, 6th Floor, Austin Grand Ballroom || Event Type: Additional Meeting || Track: EDA, IoT Topic Area: Physical Design & DFM, Emerging Architectures & Technologies

LUNCH'N'LEARN: PYTHON FOR SCIENTIFIC COMPUTING AND MACHINE LEARNING

Date: Wednesday, June 21, 2017 || Time: 12:15pm to 1:15pm || Location: Ballroom D
Event Type: Additional Meeting || Registration Type: Additional Registration Required, Conference, Designer/IP Special, One Day Only Available || Track: EDA, Design
Topic Area: Emerging Architectures & Technologies, General Interest, Test & Verification

'Thursday is Training Day' comes to Wednesday with this special Lunch 'n' Learn from Doulos.

Attendance is FREE. Space is Limited!

Box lunch kindly sponsored by Synopsys

Attendees also receive a $25 discount coupon for 'Thursday is Training Day'

As well as being a general purpose programming and scripting language, Python has become one of the most popular languages for scientific computing and more recently for machine learning. Python is everywhere, and Python is cool. Python is easy to learn and Python programs are very readable, even by people who don't know Python. There are Python libraries available for doing pretty much anything.

In this tutorial you will learn enough Python to start using Python libraries such as NumPy and Matplotlib that are widely used in scientific computing, and you will become sufficiently familiar with Python to start making sense of the emerging libraries and frameworks being used for deep learning, such as TensorFlow, Keras, and Caffe. This tutorial will show you some of the really cool things you can do with Python right out-of-the-box!

More on the Python language will be taught in the afternoon session on 'Thursday is Training Day'.

Thank You to Our Sponsor

DOULOS

CADENCE LUNCHEON: OVERCOMING MIXED-SIGNAL DESIGN AND VERIFICATION CHALLENGES IN AUTOMOTIVE AND IOT SYSTEMS

Date: Wednesday, June 21, 2017 || Time: 12:00pm to 1:30pm || Location: Ballroom BC
Event Type: Additional Meeting || Registration Type: One Day Only Available, Designer/IP Special, Conference, I Love DAC || Track: EDA, IoT
Topic Area: Analog & Mixed-signal Design, Codesign & System Design

The Internet of Things (IoT) is transforming our daily lives, particularly with the increasing popularity in connected cars over the past few years. As IoT devices in cars rely more on sensors for connectivity, methodologies to address and mitigate reliability challenges, as well as accurate reliability analysis, become mandatory to ensure that these devices continue to function correctly over time. In addition, miniaturization of IoT devices requires heterogeneous integration across chips of all process technologies down to 7nm, packages, and board. Learn how industry experts overcome these design and verification challenges.

A. RICHARD NEWTON YOUNG FELLOW PROGRAM CLOSING SESSION & AWARD CEREMONY

Date: Thursday, June 22 || Time: 6:00 - 6:45pm || Room: 12AB
Event Type: Additional Meeting || Track: EDA || Topic Area: General Interest

The Newton Young Fellow Program is designed to assist young students at the beginning of a career in Electronic Design Automation and Embedded Systems. Each Newton Young Fellow will actively engage in DAC through a number of events including meetings with design automation luminaries, attendance at technical sessions and exhibits, participation in student-related events at DAC.

In addition, Newton Young Fellows will participate in a welcome orientation breakfast on Sunday morning, attend the Design Automation Summer School program, present posters of their academic/research work on Tuesday evening (colocated with the SIGDA Ph.D. Forum), and participate in a closing award ceremony for Young Fellows on Thursday evening.

Following a 50-year tradition, DAC strives to foster a vibrant and worldwide community of electronic design and embedded systems professionals; the fellowship actively supports and attempts to build an active cohort of the next generation of EDA and Embedded Systems professionals.

Closing Session and Award Ceremony
Thursday, June 22
6:00 - 6:45pm
Room: 12AB

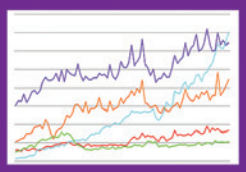
Thank You to Our Sponsors

cadence ACADEMIC NETWORK

SYNOPSYS® Silicon to Software™

Electronic System Design Alliance™

Representing the semiconductor design ecosystem



JOIN US!

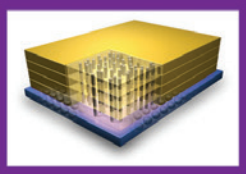
The *Electronic System Design Alliance* provides a platform for member companies to address technical, marketing, economic and legislative issues affecting the entire industry. We also provide networking events and targeted programs to assist emerging companies in the design ecosystem.

ESD Alliance committees and working groups focus on critical issues that affect the design ecosystem including -- Export Regulations, License Management & Anti-Piracy, Market Statistics Service, O/S Interoperability, Emerging Companies, IP Tracking & Auditing and Trade Shows.

The ESD Alliance is a proud sponsor of the Design Automation Conference (DAC) and Design and Test in Europe (DATE).

IP Fingerprinting

This working group is bringing together IP vendors and users to develop a common methodology and best practices for IP fingerprinting -- a technology that provides a solution to efficient IP auditing.



Advanced Packaging

Download the Multi-Die IC User Guide from the ESD Alliance web site. It is a comprehensive document covering design tools, IP, materials, services, market information, and more.

Phil Kaufman Award

The ESD Alliance, in cooperation with the IEEE Council on EDA (CEDA), is proud to present the annual Phil Kaufman Award honoring an individual who has had demonstrable impact on electronic design. Submit nominations at esd-alliance.org.

Join the Electronic System Design Alliance

For more information about the benefits of membership, visit esd-alliance.org or email us at info@esd-alliance.org.

EDA INDUSTRY TRENDS AND WHAT'S HOT AT DAC

Date: Monday, June 19 || Time: 10:30 - 11:00am || Room: DAC Pavilion
Event Type: DAC Pavilion || Track: Design, EDA || Topic Area: General Interest

In longstanding Gary Smith EDA tradition, EDA Chief Analyst Laurie Balch of Gary Smith EDA will share her views on the latest directions for the EDA technology and business fronts. What new trends are facing the EDA, semiconductor and design communities and how will they impact you? What are the hot 'must see' products at this year's conference? How can you prepare for the future of electronics design? Plus, get a rundown of the annual Gary Smith EDA Sunday night kickoff talk.

SPEAKER:

Laurie Balch - *Gary Smith EDA, San Jose, CA*

ONE-ON-ONE: LIP-BU TAN: CHAIRMAN AND CEO, CADENCE DESIGN SYSTEMS

Date: Monday, June 19 || Time: 11:30am - 12:15pm || Room: DAC Pavilion
Event Type: DAC Pavilion || Track: EDA || Topic Area: General Interest

MODERATOR:

Ed Sperling - *Semiconductor Engineering, San Jose, CA*

Cadence's CEO shares insights about big changes in the data center and end markets, the rise of machine learning, growing challenges in system design, and what to watch for in China, in a lively discussion with Semiconductor Engineering Editor In Chief Ed Sperling.

SPEAKER:

Lip-Bu Tan - *Cadence Design Systems, Inc., San Jose, CA*

SKY TALK: CHINA'S IC INDUSTRY: TODAY AND TOMORROW - ITS INFLUENCE ON GLOBAL DESIGN AND DESIGN AUTOMATION COMMUNITY

Time: 1:00 - 1:25pm || Room: DAC Pavilion || Event Type: SKY Talk
Track: Design, EDA || Topic Area: General Interest

ORGANIZER:

Sharon Hu - *Univ. of Notre Dame, IN*

When China announced its national plan to promote its native IC industry, this raised many questions. With its rapid growth, China's IC industry is becoming an emerging force globally, increasing the importance of understanding the answers to these questions. Few people really understand China's IC industry. For example, what is the real state of the China's IC industry today, what implications does such a promotion have to the global IC, EDA and other related industries, and what goals are China's IC industry working to achieve?

This presentation will give an overview of the Chinese IC market, followed by an introduction of China's IC industry with an emphasis on fabless companies. China's native products, design technologies, and talents will be described in detail to provide an objective and comprehensive picture of China's IC industry. In addition, China's current status in design automation technology and indigenous EDA companies will be discussed.

As China is a unique country with huge population, vast territory, rapidly growing but unbalanced economy, and many diverse cultures, life-styles and traditions, its native product demands are also diverse. How to meet these drastically different requirements with a reasonable time to market while keeping costs low presents a big challenge. A rapidly growing IC industry in China will force design and EDA engineers, both inside and outside China, to explore, to innovate as well as to collaborate. With a large talent pool addressing unique challenges, who can say there will not be new technologies, methodologies and products emerging to change the rules of the global information technology landscape?

SPEAKER:

Shaojun Wei - *Tsinghua Univ., Beijing, China*

FUTURE CAST: WHERE ELECTRONICS DESIGN IS HEADED THROUGH THE EYES OF THE UNDER 40 INNOVATOR AWARD WINNERS

Date: Monday, June 19 || Time: 3:00 - 3:45pm || Room: DAC Pavilion
Event Type: DAC Pavilion || Track: EDA || Topic Area: General Interest

MODERATOR: Dylan McGrath - *EE Times, San Francisco, CA*

ORGANIZER: Michelle Clancy - *Cayenne Communications, Sunnyvale, CA*

This panel will honor the five recipients of DAC's New Under 40 Innovator Award Winners. Panelist will discuss where they see the future of electronic design, the current trends and new markets that may or may not be a factor in the next decade. Winners will be announced Monday, June 19 at the General Session.

IFIXIT NINTENDO SWITCH TEARDOWN

Date: Monday, June 19 || Time: 4:30 - 5:00pm || Room: DAC Pavilion
Event Type: DAC Pavilion || Track: Embedded Systems || Topic Area: General Interest

The moment you've all been waiting for: Nintendo has finally released a brand new Zelda game! And, incidentally, a new console to play it on—the Switch. Join iFixit, the world's foremost experts on teardowns and repair, for a legendary adventure through the depths of this handheld/console hybrid. They'll tear through the system to expose the tech and rate its repairability.

SPEAKERS:

Evan Noronha - *iFixit, San Luis Obispo, CA*
Scott Havard - *iFixit, San Luis Obispo, CA*

SIP TRENDS

Date: Tuesday, June 20 || Time: 10:30 - 11:00am || Room: DAC Pavilion
Event Type: DAC Pavilion || Track: IoT || Topic Area: General Interest

ORGANIZERS:

Linda Bal - *TechSearch International, Inc., Austin, TX*
Jan Vardaman - *TechSearch International, Inc., Austin, TX*

Smartphones remain one of the main applications for system-in-package (SiP) volumes, but the growing demand for connectivity is resulting in new SiP designs for a variety of products ranging from wearables to high-performance computing to automotive electronics. This presentation examines the drivers for these applications and the formats are being adopted. SiP is defined as a functional system or subsystem assembled into a standard footprint package such as LGA, FBGA, QFN, FO-WLP, or a module with a silicon, glass, or laminate interposer. It contains two or more dissimilar die, typically combined with other components such as passives, filters, MEMS, sensors, and/or antennas. The components are mounted together on a substrate to create a customized, highly integrated product for a given application. SiPs may utilize a combination of advanced packaging including bare die (wire bond or flip chip), wafer level packages, pre-packaged ICs such as CSPs, stacked packages, stacked die, or any combination of these. In some cases the package may be an embedded die solution.

The critical role of design in each application is addressed.

SPEAKER:

Dick James - *TechSearch International, Inc., Austin, TX*

ONE-ON-ONE: AART DE GEUS: CHAIRMAN AND CO-CHIEF EXECUTIVE OFFICER - SYNOPSYS, INC.

Date: Tuesday, June 20 || Time: 11:30am - 12:15pm || Room: DAC Pavilion
Event Type: DAC Pavilion || Track: EDA || Topic Area: General Interest

MODERATOR:

Ed Sperling - *Semiconductor Engineering, San Jose, CA*

Synopsys' chairman and co-CEO talks with Semiconductor Engineering Editor In Chief Ed Sperling about the rise of "smart" everything—the third generation of electronics. What are the drivers, the important trends, and the future possibilities for the silicon-to-software ecosystem.

SPEAKER:

Aart de Geus - *Synopsys, Inc., Mountain View, CA*

SKY TALK: EXPLORING THE CONNECTIONS BETWEEN THE DIGITAL WORLD AND PHYSICAL WORLD WITH SIMON SEGARS AND LUCIO LANZA

Time: 1:00 - 1:25pm || Room: DAC Pavilion || Event Type: SKY Talk
Track: IoT, Design || Topic Area: Digital Design, Analog & Mixed-signal Design, Emerging Architectures & Technologies

MODERATOR:

Ed Sperling - *Semiconductor Engineering, San Jose, CA*

DAC attendees are invited to join industry luminaries Simon Segars and Lucio Lanza in a lively, far-reaching conversation about the Internet of Things, and how the digital world will be connected with the physical world. Expect an analysis of the variety of new components required — far more than the industry is accustomed to — to support the emerging analog/mixed-signal phenomenon. They will consider how to meet these challenges, why the design ecosystem needs to be reinvented as well as why design and device costs must be reduced to meet a reasonable target. Attendees can expect to hear about new compute models and architectures, smaller processors and how an IoT infrastructure can be secured. The conversation will conclude with a few intriguing predictions on the biggest trends, along with the dreams of how to shape the IoT wave.

SPEAKERS:

Simon Segars - *ARM Ltd., Cambridge, United Kingdom*
Lucio Lanza - *Lanza TechVentures, Palo Alto, CA*

ARTIFICIAL INTELLIGENCE AND CONVOLUTION NEURAL NETWORKS

Date: Tuesday, June 20 || Time: 3:00 - 3:45pm || Room: DAC Pavilion
Event Type: DAC Pavilion || Track: IoT || Topic Area: General Interest

MODERATOR:

Jim Hogan - *Vista Ventures, Los Gatos, CA*

Today lots of companies are building systems that gather data and automatically process this to drive parts of their business operations. Obvious cases are Amazon telling you at point of sale, “Other people who bought XYZ shoes purchased ABC socks and ZXY shoe polish”. We are move deeper into this new world at a blinding pace. Listen to Jim discuss with industry experts what can be done in this area, what we should be worried about, and where it is all going.

PANELISTS:

Chris Rowen - *Cognite Ventures, Santa Cruz, CA*
James Gambale - *Lomasoft Corp., San Diego, CA*
Raik Brinkmann - *OneSpin Solutions GmbH, San Jose, CA*

IFIXIT GOPRO KARMA DRONE TEARDOWN

Date: Tuesday, June 20 || Time: 4:30 - 5:00pm || Room: DAC Pavilion
Event Type: DAC Pavilion || Track: Embedded Systems || Topic Area: General Interest

Last year GoPro’s airborne camera division took flight. Unfortunately, the takeoff was rather turbulent as the Karma Drone had a tendency to fall out of the sky. So, they took it back to the drawing board and re-released the Karma Drone in February. Come hang out with iFixit Teardown Extraordinaires as they rip this revamped drone apart to assess if pilots can expect smooth sailing, and how easy it will be to fix the damaged craft after you “didn’t see that tree.”

SPEAKERS:

Evan Noronha - *iFixit, San Luis Obispo, CA*
Scott Havard - *iFixit, San Luis Obispo, CA*

IS INTEGRATION LEAVING LESS ROOM FOR DESIGN INNOVATION?

Date: Wednesday, June 21 || Time: 10:30 - 11:00am || Room: DAC Pavilion
Event Type: DAC Pavilion || Track: IoT || Topic Area: Emerging Architectures & Technologies, SoC & Embedded System Architectures, Codesign & System Design

Is all the differentiation gone in hardware product design? Not too long ago, product engineers chose the components they needed to design a functional system – CPUs, cache and working memory, non-volatile memory and storage, system interconnect, offload accelerators, peripheral interfaces, and sensors. Modern System-on-Chip (SoC) designs integrate most of those design choices, while new packaging techniques integrate best of class manufacturing process choices for logic, memory, human interface (tactile, audio, and visual), communications (wired and wireless), and sensors. Unless you can fund your own chip design, it is by far cheaper to select off-the-shelf SoCs pre-packaged for specific application classes in multi-chip modules. The question then becomes – how do you differentiate your IoT widget?

What's left for product designers other than choosing the right integration level at the right price point, size, and power consumption? Seriously? Your product is now part of a service, it's a key piece of the behavior of systems-of-systems, but so are security architecture, network architecture, data ingress and storage, analytics, and machine learning. This presentation will discuss the impacts of SoC and systems-of-systems architecture on product design and differentiation.

SPEAKER:

Paul Teich - *TIRIAS Research, Austin, TX*

ONE-ON-ONE: WALLY RHINES: CHAIRMAN AND CHIEF EXECUTIVE OFFICER - MENTOR, A SIEMENS BUSINESS

Date: Wednesday, June 21 || Time: 11:30am - 12:15pm || Room: DAC Pavilion
Event Type: DAC Pavilion || Track: EDA || Topic Area: General Interest

MODERATOR:

Ed Sperling - *Semiconductor Engineering, San Jose, CA*

Wally Rhines, CEO of Siemens' Mentor Graphics business unit, talks with Semiconductor Engineering Editor In Chief Ed Sperling about major changes in design and EDA, including the fallout from semiconductor mergers, growth of electronic system design, and the IoT and IIoT.

SPEAKER:

Wally Rhines - *Mentor, A Siemens Business, Wilsonville, OR*

SKY TALK: POWER ELECTRONICS WITH VERTICAL GAN DEVICES

Time: 1:00 - 1:25pm || Room: DAC Pavilion || Event Type: SKY Talk
Track: Embedded Systems || Topic Area: Analog & Mixed-signal Design, Low-Power & Reliability, General Interest

ORGANIZER:

Michael 'Mac' McNamara - *Adapt-IP, Palo Alto, CA*

Electronic systems have become an indispensible part of our daily lives. All electronics devices have to convert AC (alternating current) that is available from the wall sockets into DC (direct current) to run the integrated circuits that define their functionality. This conversion is typically done by a switch mode power supply (SMPS) that was a major breakthrough in the 1980s, and has lead to the proliferation of electronics systems.

At the heart of an SMPS is a high voltage silicon power transistor. Unfortunately, silicon is not the best semiconductor for high voltage (HV) devices. Silicon based Super Junction (SJ) MOSFETs achieve up to 600V. Higher voltages in silicon are realized with Insulated Gate Bipolar Transistors (IGBTs). IGBT's switching frequency tops off at 20kHz while HV SJ MOSFETs top off at 200kHz. Switching frequency freezes the efficiency and size of any SMPS.

III-V compound semiconductors such silicon carbide (SiC) or Gallium Nitride (GaN) are much better suited for high voltage power transistors. NexGen Power Systems has demonstrated vertical GaN Junction Field Effect Transistor (JFETs). We have demonstrated vertical JFETs operating at 1200V, passing the JDEC device reliability requirements, and switching at 1MHz. These devices have extremely low Coss and Qrr. We have also demonstrated working converter systems with vertical GaN devices. Further, we have shown the breakdown voltages for these vertical devices can scale up to 4000V and they can sink up to 400A of current.

This talk will compare the NexGen Power Systems vertical GaN devices with other devices in the market and show their impact on power applications such data centers, motor drives and photovoltaic inverters.

SPEAKERS

Dinesh Ramanathan - *NexGen Power Systems, Inc., Cupertino, CA*

INTERNATIONAL HARDWARE DESIGN CONTEST AWARD CEREMONY

Date: Wednesday, June 21 || Time: 3:00 - 3:45pm || Room: DAC Pavilion
Event Type: DAC Pavilion || Track: || Topic Area: General Interest

DAC will present the Hack@DAC and FPGA Design Contest Awards.

Hack@DAC: Participating teams in this contest try to mimic the behavior of a malicious or secure-unaware CAD engineer. Their objective is to show that reasonable modifications to CAD algorithms can have unintended security consequences.

FPGA Design Contest: As this is largely an open-ended design contest, each submitted design will be evaluated by a panel of judges formed by experts from both industry and academia according to the creativity of the design. Feedback from the panel will be provided to each team. Evaluation will be a combination of positive points, awarded to the design functionality, innovation, and repeatability, easiness for implementation, robustness and security.

IFIXIT IPHONE 7 TEARDOWN

Date: Wednesday, June 21 || Time: 4:30 - 5:00pm || Room: DAC Pavilion
Event Type: DAC Pavilion || Track: Embedded Systems || Topic Area: General Interest

Apple has finally delivered their first water-resistant iPhone, but with more ingress protection comes less… headphone jack? There's only one way to find out what's filling the void where analog output once reigned supreme. Join iFixit as they tear down the iPhone and try to answer exactly what all the "courage" is that Apple's been talking about.

SPEAKERS:

Evan Noronha - *iFixit, San Luis Obispo, CA*
Scott Havard - *iFixit, San Luis Obispo, CA*

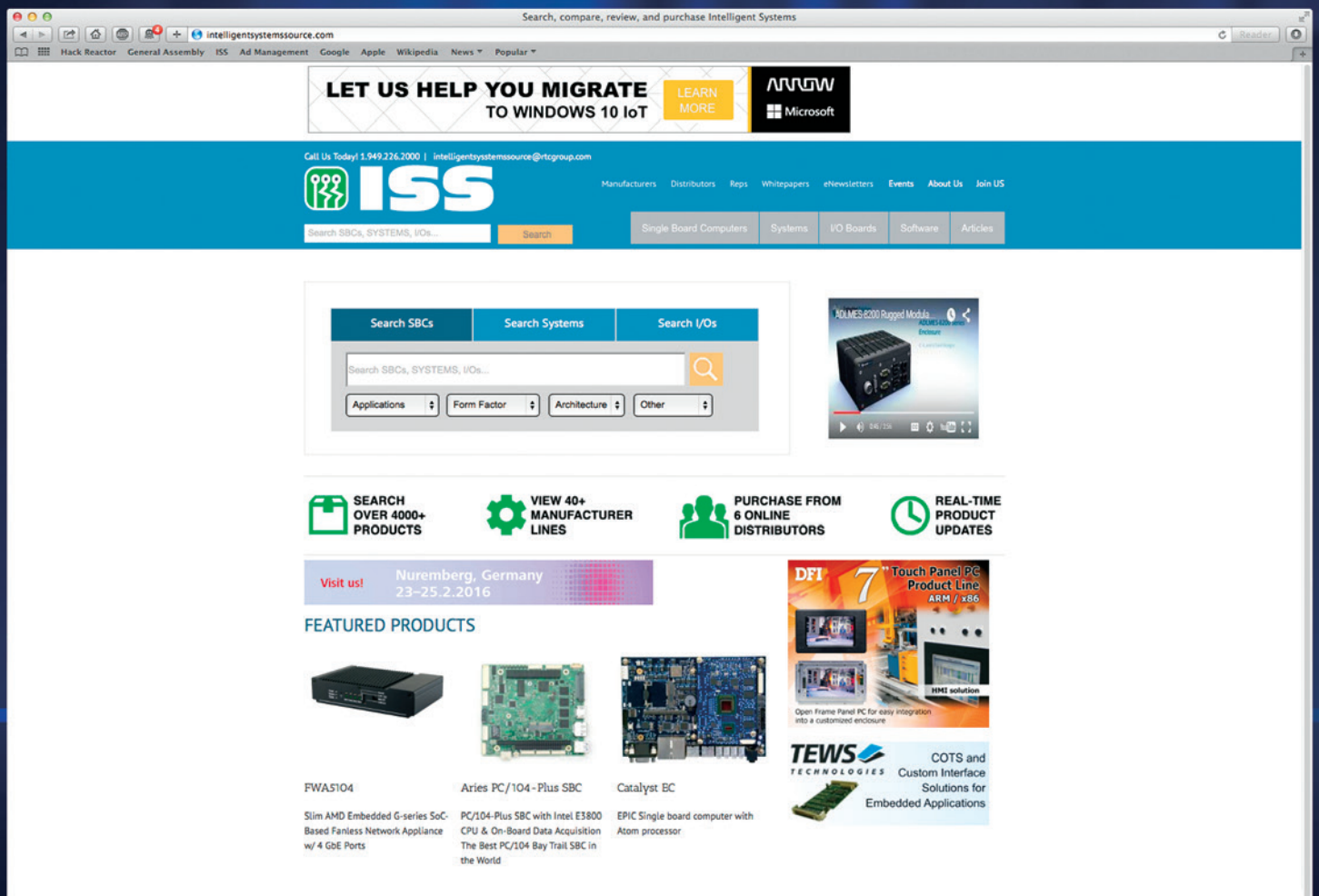
Why Should Researching SBCs Be More Difficult Than Car Shopping?

Today's systems combine an array of very complex elements from multiple manufactures. To assist in these complex architectures, ISS has built a simple tool that will source products from an array of companies for a side by side comparison and provide purchase support.

INTELLIGENTSYSTEMSSOURCE.COM is a purchasing tool for Design Engineers looking for custom and off-the-shelf SBCs and system modules.

ISS

INTELLIGENTSYSTEMSSOURCE.COM



EXECUTIVE COMMITTEE

General Chair
Michael 'Mac' McNamara
Adapt-IP
mac@adapt-ip.com

Vice Chair
X. Sharon Hu
Univ. of Notre Dame
shu@nd.edu

Past Chair
Charles Alpert
Cadence Design Systems, Inc.
alpert@cadence.com

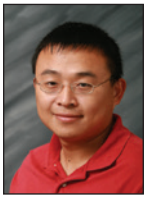
Program Chair
Robert Aitken
ARM, Inc.
rob.aitken@arm.com

Technical Program Chair
Valeria Bertacco
Univ. of Michigan
valeria@dac.com

Special Sessions Chair
Anand Raghunathan
Purdue Univ.
raghunathan@purdue.edu

Panel Chair / Security Chair
Ramesh Karri
New York University
rkarri@nyu.edu

Tutorial Chair
Ramond Rodriguez
Intel Corp.
ramond.rodriguez@intel.com



Designer Track Chair
Zhuo Li
Cadence Design Systems, Inc.
zhuoli@cadence.com

Designer Track Systems Chair
Robert Oshana
NXP Semiconductors
Robert.oshana@nxp.com

Designer Track Silicon Chair
Steve Padnos
Consultant
spadnos@yahoo.com

Designer Track Verification Chair
Harry Foster
Mentor, A Siemens Business
harry_foster@mentor.com

IP Track Chair
Claude Moughanni
Lattice Semiconductor
Claude.Moughanni@latticesemi.com

Finance Chair
Patrick Groeneveld
dac@groeneveld.us

Industry Advisory Chair
Rob van Blommestein
S2C Inc.
robvb@s2cinc.com

Publicity Chair
Michelle Clancy
Cayenne Communication
michelle.clancy@cayennecom.com

Outreach Chair
Naehyuck Chang
Korea Advanced Institute of Science and Technology
naehyuck@cad4x.kaist.ac.kr

ACM Representative
Vijaykrishnan Narayanan
Pennsylvania State Univ.
vxn9@cse.psu.edu

ESD Alliance Representative
Graham Bell
Uniquify, Inc.
gbell786@yahoo.com

IEEE/CEDA Representative
David Atienza
EPFL
david.atienza@epfl.ch

Conference Manager
Kevin Lepine
MP Associates, Inc.
kevin@mpassociates.com

Exhibit Manager
Lee Wood
MP Associates, Inc.
lee@mpassociates.com

THANK YOU

TO THE FOLLOWING EXHIBITORS FOR THEIR SUPPORT OF:

AISLE SIGNS

flexlogix Technologies, Inc.

CONFERENCE BAG, DAC T-SHIRT

cadence®

IP TRACK

ChipEstimate.com™

STUDENT EVENTS

cadence® ACADEMIC NETWORK

SYNOPSYS® Silicon to Software™

I LOVE DAC

CLIO SOFT

onespin

Tru:chip The Verification IP Specialist

BADGE/LANYARD, DESIGNER TRACK

Mentor® A Siemens Business

MONDAY & TUESDAY RECEPTIONS

AMIQ

SUNDAY, MONDAY & TUESDAY ATTENDEE COFFEE BREAKS

ANSYS®

EXHIBIT FLOOR SEATING

SYNOPSYS® Silicon to Software™

REGISTRATION

Empyrean

MAP GUIDE

Consensia

DASSAULT SYSTEMES

THANK YOU

TO OUR LOYAL SUPPORTERS:

Platinum Exhibitors

cadence®

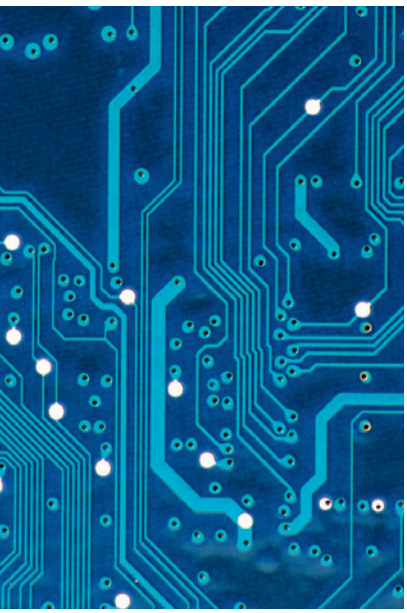
Mentor®
A Siemens Business

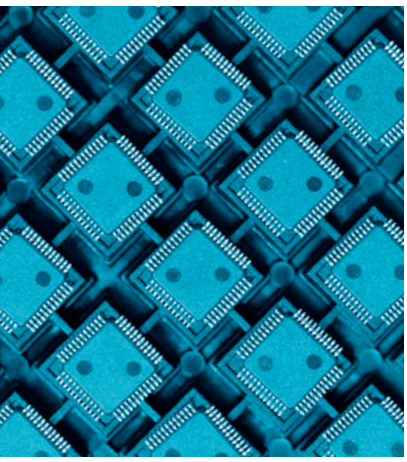
SYNOPSYS®
Silicon to Software™

DATE 2018

SAVE THE DATE

follow us on





MARCH 19—23, 2018

DRESDEN, GERMANY

ICC — International Congress Center

DATE 18

www.date-conference.com

Design, Automation and Test in Europe

Listing as of May 15, 2017

HOT Benefit Party at DAC

Monday, June 19 • 7:00pm – 11:00pm
Speakeasy Austin • 412 Congress Avenue

ORGANIZED BY

Heart OF TECHNOLOGY

DONATIONS BENEFIT

The Gary Smith Foundation Scholarship at San Jose State University

SPEAKEASY SPONSORS

Solido • Team Hogan

SCHOLARSHIP SPONSORS

ARM • ESD Alliance • eSilicon • Harvest Partners • Lori Kate Smith • Mentor OneSpin • Runtime • Semifore • Sonics • Synopsys

MEDIA SPONSORS: DeepChip • SemiWiki

PARTY WITH HOT FOR A GREAT CAUSE!

Featured Entertainment: Vista Roads Band with special guests The JD Experience

heartoftechnology.org

Listing as of May 15, 2017

NOTES

ENCOUNTER THE WORLD OF IoT

- Maker's Market
- Find Your IP @ DAC – **Part of DAC ATTACK**
- Teardowns
- VR Experience: Enter Another Realm of Reality

KEEP WEIRD

- Keep IoT Weird Tech Puzzle – **Part of DAC ATTACK**

DAC ATTACK

All activities part of DAC ATTACK
Download the App and Play to Win

ANDROID APP ON Google play

Available on the App Store

Stop by booth #1038 and find out how Dell EMC can speed up your EDA workflows.

What you see might just knock your SoCs off!

www.dellemc.com

DELL EMC