Field-Effect Transistors Using Silicon Nanowires Prepared by Electroless Chemical Etching

M. Zaremba-Tymieniecki, C. Li, K. Fobelets, and Z. A. K. Durrani

***Abstract*—Silicon nanowires, prepared by electroless chemical etching, are used to fabricate dual-gate field-effect transistors. The diameters of the nanowires vary from 40–300 nm, with a maximum aspect ratio of ∼3000. Titanium silicide contacts are fabricated on single nanowires. An aluminium top-gate, combined with a back-gate, forms a dual-gate transistor. In an n-channel device with a nanowire diameter of ∼70 nm, the output characteristics show current saturation, with a maximum current of ∼100 nA. A drain-source threshold voltage exists for current flow, controlled by the gate voltage, and assists in device turn-off. The ON/OFF current ratio is ∼3000, and the subthreshold swing is ∼780 mV/decade.**

***Index Terms*—Electroless chemical etching, nanoelectronics, nanowire MOSFET, silicon nanowire.**

I. Introduction

In recent years, silicon nanowires (SiNWs) have generated great interest for the fabrication of nanometer-scale devices for integrated circuit, sensor, optoelectronic, and thermoelectric applications [1]–[3]. In particular, SiNWs have been investigated for nanoscale field-effect transistor (FET) fabrication for continued scaling into the ∼10 nm regime [1]. Silicon nanowires, prepared by "bottom-up" techniques such as vapor-liquid solid (VLS) growth [4], [5] or by "top-down" lithographic techniques [6], [7] may be defined with diameters < 10 nm and lengths ∼100 μm. For FET applications, VLS SiNWs may be deposited or grown directly on a suitable substrate [8], [9] while lithographically defined SiNWs may be fabricated in silicon-on-insulator material [10].

SiNWs have also been prepared by electroless chemical etching of Si wafers [11]. Here, the electroless deposition of an Ag dendritic network on the Si wafer catalyses subsequent chemical etching of a SiNW array. Vertical large aspect ratio and densely packed NWs are formed over the entire Si surface. Nanowire diameters from ∼20–300 nm and with lengths up to ∼150 μm have been demonstrated [3], [12]. These NWs have been used to define p-channel FETs with NW diameter ∼180 nm, an underlying "back-gate," and Au contacts. Here, an on-off current ratio $I_{\rm on}/I_{\rm off} \sim 10^4$ and a subthreshold swing $S = 760$ mV/decade was reported [12]. However, there is limited work on FETs using these NWs in comparison with VLS-grown NWs.

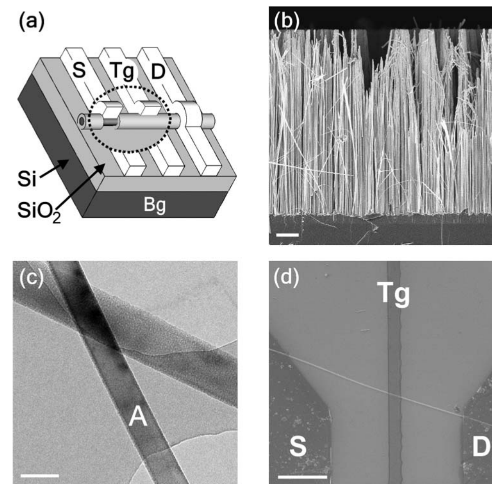

Fig. 1. (a) Schematic diagram of dual-gate SiNW FET with $\mathrm{Ti}_x\mathrm{Si}_y$/Al source (S) and drain (D) contacts, Al top-gate (Tg), and substrate back-gate (Bg). (b) Scanning electron micrograph of chemically etched SiNW array. (c) Transmission electron micrograph of the SiNWs. (d) Scanning electron micrograph of SiNW FET. The scale bars are 10 μm, 100 nm, and 10 μm, respectively.

In this letter, we demonstrate dual-gate FETs in SiNWs fabricated using electroless chemical etching. We fabricate $\mathrm{Ti}_x\mathrm{Si}_y/\mathrm{Al}$ source/drain contacts on single SiNWs, with a dual-gate formed by an Al top-gate and a substrate "back-gate" [Fig. 1(a)]. In a FET with a ∼70 nm diameter SiNW, the drain-source current $(I_{\rm DS})$—voltage $(V_{\rm DS})$ output characteristics, with simultaneously applied top- and back-gate voltages $V_{\rm TG}$ and $V_{\rm BG}$, show current saturation with maximum $I_{\rm DS} \sim 100$ nA. A drain-source threshold voltage for current flow, controlled by the gate voltages, assists in device turn-off. In the FET transfer $(I_{\rm DS} - V_{\rm BG}, V_{\rm TG})$ characteristics, we measure $I_{\rm on}/I_{\rm off} \sim 3000$ and $S \sim 780$ mV/decade. The device may be analyzed using Schottky barrier contacts, in series with a FET formed by the SiNW.

II. Device Fabrication

The SiNWs were synthesised from a p-type, Sb-doped silicon (100) wafer (resistivity $\rho \sim 10^{-2}$ Ωcm). A Si sample was immersed in HF/$\mathrm{AgNO_3}$ solution at room temperature for 5 minutes. Here, an electroless deposition (galvanic exchange) process [11] forms a network of Ag dendrites on the Si surface. Etching is continued using mainly nitrate ions as the oxidizing agent. Etching for three hours produces a densely

Manuscript received March 10, 2010; revised April 30, 2010; accepted May 4, 2010. Date of publication June 28, 2010; date of current version July 23, 2010. The review of this letter was arranged by Editor C. Bulucea.

The authors are with the Department of Electrical and Electronic Engineering, Imperial College London, South Kensington Campus, SW7 2AZ London, U.K. (e-mail: michal.tymieniecki08@imperial.ac.uk; chuanbo.li@imperial.ac.uk; k.fobelets@imperial.ac.uk; z.durrani@imperial.ac.uk).

Digital Object Identifier 10.1109/LED.2010.2050572

0741-3106/$26.00 © 2010 IEEE

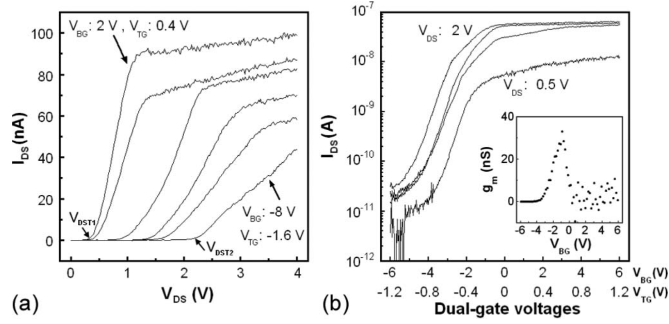

Fig. 2. (a) $I_{\rm DS}$–$V_{\rm DS}$ output characteristics of a SiNW FET. $V_{\rm BG}$ is varied from 2 V to -8 V in -2 V steps and $V_{\rm TG}$ is varied from 0.4 V to -1.6 V in -0.4 V steps. $V_{\rm DST}$ is seen to vary from $V_{\rm DST1} = 0.3$ V to $V_{\rm DST2} = 2.3$ V (b) $I_{\rm DS}$–$V_{\rm BG}$, $V_{\rm TG}$ transfer characteristics (log scale), as $V_{\rm DS}$ is varied from 2 V to 0.5 V in 0.5 V steps. The inset shows extracted g_m versus $V_{\rm BG}$ for $V_{\rm DS} = 1.5$ V. $V_{\rm TG}$ (not shown) is varied simultaneously with $V_{\rm BG}$, in the ratio 1 : 5.

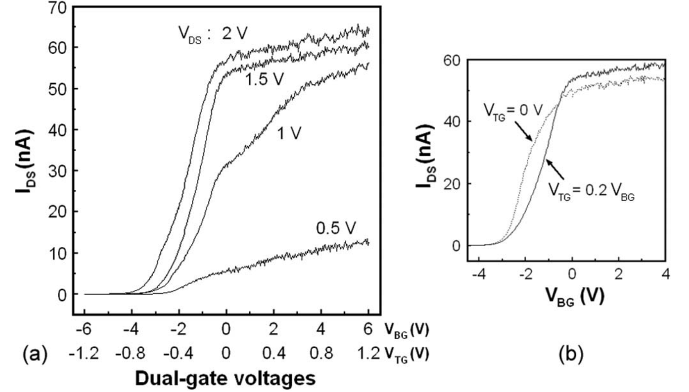

Fig. 3. (a) $I_{\rm DS}$–$V_{\rm BG}$, $V_{\rm TG}$ transfer characteristics (linear scale) of a SiNW FET, as $V_{\rm DS}$ is varied from 2 V to 0.5 V in 0.5 V steps. (b) $I_{\rm DS}$–$V_{\rm BG}$ characteristics at $V_{\rm DS} = 1.5$ V, for $V_{\rm TG} = 0$ V, and for $V_{\rm TG} = 0.2V_{\rm BG}$.

packed vertical array of $\sim$300 μm-long NWs. HNO_3 is then used to remove the Ag. Fig. 1(b) shows a scanning electron micrograph of a SiNW array, with NW diameter of 40–300 nm. The NW packing density is $\sim 10^9/{\rm cm}^2$. Nanowires with a diameter of $\sim$100 nm can be $\sim$300 μm-long, for an aspect ratio of $\sim$3000. Fig. 1(c) shows a transmission electron micrograph of the SiNWs. The SiNW marked "A" has a crystalline core 60 nm in diameter, with a $\sim$5-nm-thick native oxide shell.

Nanowires from the array were dispersed in isopropyl alcohol using ultrasonic agitation and then deposited from this solution on a SiO_2 (130 nm thick) on p-Si substrate. The sample was then oxidised at 850 °C for 5 min to passivate the NW surface and form a $\sim$10 nm surface oxide. ${\rm Ti}_x{\rm Si}_y$ contacts were defined on single selected NWs using optical lithography. Here, 40 nm of Ti was thermally evaporated after an oxide strip and excess metal was removed using "lift-off." The Ti was then annealed at 700 °C for 30 sec. Here, a "snowplow" process [13] dissociated SiO_2 at the Si/Ti interface, driving oxygen to the surface and forming a ${\rm Ti}_x{\rm Si}_y$ contact covered by a thin ${\rm TiO}_x$ layer. The ${\rm TiO}_x$ layer was then removed using buffered HF and a 100-nm Al capping layer thermally evaporated to complete the contact. Finally, a $\sim$2 μm-wide and 100-nm-thick Al top-gate was defined on the NW. Fig. 1(d) shows a scanning electron micrograph of a device with a $\sim$250-nm diameter SiNW.

III. Results and Discussion

Fig. 2 shows the dual-gate characteristics of a SiNW device. Here, the NW core diameter was $\sim$70 nm and the source-drain separation was 45 μm. The large source-drain separation implies a continuous NW conduction path over tens of micrometers. The characteristics were measured at 300 K with an Agilent 4155B parameter analyzer. Fig. 2(a) shows the $I_{\rm DS}$–$V_{\rm DS}$ characteristics, where $V_{\rm TG}$ and $V_{\rm BG}$ are varied in a constant proportion of 1 : 5, in a manner similar to a dynamic threshold FET [14]. $V_{\rm BG}$ is varied from 2 V to -8 V and $V_{\rm TG}$ is varied from 0.4 V to -1.6 V. Both the saturation current and drain-source threshold voltage $V_{\rm DST}$ for current flow are modulated by the gate voltages. $I_{\rm DS}$ reduces in value as the gate voltages decrease, implying n-channel FET operation even though the SiNWs were nominally doped p-type. $V_{\rm DST}$ shifts from 0.3–2.3 V as the gate voltages decrease, and this helps turn the device "off." Fig. 2(b) shows the $I_{\rm DS}$–$V_{\rm BG}$, $V_{\rm TG}$ characteristics for $V_{\rm DS} = 2 - 0.5$ V on a log scale. Here, maximum $I_{\rm on}/I_{\rm off} = 60$ nA/20 pA $= 3000$ at $V_{\rm DS} = 1.5$ V. The inset to Fig. 2(b) shows the transconductance g_m versus gate voltage at $V_{\rm DS} = 1.5$ V. The peak value of $g_m = dI_{\rm DS}/dV_{\rm GS} \sim 30$ nS and the subthreshold swing $S = 780$ mV/decade.

Fig. 3(a) shows the dual-gate transfer characteristics of the device on a linear-scale for $V_{\rm DS} = 2 - 0.5$ V. Fig. 3(b) compares the dual-gate characteristics to the back-gate only characteristics at $V_{\rm DS} = 1.5$ V. The modulation of $I_{\rm DS}$ is enhanced with dual-gate operation, with larger values of $I_{\rm on}$ for positive gate voltages and a comparatively sharper transition from $I_{\rm on}$ to $I_{\rm off}$.

The electrical characteristics of the device are influenced by Schottky barriers (SBs) formed at the NW contacts and by charge trapped at or near the NW surface. The inversion of the charge carrier type from p-type in the source Si wafer to n-type in Figs. 2 and 3 implies positive fixed charge at the NW surface or in the gate oxide. This can lower the conduction (E_c) and valence (E_v) energy band edges in the NW relative to the Fermi energy E_F and invert the NW from p- to n-type. Inversion from n- to p-type due to surface effects has been reported in similar NWs [12].

Fig. 4(a) show schematically the energy band diagram in our n-channel SiNW FET. We assume that SBs exist at the NW source/drain contacts [15] and that $V_{\rm TG}$ is varied in tandem with $V_{\rm BG}$. Applying $V_{\rm DS} > 0$ V at $V_{\rm BG} = 0$ V allows electron injection across the source SB. If $V_{\rm BG} < 0$ V, then the upward shift in E_c increases the source SB width a and the band offset eV_b, reducing $I_{\rm DS}$. The increase in eV_b increases $V_{\rm DST}$, similar to our observed behavior [Fig. 2(a)]. The top-gate in our device is less effective, as it does not modulate the NW "lead" regions that lie on either side.

Modeling our device as a NW FET with series SBs for $V_{\rm DS} > V_{\rm DST}$ the source SB turns-on. The source resistance R_S (Fig. 4(d), inset) is associated with this SB after turn-on and any additional source contact resistance. The drain SB is forward biased [Fig. 4(a)] with resistance $R_D \ll R_S$. Subtracting $V_{\rm DST}$ from $V_{\rm DS}$ removes the effect of the SBs from the data, allowing

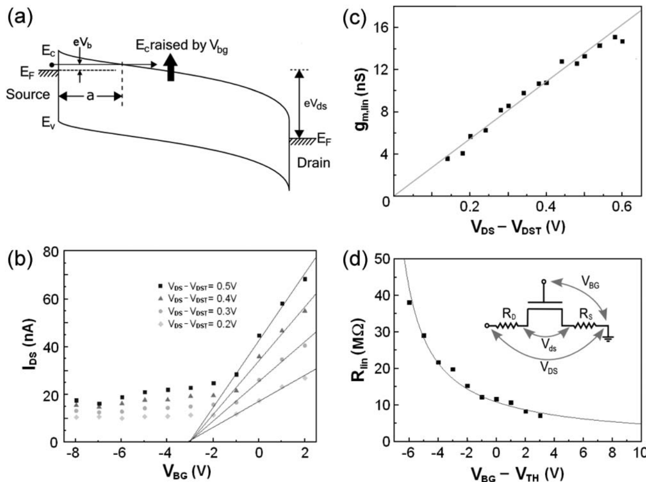

Fig. 4. (a) Energy band diagram of the SiNW FET with electron injection from the source, $V_{\mathrm{DS}} > 0$ V. (b) I_{DS}–V_{BG} characteristics at $V_{\mathrm{DS}} - V_{\mathrm{DST}} =$ 0.5 V − 0.2 V, extracted from the data of Fig. 2(a). (c) $g_{m,\mathrm{lin}}$ versus $(V_{\mathrm{DS}} - V_{\mathrm{DST}})$ characteristics. (d) R_{lin} versus $(V_{\mathrm{BG}} - V_{\mathrm{TH}})$ characteristics. Inset shows the contact resistance circuit model.

the extraction of parameters associated with the NW only. Fig. 4(b) shows I_{DS} versus V_{BG} as $V_{\mathrm{DS}} - V_{\mathrm{DST}}$ is varied. Above a threshold gate voltage $V_{\mathrm{TH}} \approx -3$ V, $I_{\mathrm{DS}} \propto V_{\mathrm{BG}}$ as expected for a FET in the linear region [16]. Here, $I_{\mathrm{DS}} = \mu_{\mathrm{FE}} C_{\mathrm{ox}} (V_{\mathrm{DS}} - V_{\mathrm{DST}})(V_{\mathrm{BG}} - V_{\mathrm{TH}})/L^2$, where C_{ox} is the oxide capacitance, μ_{FE} is the electron field-effect mobility, and L is the NW length. The peak value of $g_m = 30$ nS [Fig. 2(b), inset] and the minimum $S = 780$ mV/decade occurs with V_{BG} near V_{TH} as the SB offset eV_b reduces. Fig. 4(b) may be used to extract the extrinsic linear region transconductance $g_{m,\mathrm{lin}} = \partial I_{\mathrm{DS}}/\partial V_{\mathrm{BG}}$. We find $g_{m,\mathrm{lin}} \propto V_{\mathrm{DS}} - V_{\mathrm{DST}}$ [Fig. 4(c)], again following linear FET behavior, where $g_{m,\mathrm{lin}} = \mu_{\mathrm{FE}} C_{\mathrm{ox}} (V_{\mathrm{DS}} - V_{\mathrm{DST}})/L^2$. Finally, we estimate R_S from a plot of the extrinsic drain-source resistance in the linear region $R_{\mathrm{lin}} = R_{\mathrm{ds}} + R_S = \partial V_{\mathrm{DS}}/\partial I_{\mathrm{DS}}$ versus gate overdrive $V_{\mathrm{BG}} - V_{\mathrm{TH}}$ [Fig. 4(d)]. The data fits $R_{\mathrm{lin}} \propto 1/(V_{\mathrm{BG}} - V_{\mathrm{TH}})$, as expected. At large gate overdrive $R_{\mathrm{ds}} \ll R_S$, implying $R_S \sim 1$ MΩ.

The intrinsic linear region transconductance may be estimated using $g_{m0} = g_{m,\mathrm{lin}}/(1 - (g_d + g_{m,\mathrm{lin}})R_S)$, using a calculation similar to [17]. Here, $g_d = \partial I_{\mathrm{DS}}/\partial V_{\mathrm{DS}}$. Using maximum values, $g_{m,\mathrm{lin}} = 10$ nS and $g_d = 130$ nS at $V_{\mathrm{DS}} - V_{\mathrm{DST}} = 0.5$ V and $V_{\mathrm{BG}} = 2$ V, and assuming a constant value of $R_S = 1$ MΩ, gives $g_{m0} \sim 12$ nS. We may use g_{m0} to estimate the range of μ_{FE}. Using $\mu_{\mathrm{FE}} = g_{m0} L^2 / C_{\mathrm{ox}} V_{\mathrm{ds}}$ and $C_{\mathrm{ox}} \sim 5 \times 10^{-15}$ F (estimated from the ideal capacitance between a cylinder and a plane) [18], we find $\mu_{\mathrm{FE}} \sim 100\ \mathrm{cm}^2/\mathrm{Vs}$. We note that we have neglected the forward-bias drain SB resistance R_D and any additional drain contact resistances. R_S may also reduce as V_{DS} increases, with further turn-on of the source SB. Our R_S may then be overestimated, suggesting lower values of g_{m0} and μ_{FE}.

ACKNOWLEDGMENT

The authors would like to thank M. Green, V. Stevens, Japan Science and Technology, and E.ON International Research Initiative.

REFERENCES

[1] J. Appenzeller, J. Knoch, M. T. Bjork, H. Riel, H. Schmid, and W. Riess, “Toward nanowire electronics,” *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 2827–2845, Nov. 2008.

[2] Y. Li, F. Qian, J. Xiang, and C. M. Lieber, “Nanowire electronic and optoelectronic devices,” *Mater. Today*, vol. 9, no. 10, pp. 18–27, Oct. 2006.

[3] A. I. Hochbaum, R. Chen, R. D. Delgado, W. Liang, E. C. Garnett, M. Najarian, A. Majumdar, and P. Yang, “Enhanced thermoelectric performance of rough silicon nanowires,” *Nature*, vol. 451, no. 7175, pp. 163–167, Jan. 2008.

[4] Y. Wu, Y. Cui, L. Huynh, C. J. Barrelet, D. C. Bell, and C. M. Lieber, “Controlled growth and structures of molecular-scale silicon nanowires,” *Nano Lett.*, vol. 4, no. 3, pp. 433–436, Mar. 2004.

[5] A. M. Morales and C. M. Lieber, “A laser ablation method for the synthesis of crystalline semiconductor nanowires,” *Science*, vol. 279, no. 5348, pp. 208–211, Jan. 1998.

[6] H. Xuejue, L. Wen-Chin, C. Kuo, D. Hisamoto, C. Leland, J. Kedzierski, E. Anderson, H. Takeuchi, C. Yang-Kyu, K. Asano, V. Subramanian, K. Tsu-Jae, J. Bokor, and H. Chenming, “Sub-50 nm P-channel FinFET,” *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 880–886, May 2001.

[7] L. Hyunjin, Y. Lee-Eun, R. Seong-Wan, H. Jin-Woo, J. Kanghoon, J. Dong-Yoon, K. Kuk-Hwan, L. Jiye, K. Ju-Hyun, C. J. Sang, S. L. Gi, S. O. Jae, C. P. Yun, H. B. Woo, M. L. Hee, M. Y. Jun, J. Y. Jung, I. K. Sang, and C. Yang-Kyu, “Sub-5 nm all-around gate FinFET for ultimate scaling,” in *VLSI Symp. Tech. Dig.*, 2006, vol. 58, pp. 58–59.

[8] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, “High performance silicon nanowire field effect transistors,” *Nano Lett.*, vol. 3, no. 2, pp. 149–152, Feb. 2003.

[9] A. Colli, A. Fasoli, P. Beecher, P. Servati, S. Pisana, Y. Fu, A. J. Flewitt, W. I. Milne, J. Robertson, C. Ducati, S. De Franceschi, S. Hofmann, and A. C. Ferrari, “Thermal and chemical vapor deposition of Si nanowires: Shape control, dispersion, and electrical properties,” *J. Appl. Phys.*, vol. 102, no. 3, pp. 034 302–034 313, Aug. 2007.

[10] O. Gunawan, L. Sekaric, A. Majumdar, M. Rooks, J. Appenzeller, J. W. Sleight, S. Guha, and W. Haensch, “Measurement of carrier mobility in silicon nanowires,” *Nano Lett.*, vol. 8, no. 6, pp. 1566–1571, Jun. 2008.

[11] K. Q. Peng, Y. J. Yan, S. P. Gao, and J. Zhu, “Synthesis of large-area silicon nanowire arrays via self-assembling nanoelectrochemistry,” *Adv. Mater.*, vol. 14, no. 16, pp. 1164–1167, Aug. 2002.

[12] J. Jie, W. Zhang, K. Peng, G. Yuan, C. S. Lee, and S.-T. Lee, “Surface-dominated transport properties of silicon nanowires,” *Adv. Funct. Mater.*, vol. 18, no. 20, pp. 3251–3257, Oct. 2008.

[13] P. Merchant and J. Amano, “Oxygen redistribution during sintering of Ti/Si structures,” *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 2, no. 4, pp. 762–765, Oct. 1984.

[14] F. Assaderaghi, S. Parke, D. Sinitsky, J. Bokor, P. K. Ko, and H. Chenming, “A dynamic threshold voltage MOSFET (DTMOS) for very low voltage operation,” *IEEE Electron Device Lett.*, vol. 15, no. 12, pp. 510–512, Dec. 1994.

[15] J. Appenzeller, J. Knoch, E. Tutuc, M. Reuter, and S. Guha, “Dual-gate silicon nanowire transistors with nickel silicide contacts,” in *IEDM Tech. Dig.*, 2006, vol. 1, pp. 1–4.

[16] S. M. Sze, *Physics of Semiconductor Device*. Hoboken, NJ: Wiley, 1981.

[17] V. Gaspari, K. Fobelets, J. E. Velazquez-Perez, and T. Hackbarth, “DC performance of deep submicrometer Schottky-gated n-channel Si:SiGe HFETs at low temperatures,” *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 2067–2074, Sep. 2005.

[18] O. Hayden, T. Björk, H. Schmid, H. Riel, U. Drechsler, S. F. Karg, E. Lörtscher, and W. Riess, “Fully depleted nanowire field-effect transistor in inversion mode,” *Small*, vol. 3, no. 2, pp. 230–234, Feb. 2007.